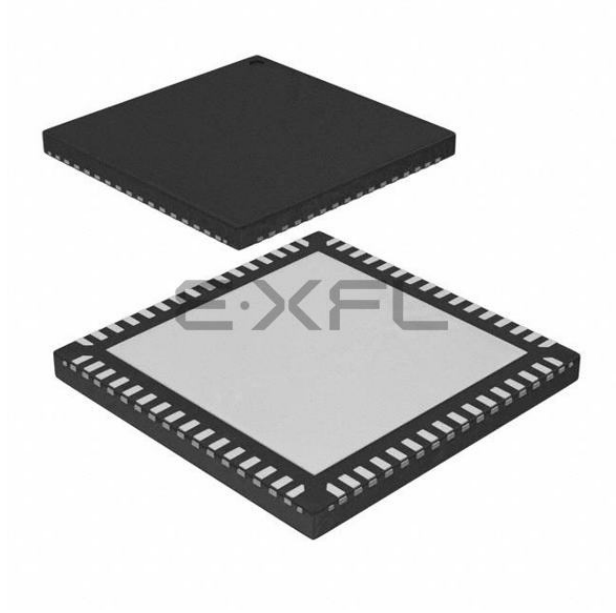

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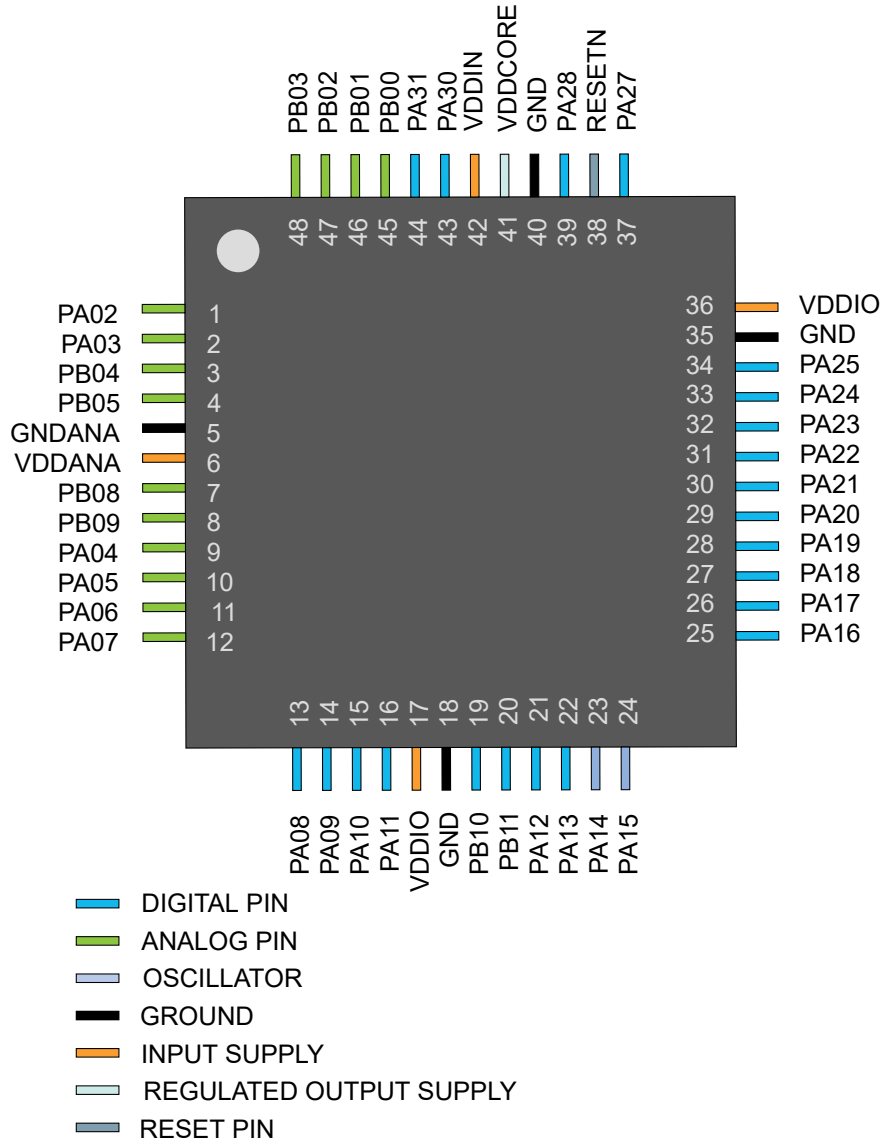
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j18a-mf

5.3 SAM D21GxL

5.3.1 QFN48



8.2.4.2 Maximum Rise Rate

The rise rate of the power supply must not exceed the values described in Electrical Characteristics. Refer to the *Electrical Characteristics* for details.

Related Links

37. Electrical Characteristics

8.3 Power-Up

This section summarizes the power-up sequence of the device. The behavior after power-up is controlled by the Power Manager. Refer to *PM – Power Manager* for details.

Related Links

16. PM – Power Manager

8.3.1 Starting of Clocks

After power-up, the device is set to its initial state and kept in reset, until the power has stabilized throughout the device. Once the power has stabilized, the device will use a 1MHz clock. This clock is derived from the 8MHz Internal Oscillator (OSC8M), which is divided by eight and used as a clock source for generic clock generator 0. Generic clock generator 0 is the main clock for the Power Manager (PM).

Some synchronous system clocks are active, allowing software execution.

Refer to the “Clock Mask Register” section in *PM – Power Manager* for the list of default peripheral clocks running. Synchronous system clocks that are running are by default not divided and receive a 1MHz clock through generic clock generator 0. Other generic clocks are disabled except GCLK_WDT, which is used by the Watchdog Timer (WDT).

Related Links

16. PM – Power Manager

8.3.2 I/O Pins

After power-up, the I/O pins are tri-stated.

8.3.3 Fetching of Initial Instructions

After reset has been released, the CPU starts fetching PC and SP values from the reset address, which is 0x00000000. This address points to the first executable address in the internal Flash. The code read from the Internal Flash is free to configure the clock system and clock sources. Refer to *PM – Power Manager*, *GCLK – Generic Clock Controller* and *SYSCTRL – System Controller* for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

Related Links

16. PM – Power Manager
17. SYSCTRL – System Controller
14. Clock System

8.4 Power-On Reset and Brown-Out Detector

The SAM D21 embeds three features to monitor, warn and/or reset the device:

- POR: Power-On Reset on VDDANA

13.13.4 Address

Name: ADDR
Offset: 0x0004
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	ADDR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[5:0]						AMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:2 – ADDR[29:0] Address
Initial word start address needed for memory operations.

Bits 1:0 – AMOD[1:0] Access Mode
The functionality of these bits is dependent on the operation mode.

Bit description when operating CRC32: refer to 13.11.3 32-bit Cyclic Redundancy Check CRC32

Bit description when testing onboard memories (MBIST): refer to 13.11.5 Testing of On-Board Memories MBIST

13.13.11 CoreSight ROM Table Entry 1

Name: ENTRY1
Offset: 0x1004
Reset: 0xXXXXX00X
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	ADDOFF[19:12]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	23	22	21	20	19	18	17	16
	ADDOFF[11:4]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
	ADDOFF[3:0]							
Access	R	R	R	R				
Reset	x	x	x	x				

Bit	7	6	5	4	3	2	1	0
							FMT	EPRES
Access							R	R
Reset							1	x

Bits 31:12 – ADDOFF[19:0] Address Offset
The base address of the component, relative to the base address of this ROM table.

Bit 1 – FMT Format
Always read as '1', indicating a 32-bit ROM table.

Bit 0 – EPRES Entry Present
This bit indicates whether an entry is present at this location in the ROM table.

This bit is set at power-up if the device is not protected indicating that the entry is not present.

This bit is cleared at power-up if the device is not protected indicating that the entry is present.

TRIGACT[1:0]	Name	Description
0x2	BEAT	One trigger required for each beat transfer
0x3	TRANSACTION	One trigger required for each transaction

Bits 13:8 – TRIGSRC[5:0] Trigger Source
These bits define the peripheral trigger which is source of the transfer. For details on trigger selection and trigger modes, refer to Transfer Triggers and Actions and CHCTRLB.TRIGACT.

Value	Name	Description
0x00	DISABLE	Only software/event triggers
0x01	SERCOM0 RX	SERCOM0 RX Trigger
0x02	SERCOM0 TX	SERCOM0 TX Trigger
0x03	SERCOM1 RX	SERCOM1 RX Trigger
0x04	SERCOM1 TX	SERCOM1 TX Trigger
0x05	SERCOM2 RX	SERCOM2 RX Trigger
0x06	SERCOM2 TX	SERCOM2 TX Trigger
0x07	SERCOM3 RX	SERCOM3 RX Trigger
0x08	SERCOM3 TX	SERCOM3 TX Trigger
0x09	SERCOM4 RX	SERCOM4 RX Trigger
0x0A	SERCOM4 TX	SERCOM4 TX Trigger
0x0B	SERCOM5 RX	SERCOM5 RX Trigger
0x0C	SERCOM5 TX	SERCOM5 TX Trigger
0x0D	TCC0 OVF	TCC0 Overflow Trigger
0x0E	TCC0 MC0	TCC0 Match/Compare 0 Trigger
0x0F	TCC0 MC1	TCC0 Match/Compare 1 Trigger
0x10	TCC0 MC2	TCC0 Match/Compare 2 Trigger
0x11	TCC0 MC3	TCC0 Match/Compare 3 Trigger
0x12	TCC1 OVF	TCC1 Overflow Trigger
0x13	TCC1 MC0	TCC1 Match/Compare 0 Trigger
0x14	TCC1 MC1	TCC1 Match/Compare 1 Trigger
0x15	TCC2 OVF	TCC2 Overflow Trigger
0x16	TCC2 MC0	TCC2 Match/Compare 0 Trigger
0x17	TCC2 MC1	TCC2 Match/Compare 1 Trigger
0x18	TC3 OVF	TC3 Overflow Trigger
0x19	TC3 MC0	TC3 Match/Compare 0 Trigger
0x1A	TC3 MC1	TC3 Match/Compare 1 Trigger
0x1B	TC4 OVF	TC4 Overflow Trigger
0x1C	TC4 MC0	TC4 Match/Compare 0 Trigger
0x1D	TC4 MC1	TC4 Match/Compare 1 Trigger
0x1E	TC5 OVF	TC5 Overflow Trigger
0x1F	TC5 MC0	TC5 Match/Compare 0 Trigger
0x20	TC5 MC1	TC5 Match/Compare 1 Trigger
0x21	TC6 OVF	TC6 Overflow Trigger
0x22	TC6 MC0	TC6 Match/Compare 0 Trigger
0x23	TC6 MC1	TC6 Match/Compare 1 Trigger
0x24	TC7 OVF	TC7 Overflow Trigger
0x25	TC7 MC0	TC7 Match/Compare 0 Trigger

20.10.3 Block Transfer Source Address

Name: SRCADDR
Offset: 0x04
Property: -

The SRCADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	31	30	29	28	27	26	25	24
	SRCADDR[31:24]							
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SRCADDR[23:16]							
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SRCADDR[15:8]							
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SRCADDR[7:0]							
Access								
Reset								

Bits 31:0 – SRCADDR[31:0] Transfer Source Address
This bit group holds the source address corresponding to the last beat transfer address in the block transfer.

21. EIC – External Interrupt Controller

21.1 Overview

The External Interrupt Controller (EIC) allows external pins to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt on rising, falling, or both edges, or on high or low levels. Each external pin has a configurable filter to remove spikes. Each external pin can also be configured to be asynchronous in order to wake up the device from sleep modes where all clocks have been disabled. External pins can also generate an event.

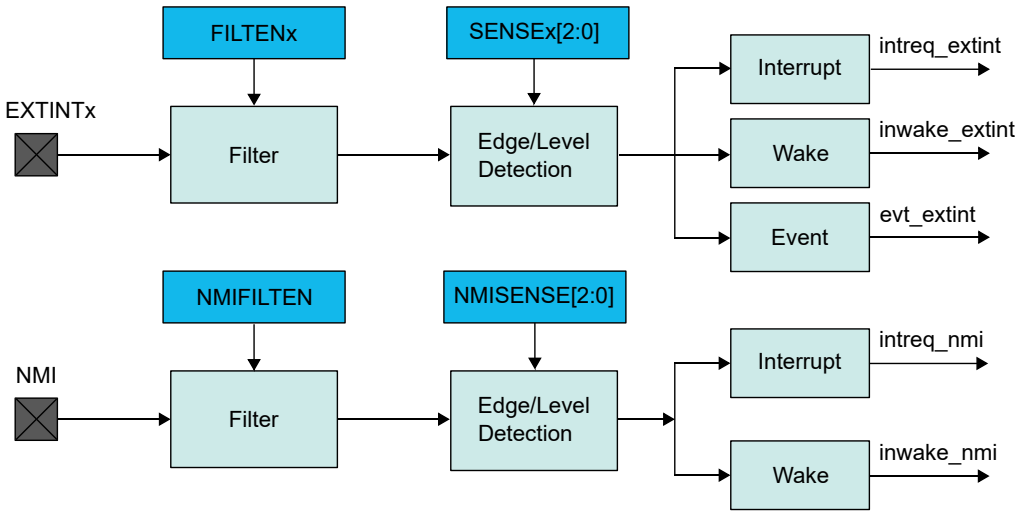
A separate non-maskable interrupt (NMI) is also supported. It has properties similar to the other external interrupts, but is connected to the NMI request of the CPU, enabling it to interrupt any other interrupt mode.

21.2 Features

- Up to 16 external pins (EXTINTx), plus one non-maskable pin (NMI)
- Dedicated, individually maskable interrupt for each pin
- Interrupt on rising, falling, or both edges
- Interrupt on high or low levels
- Asynchronous interrupts for sleep modes without clock
- Filtering of external pins
- Event generation from EXTINTx

21.3 Block Diagram

Figure 21-1. EIC Block Diagram



Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

28.7 Register Summary - I2C Slave

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
		15:8								
		23:16	SEXTTOEN		SDAHOLD[1:0]					PINOUT
		31:24		LOWTOUT			SCLSM		SPEED[1:0]	
0x04	CTRLB	7:0								
		15:8	AMODE[1:0]					AACKEN	GCMD	SMEN
		23:16	FIFOCLR[1:0]					ACKACT	CMD[1:0]	
		31:24								
0x08 ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR			RXFF	TXFE	DRDY	AMATCH	PREC
0x15	Reserved									
0x16	INTENSET	7:0	ERROR			RXFF	TXFE	DRDY	AMATCH	PREC
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR			RXFF	TXFE	DRDY	AMATCH	PREC
0x19	Reserved									
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
		15:8					LENERR	HS	SEXTTOUT	
0x1C	SYNCBUSY	7:0						SYSOP	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20 ... 0x23	Reserved									
0x24	ADDR	7:0	ADDR[6:0]							GENCEN
		15:8	TENBITEN					ADDR[9:7]		
		23:16	ADDRMASK[6:0]							
		31:24						ADDRMASK[9:7]		
0x28	DATA	7:0	DATA[7:0]							
		15:8								
0x2A ... 0x33	Reserved									
0x34	FIFOSPACE	7:0				TXSPACE[4:0]				
		15:8				RXSPACE[4:0]				
0x36	FIFOPTR	7:0					CPUWRPTR[3:0]			
		15:8					CPURDPTR[3:0]			

28.9 Register Summary - I2C Master

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
		15:8								
		23:16	SEXTTOEN	MEXTTOEN	SDAHOLD[1:0]					PINOUT
		31:24		LOWTOUT	INACTOUT[1:0]		SCLSM		SPEED[1:0]	
0x04	CTRLB	7:0								
		15:8							QCEN	SMEN
		23:16	FIFOCLR[1:0]					ACKACT	CMD[1:0]	
		31:24								
0x08 ... 0x0B	Reserved									
0x0C	BAUD	7:0	BAUD[7:0]							
		15:8	BAUDLOW[7:0]							
		23:16	HSBAUD[7:0]							
		31:24	HSBAUDLOW[7:0]							
0x10 ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR			RXFF	TXFE		SB	MB
0x15	Reserved									
0x16	INTENSET	7:0	ERROR			RXFF	TXFE		SB	MB
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR			RXFF	TXFE		SB	MB
0x18	DATA	7:0	DATA[7:0]							
		15:8								
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT	BUSSTATE[1:0]			RXNACK	ARBLOST	BUSERR
		15:8						LENERR	SEXTTOUT	MEXTTOUT
0x1C	SYNCBUSY	7:0						SYSOP	ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20 ... 0x23	Reserved									
0x24	ADDR	7:0	ADDR[7:0]							
		15:8	TENBITEN	HS	LENEN			ADDR[10:8]		
		23:16	LEN[7:0]							
		31:24								
0x28 ... 0x2F	Reserved									
0x30	DBGCTRL	7:0								DBGSTOP
0x31 ...	Reserved									

28.10.9 Address

Name: ADDR
Offset: 0x24
Reset: 0x0000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TENBITEN	HS	LENEN			ADDR[10:8]		
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – LEN[7:0] Transaction Length
These bits define the transaction length of a DMA transaction from 0 to 255 bytes. The Transfer Length Enable (LENEN) bit must be written to '1' in order to use DMA.

Bit 15 – TENBITEN Ten Bit Addressing Enable
This bit enables 10-bit addressing. This bit can be written simultaneously with ADDR to indicate a 10-bit or 7-bit address transmission.

Value	Description
0	10-bit addressing disabled.
1	10-bit addressing enabled.

Bit 14 – HS High Speed
This bit enables High-speed mode for the current transfer from repeated START to STOP. This bit can be written simultaneously with ADDR for a high speed transfer.

Value	Description
0	High-speed transfer disabled.
1	High-speed transfer enabled.

Bit 13 – LENEN Transfer Length Enable

29.9.4 Interrupt Enable Set

Name: INTENSET
Offset: 0x10
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
			TXURx	TXURx			TXRDYx	TXRDYx
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
			RXORx	RXORx			RXRDYx	RXRDYx
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 13,12 – TXURx Transmit Underrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Transmit Underrun Interrupt Enable bit, which enables the Transmit Underrun interrupt.

Value	Description
0	The Transmit Underrun interrupt is disabled.
1	The Transmit Underrun interrupt is enabled.

Bits 9,8 – TXRDYx Transmit Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Transmit Ready Interrupt Enable bit, which enables the Transmit Ready interrupt.

Value	Description
0	The Transmit Ready interrupt is disabled.
1	The Transmit Ready interrupt is enabled.

Bits 4,5 – RXORx Receive Overrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Receive Overrun Interrupt Enable bit, which enables the Receive Overrun interrupt.

Value	Description
0	The Receive Overrun interrupt is disabled.
1	The Receive Overrun interrupt is enabled.

Bits 1,0 – RXRDYx Receive Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

32.8.3.1 Device Endpoint Configuration register n

Name: EPCFGn
Offset: 0x100 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
		EPTYPE1[2:0]				EPTYPE0[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 6:4 – EPTYPE1[2:0] Endpoint Type for IN direction
These bits contains the endpoint type for IN direction.

Upon receiving a USB reset EPCFGn.EPTYPE1 is cleared except for endpoint 0 which is unchanged.

Value	Description
0x0	Bank1 is disabled.
0x1	Bank1 is enabled and configured as Control IN.
0x2	Bank1 is enabled and configured as Isochronous IN.
0x3	Bank1 is enabled and configured as Bulk IN.
0x4	Bank1 is enabled and configured as Interrupt IN.
0x5	Bank1 is enabled and configured as Dual-Bank OUT (Endpoint type is the same as the one defined in EPTYPE0)
0x6-0x7	Reserved

Bits 2:0 – EPTYPE0[2:0] Endpoint Type for OUT direction
These bits contains the endpoint type for OUT direction.

Upon receiving a USB reset EPCFGn.EPTYPE0 is cleared except for endpoint 0 which is unchanged.

Value	Description
0x0	Bank0 is disabled.
0x1	Bank0 is enabled and configured as Control SETUP / Control OUT.
0x2	Bank0 is enabled and configured as Isochronous OUT.
0x3	Bank0 is enabled and configured as Bulk OUT.
0x4	Bank0 is enabled and configured as Interrupt OUT.
0x5	Bank0 is enabled and configured as Dual Bank IN (Endpoint type is the same as the one defined in EPTYPE1)
0x6-0x7	Reserved

32.8.3.6 Device EndPoint Interrupt Enable n

Name: EPINTENCLRn
Offset: 0x108 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Endpoint Interrupt Enable Set (EPINTENSET) register.

Bit	7	6	5	4	3	2	1	0
			STALL	RXSTP		TRFAIL		TRCPT
Access			R/W	R/W		R/W		R/W
Reset			0	0		0		0

Bit 5 – STALL Transmit STALL x Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Transmit Stall x Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Transmit Stall x interrupt is disabled.
1	The Transmit Stall x interrupt is enabled and an interrupt request will be generated when the Transmit Stall x Interrupt Flag is set.

Bit 4 – RXSTP Received Setup Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Received Setup Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Received Setup interrupt is disabled.
1	The Received Setup interrupt is enabled and an interrupt request will be generated when the Received Setup Interrupt Flag is set.

Bit 2 – TRFAIL Transfer Fail x Interrupt Enable
The user should look into the descriptor table status located in ram to be informed about the error condition : ERRORFLOW, CRC.

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Transfer Fail x Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Transfer Fail bank x interrupt is disabled.
1	The Transfer Fail bank x interrupt is enabled and an interrupt request will be generated when the Transfer Fail x Interrupt Flag is set.

Bit 0 – TRCPT Transfer Complete x interrupt Enable
Writing a zero to this bit has no effect.

35.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
						RUNSTDBY	ENABLE	SWRST
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – RUNSTDBY Run in Standby
This bit is not synchronized

Value	Description
0	The DAC output buffer is disabled in standby sleep mode.
1	The DAC output buffer can be enabled in standby sleep mode.

Bit 1 – ENABLE Enable DAC Controller
Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the corresponding bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST Software Reset
Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the DAC to their initial state, and the DAC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
		Calibrated against a 32.768kHz reference at 25°C, over [1.62, 3.63]V	31.293	32.768	34.570	
$i_{OSCULP32K}$(1)(2)			-	-	125	nA
$t_{STARTUP}$	Start-up time		-	10	-	cycles
Duty	Duty Cycle		-	50	-	%

Notes: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

2. This oscillator is always on.

37.13.6 8MHz RC Oscillator (OSC8M) Characteristics

Table 37-56. Internal 8MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 8MHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	7.8	8	8.16	MHz
		Calibrated against a 8MHz reference at 25°C, at V_{DD}=3.3V	7.94	8	8.06	
		Calibrated against a 8MHz reference at 25°C, over [1.62, 3.63]V	7.92	8	8.08	
TempCo	Frequency vs. Temperature drift		-1.2		1	%
SupplyCo	Frequency vs. Supply drift		-2		2	%
I_{OSC8M}	Current consumption	IDLE2 on OSC32K versus IDLE2 on calibrated OSC8M enabled at 8MHz (FRANGE=1, PRESC=0)		64		µA
$t_{STARTUP}$	Startup time		-	2.4	3.3	µs
Duty	Duty cycle		-	50	-	%

37.13.7 Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics

Table 37-57. FDPLL96M Characteristics(1) (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input frequency		32	-	2000	KHz
f_{OUT}	Output frequency		48	-	96	MHz
$I_{FDPLL96M}$	Current consumption	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	500	700	µA
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	900	1200	

Figure 37-14. 1 Sensor / PTC_GCLK = 4MHz / FREQ_MODE_NONE

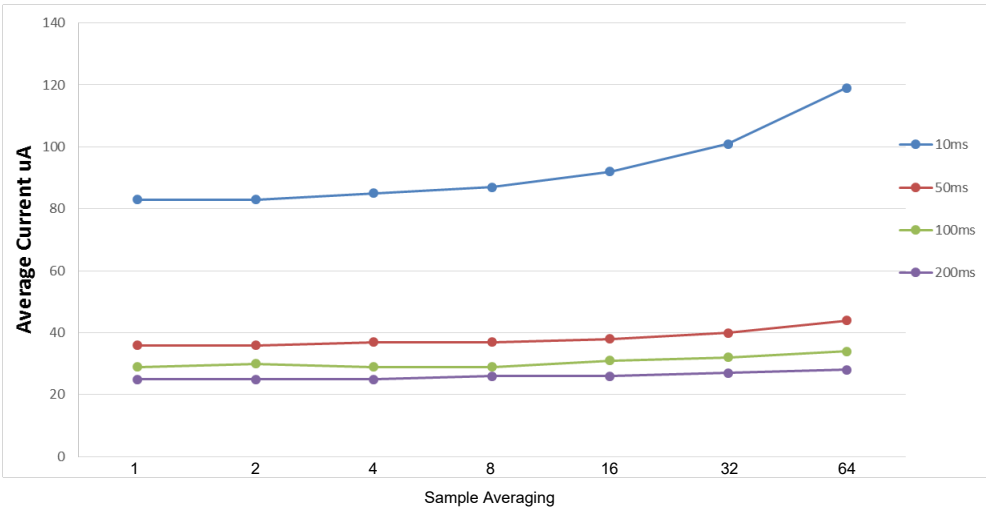
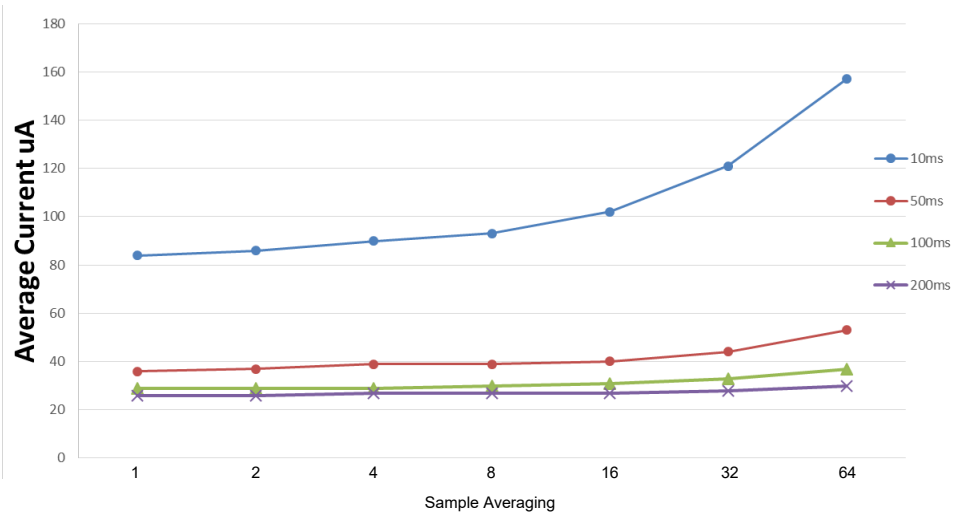


Figure 37-15. 1 Sensor / PTC_GCLK = 2MHz / FREQ_MODE_HOP



Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
t_{SSCKW}	SCK high/low width	Slave		0.5*t_{SSCK}	-	-	
t_{SSCKR}	SCK rise time(2)	Slave		-	-	-	
t_{SSCKF}	SCK fall time(2)	Slave		-	-	-	
t_{SIS}	MOSI setup to SCK	Slave		t_{SSCK}/2 - 9	-	-	
t_{SIH}	MOSI hold after SCK	Slave		t_{SSCK}/2 - 3	-	-	
t_{SSS}	SS setup to SCK	Slave	PRELOADEN =1	2*t_{CLK_APB} + t_{SOS}	-	-	
			PRELOADEN =0	t_{SOS}+7	-	-	
t_{SSH}	SS hold after SCK	Slave		t_{SIH} - 4	-	-	
t_{SOS}	MISO setup SCK	Slave		-	t_{SSCK}/2 - 18	-	
t_{SOH}	MISO hold after SCK	Slave		-	18	-	
t_{SOSS}	MISO setup after SS low	Slave		-	18	-	
t_{SOSH}	MISO hold after SS high	Slave		-	10	-	

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. See 37.9 I/O Pin Characteristics

37.16.3 SERCOM in I²C Mode Timing

This section describes the requirements for devices connected to the I²C Interface Bus.

Figure 37-22. I²C Interface Bus Timing

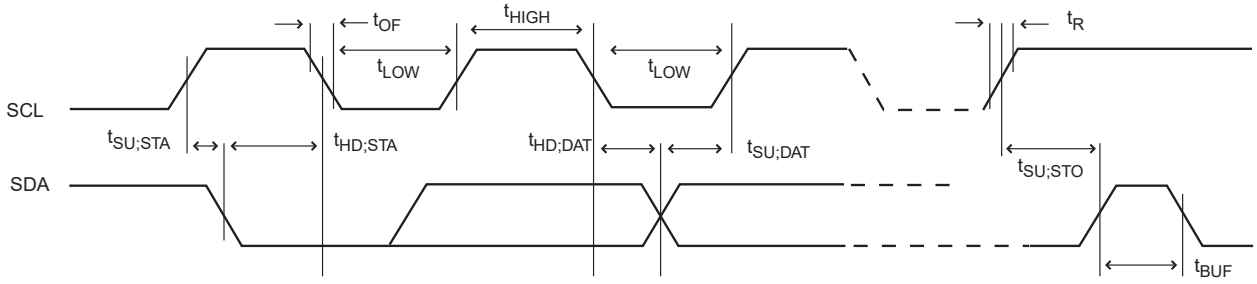
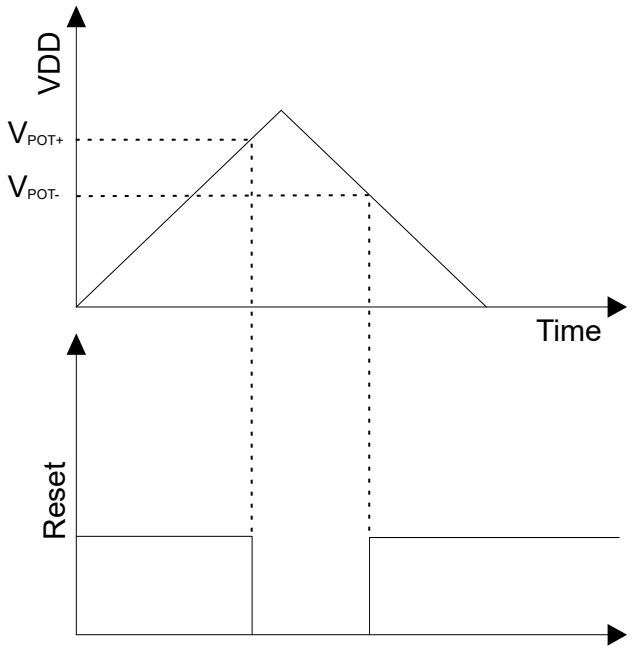


Table 37-63. I²C Interface Timing (Device Variant A)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
t_R	Rise time for both SDA and SCL	Standard / Fast Mode	IC_b(2) = 400pF	-	215	300	ns
		Fast	IC_b(2) = 550pF		60	100	

Figure 38-2. POR Operating Principle



38.6.2 Brown-Out Detectors Characteristics

38.6.2.1 BOD33 Characteristics

Table 38-8. BOD33 Characteristics

Symbol	Parameter	Conditions	Temp.	Min.	Typ.	Max.	Units
I	Step size, between adjacent values in BOD33.LEVEL			-	34	-	mV
V_{HYST}	VBOD+ - VBOD-	Hysteresis ON		35	-	170	mV
t_{DET}	Detection time	Time with $V_{DDANA} < V_{TH}$ necessary to generate a reset signal		-	0.9(1)	-	µs
$I_{IdleBOD33}$	Current consumption om Active/Idle mode	Continuous mode	25°C	-	25	48	µA
			-40- to 105°C	-	-	51	
		Sampling mode	25°C	-	0.034	0.21	
			-40- to 105°C	-	-	2.44	
$I_{SbyBOD33}$	Current consumption in Standby mode	Sampling mode	25°C		0.132	0.38	µA

Table 40-16. PA24/PA25 Pins Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{PULL}	Pull-up - Pull-down resistance	-	20	40	60	kΩ
V_{IL}	Input low-level voltage	VDD = 2.7V-3.63V	-	-	0.29*VDD	V
V_{IH}	Input high-level voltage	VDD = 2.7V-3.63V	0.55*VDD	-	-	
V_{OL}	Output low-level voltage	VDD>2.7V, IOL max	-	0.1*VDD	0.2*VDD	
V_{OH}	Output high-level voltage	VDD>2.7V, IOH max	0.8*VDD	0.9*VDD	-	
I_{OL}	Output low-level current	VDD = 2.7V-3V,	-	-	3	mA
		VDD=3V-3.63V,	-	-	8	
I_{OH}	Output high-level current	VDD=2.7V-3V,	-	-	2	
		VDD = 3V-3.63V,	-	-	7	
t_{RISE}	Rise time(1)	Load = 5pF, VDD = 3.3V	-	-	15	ns
		Load = 20pF, VDD = 3.3V				
t_{FALL}	Fall time(1)	Load = 5pF, VDD = 3.3V	-	-	15	
		Load = 20pF, VDD = 3.3V				
I_{LEAK}	Input leakage current	Pull-up resistors disabled	-1	+/-0.015	1	µA

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.
2. The I^2C pins have faster fall-time in I^2C Fast Plus mode (Fm+) and High Speed mode (HS). The fall-time can be in 7 ns range in Fm+ mode, and in 5 ns range in HS mode.
3. USB pads PA24, PA25 compliant with USB standard in USB mode.

40.9 Analog Characteristics

40.9.1 Power-On Reset (POR) Characteristics

Table 40-17. POR Characteristics (Device Variant A)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{POT+}	Voltage threshold Level on VDDIN rising	VDD falls at 1V/ms or slower	1.27	1.44	1.62	V
V_{POT-}	Voltage threshold Level on VDDIN falling		0.72	1.07	1.37	V