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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	29.5KB (29.5k x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini57tde

1 GENERAL DESCRIPTION

The NuMicro® Mini57 series 32-bit microcontrollers are embedded with ARM® Cortex®-M0 core for industrial applications which need high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The Mini57 series can run up to 48 MHz and operate at 2.1V ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The Mini57 offers 29.5 Kbytes embedded program Flash, size configurable Data Flash (shared with program Flash), 2 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 4 Kbytes SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the Mini57 to reduce component count, board space and system cost. These useful functions make the Mini57 powerful for a wide range of applications.

Additionally, the Mini57 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.1V to 5.5V
- Memory
  - 29.5 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM)
  - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 22 general-purpose I/O (GPIO) pins and 1 Reset pin for QFN-33 package
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode

- Supports software selectable slew rate control
- GPIO built-in Pull-up/Pull-low resistor for selection

- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous operation modes
  - 24-bit up counter value is readable through CNT (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
  - Timer0, Timer1 and Systick provided with Continuous capture function to capture at most 4 edges continuously on one signal
- Continuous Capture
  - Timer0, Timer1 and Systick have support Continuous capture function can Continuous Capture 4 edge on one signal
- Enhanced Input Capture
  - One unit of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - PWM Trigger
    - ADC Trigger
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Supports a built-in 16-bit PWM clock generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Supports Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control

	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.
22	NC			No Connection
23	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
24	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
25	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
26	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
27	PC.4	I/O	MFP0	General purpose digital I/O pin.
	ECAP_P3	I	MFP7	Enhanced Input Capture input pin
28	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel3 analog input.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.

6.1.2 Features

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

voltage is lower than 0.2 V_{DD} and the state keeps longer than 16.8 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

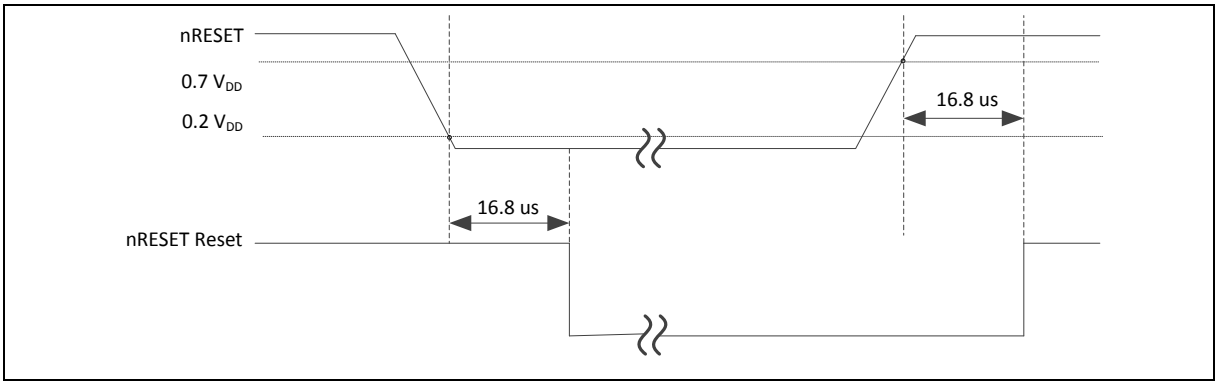


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF (SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF (SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the waveform of Power-On reset.

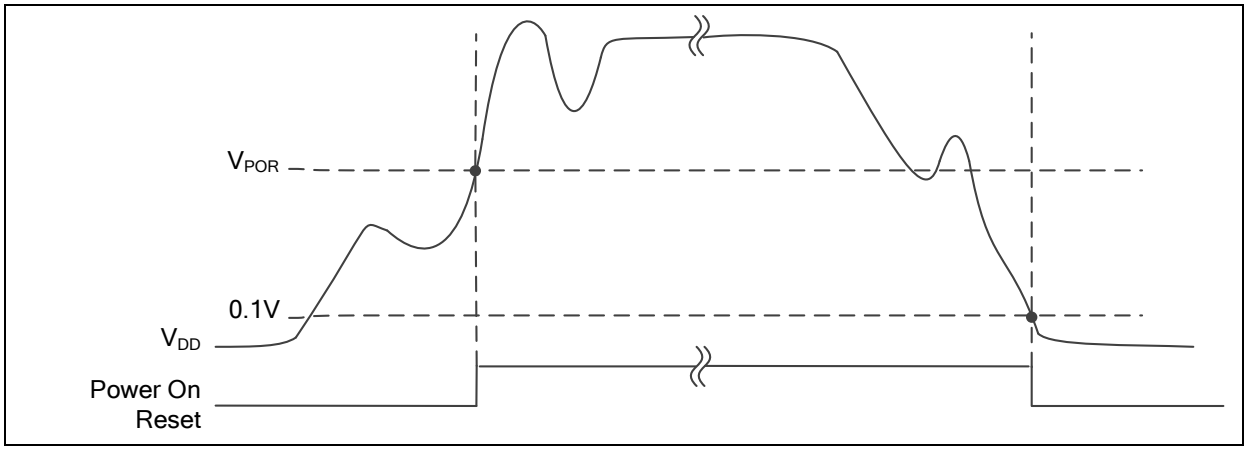


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

Low Voltage Reset detects AV_{DD} during system operation. When the AV_{DD} voltage is lower than

6.2.7.3 SRAM Memory Organization

The Mini57 supports embedded SRAM with total 4 Kbytes size.

- Supports total 4 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

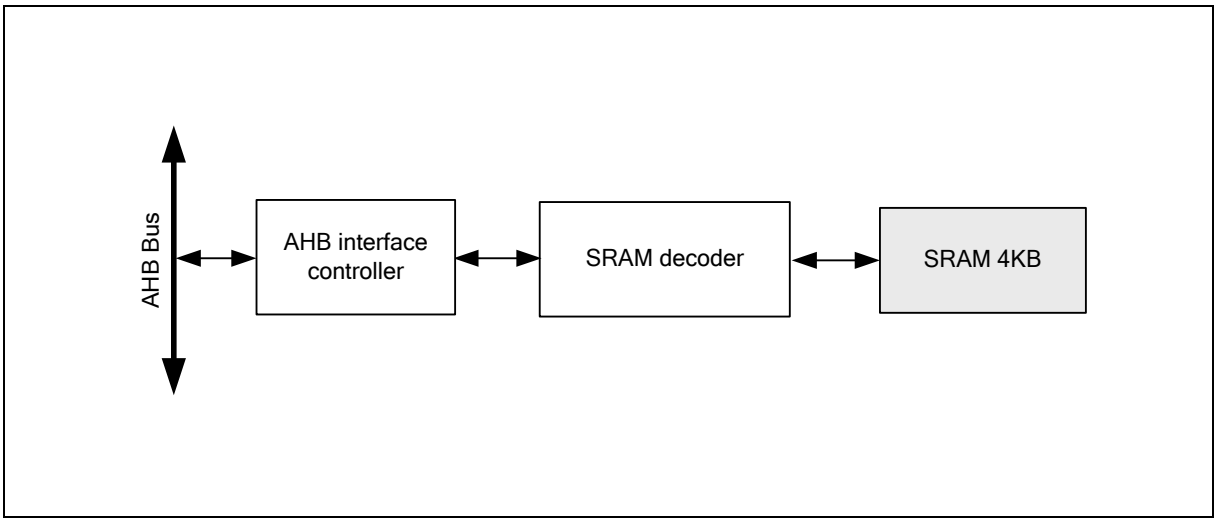


Figure 6.2-9 SRAM Block Diagram

SysTick Current Value Register （SYST_CVR）

Register	Offset	R/W	Description	Reset Value
SYST_CVR	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURRENT							
15	14	13	12	11	10	9	8
CURRENT							
7	6	5	4	3	2	1	0
CURRENT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	**BOD_OUT**	Brown-Out low voltage detected interrupt
17	1	**WDTPINT**	Watchdog Timer interrupt
18	2	**USCI0**	USCI0 interrupt
19	3	**USCI1**	USCI1 interrupt
20	4	**GP_INT**	External interrupt from GPA ~ GPD pins
21	5	**EPWM_INT**	EPWM interrupt
22	6	**BRAKE0_INT**	EPWM brake interrupt from PWM0 or PWM_BRAKE pin
23	7	**BRAKE1_INT**	EPWM brake interrupt from PWM1
24	8	**BPWM0_INT**	BPWM0 interrupt
25	9	**BPWM1_INT**	BPWM1 interrupt
26	10	Reserved	Reserved
27	11	Reserved	Reserved
28	12	Reserved	Reserved
29	13	Reserved	Reserved
30	14	Reserved	Reserved
31	15	**ECAP_INT**	Enhanced Input Capture interrupt
32	16	**CCAP_INT**	Continues Input Capture interrupt
33	17	Reserved	Reserved

34	18	Reserved	Reserved
35	19	Reserved	Reserved
36	20	Reserved	Reserved
37	21	**HIRCTRIM_INT**	HIRC TRIM interrupt
38	22	**TMR0_INT**	Timer 0 interrupt
39	23	**TMR1_INT**	Timer 1 interrupt
40	24	Reserved	Reserved
41	25	Reserved	Reserved
42	26	**ACMP_INT**	Analog Comparator 0 or Comparator 1 interrupt
43	27	Reserved	Reserved
44	28	**PWRWU_INT**	Chip wake-up from Power-down state interrupt
45	29	**ADC0_INT**	ADC0 interrupt
46	30	**ADC1_INT**	ADC1 interrupt
47	31	**ADCWCMP_INT**	ADC Window Compare interrupt

Table 6.2-9 System Interrupt Map Vector Table

6.2.9.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-10 Vector Table Format

6.2.9.5 Operation Description

The NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used

IRQ12 ~ IRQ15 Interrupt Priority Register (NVIC_IPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR3	SCS_BA+0x40C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		Reserved					
23	22	21	20	19	18	17	16
PRI_14		Reserved					
15	14	13	12	11	10	9	8
PRI_13		Reserved					
7	6	5	4	3	2	1	0
PRI_12		Reserved					

Bits	Description	
[31:30]	**PRI_15**	**Priority of IRQ15** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of IRQ14** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_13**	**Priority of IRQ13** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_12**	**Priority of IRQ12** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SCS_SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_15**	**Priority of System Handler 15 – SysTick** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of System Handler 14 – PendSV** "0" denotes the highest priority and "3" denotes the lowest priority.
[21:0]	**Reserved**	Reserved.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when the Cortex®-M0 core executes the WFI instruction only if the PDEN (CLK_PWRCTL[7]) bit set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-2 shows the clock generator and the overview of the clock source control.

The clock generator consists of 4 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

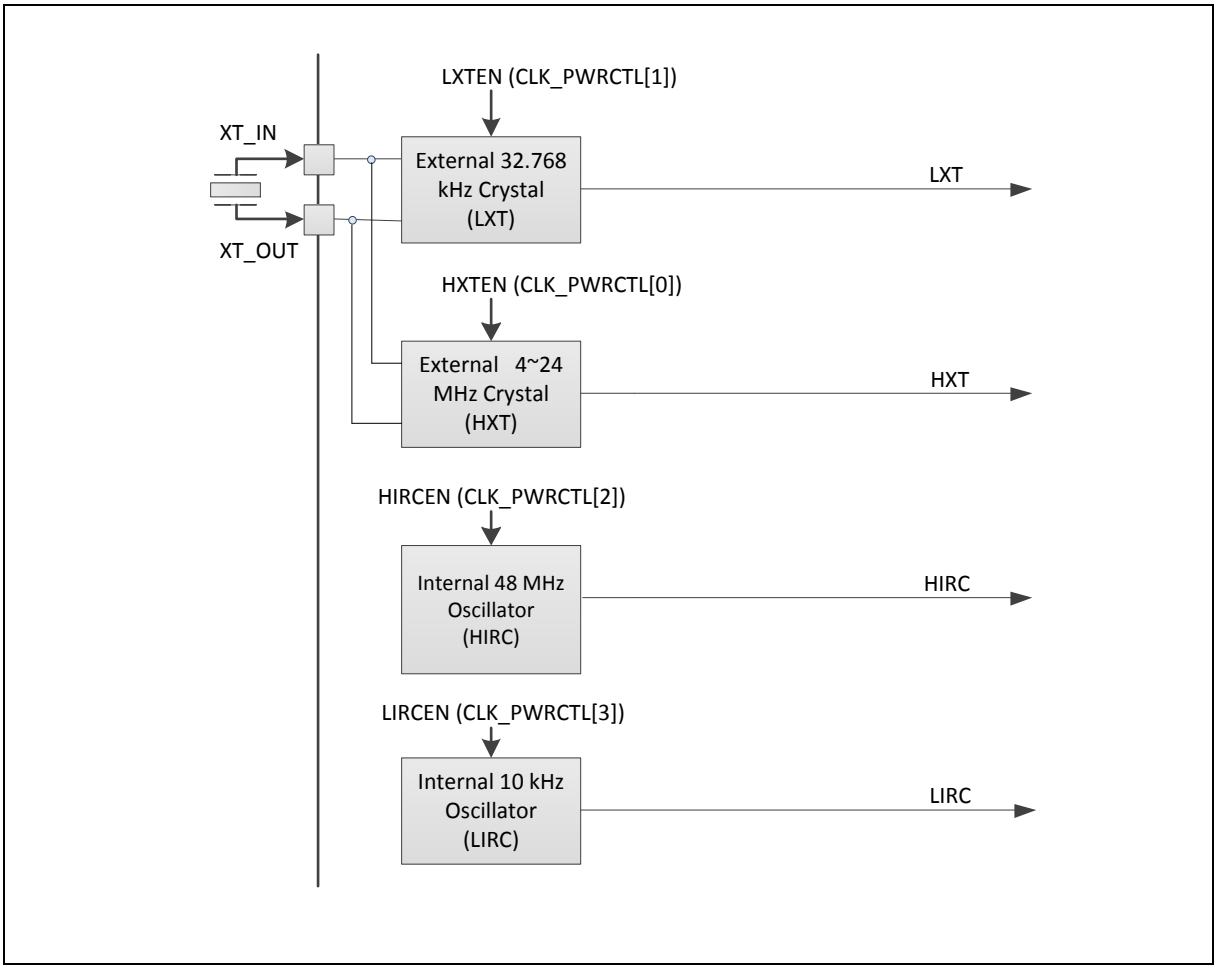


Figure 6.3-1 Clock Generator Block Diagram

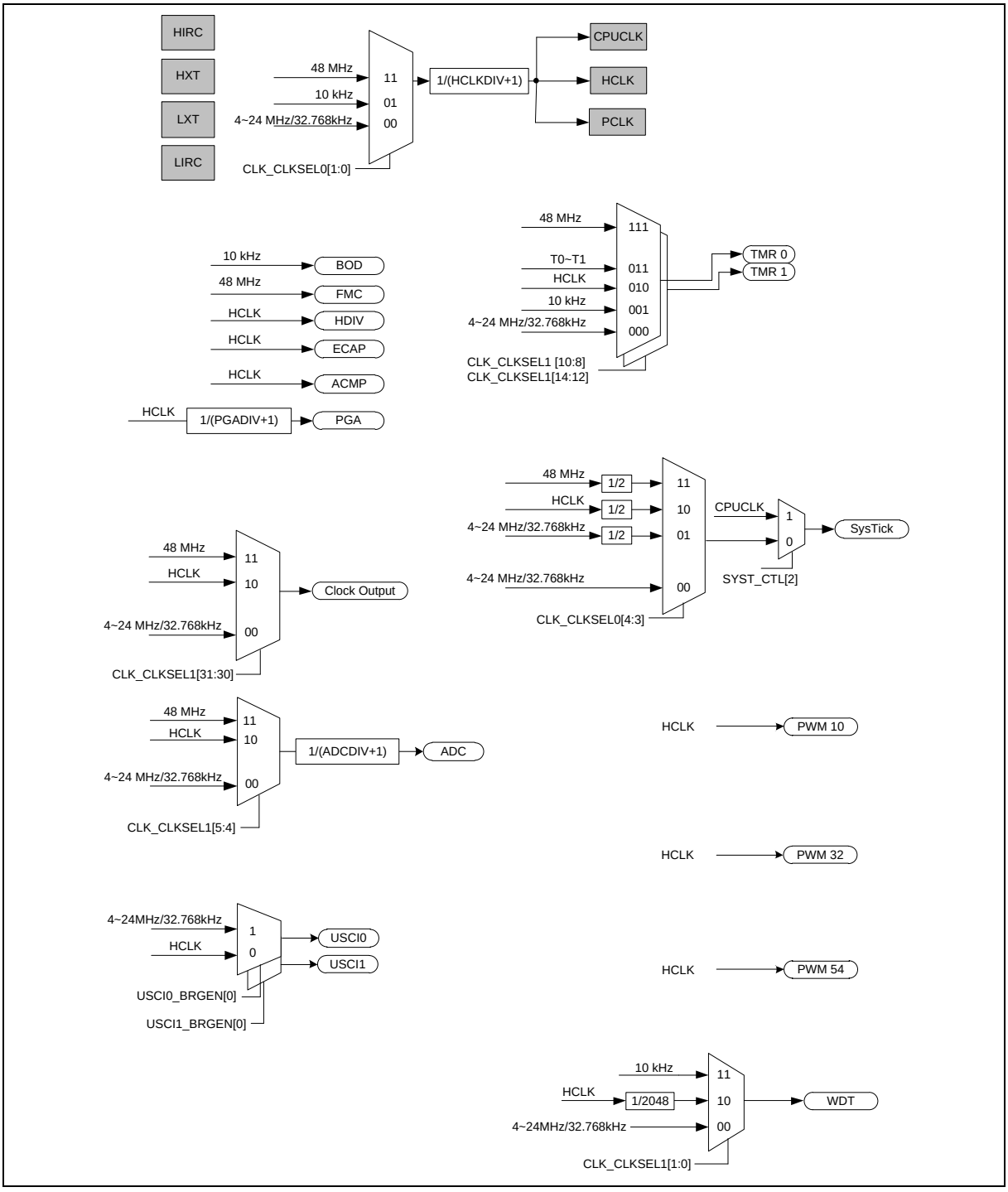


Figure 6.3-2 Clock Generator Global View Diagram

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Supports two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Supports independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Supports four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit CMPDAT)
- Supports maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}); T is the period of timer clock
- 24-bit up counter value is readable through TIMERx_CNT (Timer Data Register)
- Supports event counting function to count the event from external pin (TM0, TM1)
- Supports internal capture triggered while internal ACMP output signal transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.9 Basic PWM Generator (BPWM)

6.9.1 Overview

The Mini57 series has one set of BPWM group supporting one set of PWM generator that can be configured as 2 independent PWM outputs, BPWM CH0~BPWM CH1, or as 1 complementary PWM pairs, (BPWM CH0, BPWM CH1) with programmable Dead-zone generators.

The PWM generator has one 8-bit pre-scalar, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generator provides two independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DTCNT01(BPWM_CTL[4]) is set, BPWM CH0 and BPWM CH1 perform complementary; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0.

To prevent PWM driving output pin from glitches, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with BPWM Counter Register(BPWM_PERIODx, x=0,1) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

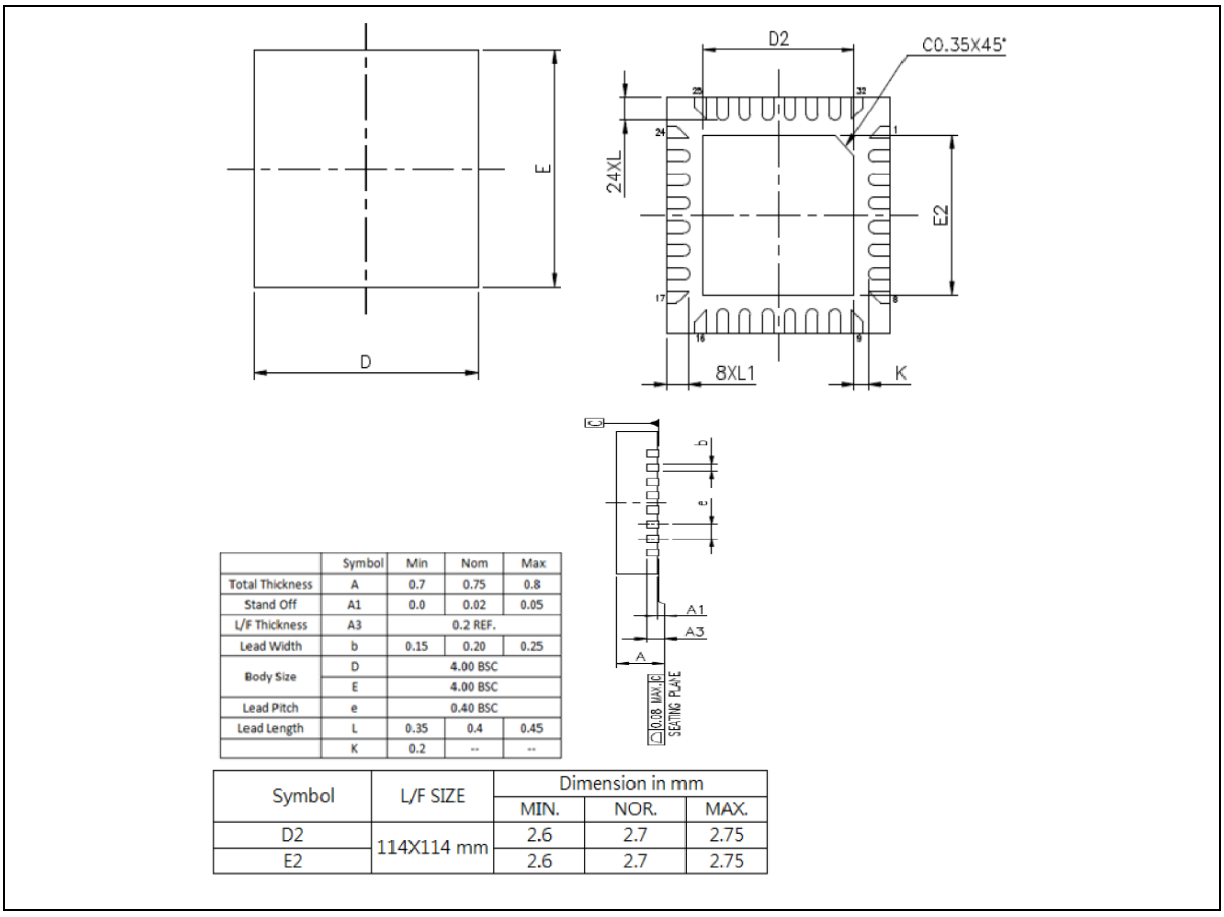
The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

6.9.2 Features

- One PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

I_{IDLE2}		-	1.9	-	mA	5.5V	24 MHz	X	X
I_{IDLE3}		-	2.8	-	mA	3V	24 MHz	X	V
I_{IDLE4}		-	1.9	-	mA	3V	24 MHz	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 16 MHz	-	2.0	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE11}		-	2.0	-	mA	3V	V	X	V
I_{IDLE12}		-	1.4	-	mA	3V	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 12 MHz	-	1.5	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.0	-	mA	5.5V	V	X	X
I_{IDLE11}		-	1.5	-	mA	3V	V	X	V
I_{IDLE12}		-	1.0	-	mA	3V	V	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	0.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE14}		-	0.6	-	mA	5.5V	V	X	X
I_{IDLE15}		-	0.7	-	mA	3V	V	X	V
I_{IDLE16}		-	0.6	-	mA	3V	V	X	X
I_{DD17}	Operating Current Idle Mode HCLK = 32 kHz	-	274.3	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{DD18}		-	273.0	-	µA	5.5V	X	V	X
I_{DD19}		-	265.0	-	µA	3V	X	V	V[1]
I_{DD20}		-	263.9	-	µA	3V	X	V	X
I_{DD17}	Operating Current Idle Mode HCLK = 10 kHz	-	232.6	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]

9.3 33-pin QFN33 (4x4x0.8 mm)



	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.