Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk52dn512zclq10

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK52 and MK52.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K52
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory

Table continues on the next page...

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

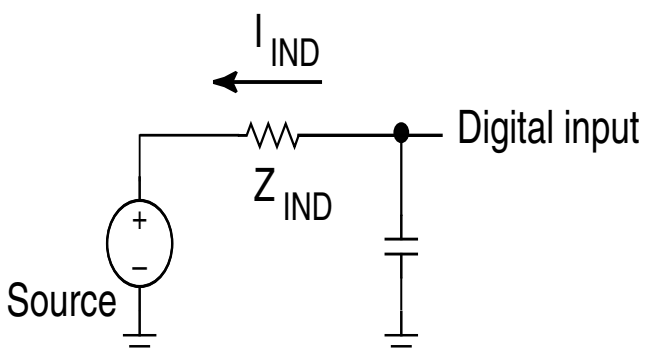
Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	—	V	
	Output high voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	—	—	0.5	V	
	Output low voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• V_{SS} ≤ V_{IN} ≤ V_{DD}					
	— All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	µA	
	— EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	µA	
	— EXTAL32, XTAL32	—	0.075	10	µA	
I_{IND}	Input leakage current, digital pins					4, 5
	• V_{SS} ≤ V_{IN} ≤ V_{IL}					
	— All digital pins	—	0.002	0.5	µA	
	• V_{IN} = V_{DD}					
	— All digital pins except PTD7	—	0.002	0.5	µA	
	— PTD7	—	0.004	1	µA	
I_{IND}	Input leakage current, digital pins					4, 5, 6
	• V_{IL} < V_{IN} < V_{DD}					
	— V_{DD} = 3.6 V	—	18	26	µA	
	— V_{DD} = 3.0 V	—	12	49	µA	
	— V_{DD} = 2.5 V	—	8	13	µA	
	— V_{DD} = 1.7 V	—	3	6	µA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	—	1	50	μA	4, 5
Z_{IND}	Input impedance examples, digital pins					4, 7
	• $V_{DD} = 3.6$ V	—	—	48	kΩ	
	• $V_{DD} = 3.0$ V	—	—	55	kΩ	
	• $V_{DD} = 2.5$ V	—	—	57	kΩ	
	• $V_{DD} = 1.7$ V	—	—	85	kΩ	
R_{PU}	Internal pullup resistors	20	35	50	kΩ	8
R_{PD}	Internal pulldown resistors	20	35	50	kΩ	9

1. Typical values characterized at 25°C and VDD = 3.6 V unless otherwise noted.
2. Open drain outputs must be pulled to V_{DD}.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
5. Internal pull-up/pull-down resistors disabled.
6. Characterized, not tested in production.
7. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
8. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
9. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}



5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	• @ –40 to 25°C	—	0.71	0.81	µA	
	• @ 70°C	—	1.01	1.3	µA	
	• @ 105°C	—	2.82	4.3	µA	
	• @ 3.0V					
	• @ –40 to 25°C	—	0.84	0.94	µA	
	• @ 70°C	—	1.17	1.5	µA	
	• @ 105°C	—	3.16	4.6	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	85	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

Table 14. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

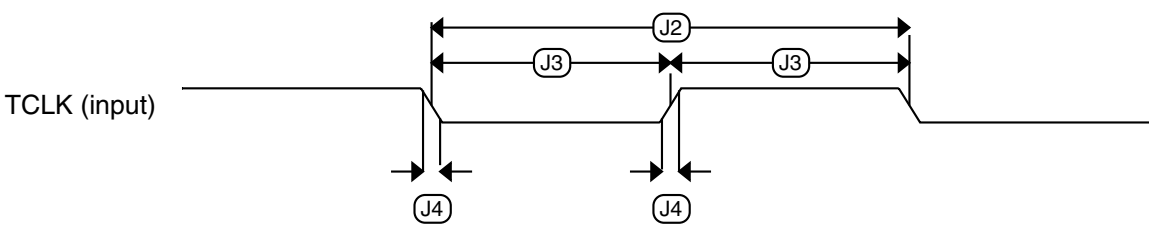


Figure 5. Test clock input timing

Table 17. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr16b128k}$	• 128 KB EEPROM backup	—	650	2400	µs	
$t_{eewr16b256k}$	• 256 KB EEPROM backup	—	1000	3200	µs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	
$t_{eewr32b128k}$	• 128 KB EEPROM backup	—	1200	2675	µs	
$t_{eewr32b256k}$	• 256 KB EEPROM backup	—	1900	3500	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

Table 24. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

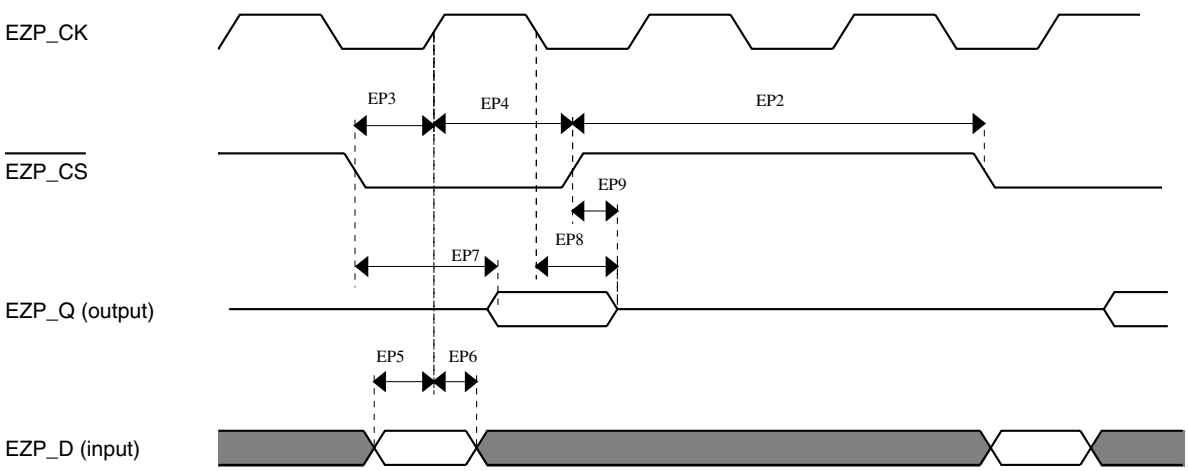


Figure 10. EzPort Timing Diagram

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 27 and Table 28 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 29 and Table 30.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} - V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} - V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

Table continues on the next page...

6.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

6.8.3 USB DCD electrical specifications

Table 45. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.4 USB VREG electrical specifications

Table 46. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.27	30	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

Table 49. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

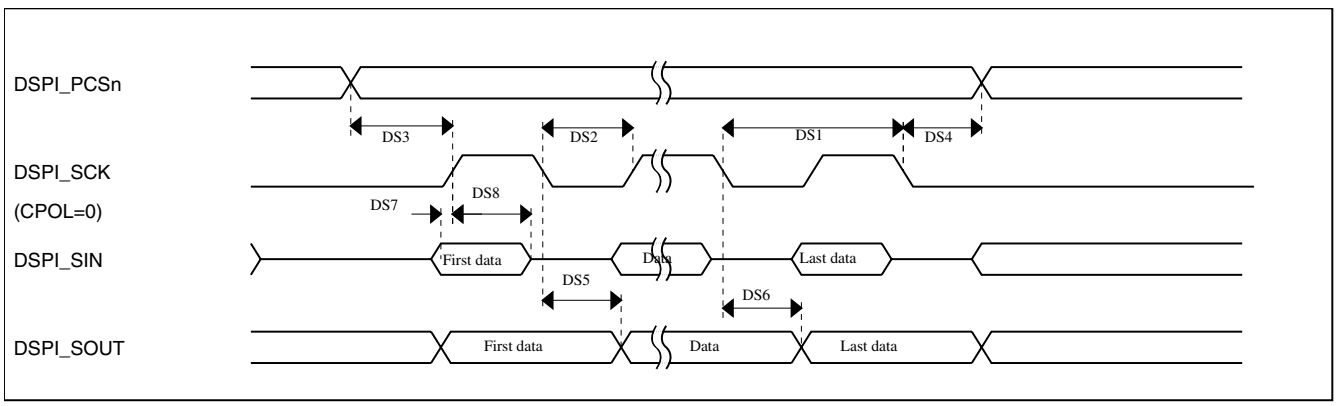


Figure 24. DSPI classic SPI timing — master mode

Table 50. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

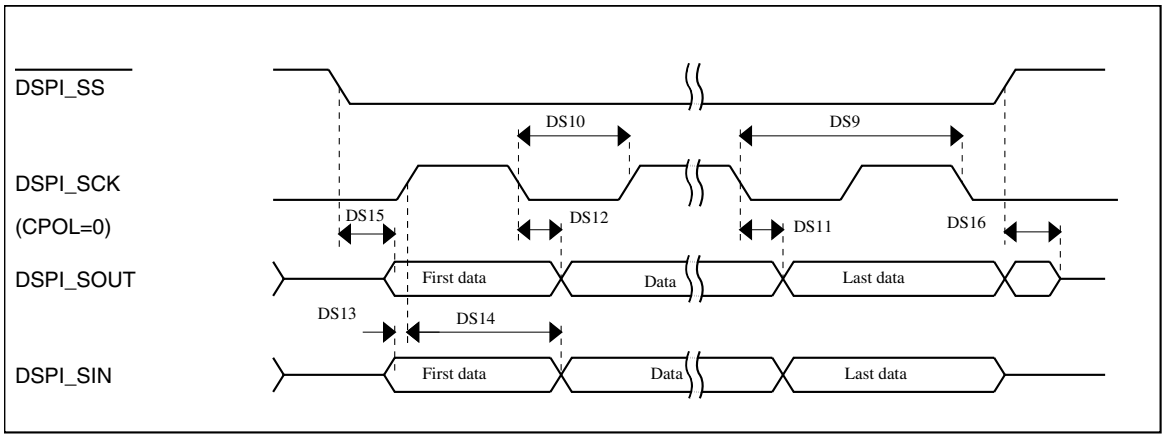


Figure 25. DSPI classic SPI timing — slave mode

6.8.7 Inter-Integrated Circuit Interface (I^2C) timing

Table 51. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

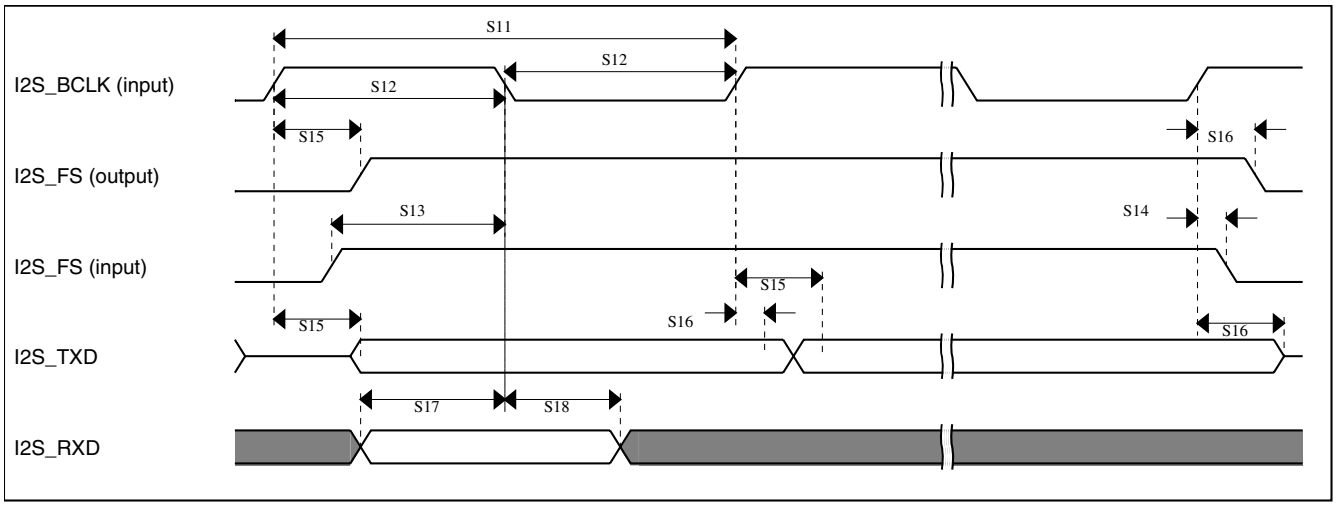


Figure 29. I²S timing — slave modes

Table 55. I²S master mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	2 x t_{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t_{SYS}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-4.3	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-4.6	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	23.9	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Table 56. I²S slave mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t_{SYS}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3.5	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	28.6	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

8 Pinout

8.1 K52 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	C10	NC	NC	NC								
—	B10	NC	NC	NC								
—	A10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
2	D2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
3	D1	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK				
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD				
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
35	K3	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2								
36	J3	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
38	L3	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2								
39	L4	TRI0_DM	TRI0_DM	TRI0_DM								
40	M4	TRI0_DP	TRI0_DP	TRI0_DP								
41	L5	TRI1_DM	TRI1_DM	TRI1_DM								
42	M5	TRI1_DP	TRI1_DP	TRI1_DP								
43	K5	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22								
44	K4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4								
45	J4	DAC1_OUT/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC1_OUT/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC1_OUT/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5								
46	M7	XTAL32	XTAL32	XTAL32								
47	M6	EXTAL32	EXTAL32	EXTAL32								
48	L6	VBAT	VBAT	VBAT								
49	H4	PTE28	DISABLED		PTE28							
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	

Table 58. Revision History (continued)

Rev. No.	Date	Substantial Changes
3	3/2011	Added sections that were inadvertently removed in previous revision
4	3/2011	Reworded I_{IC} footnote in "Voltage and Current Operating Requirements" table. Added paragraph to "Peripheral operating requirements and behaviors" section. Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.
5	6/2011	• Changed supported part numbers per new part number scheme • Changed *DC injection current* specs in "Voltage and current operating requirements" table • Changed *Input leakage current* and *internal pullup/pulldown resistor* specs in "Voltage and current operating behaviors" table • Split *Low power stop mode current* specs by temperature range in "Power consumption operating behaviors" table • Changed typical I_{DD_VBAT} spec in "Power consumption operating behaviors" table • Added ENET and LPTMR clock specs to "Device clock specifications" table • Changed *Minimum external reset pulse width* in "General switching specifications" table • Changed *PLL operating current* in "MCG specifications" table • Added footnote to *PLL period jitter* in "MCG specifications" table • Changed *Supply current* in "Oscillator DC electrical specifications" table • Changed *Crystal startup time* in "Oscillator frequency specifications" table • Changed *Operating voltage* in "EzPort switching specifications" table • Changed title of "FlexBus switching specifications" table and added Output valid and hold specs • Added "FlexBus full range switching specifications" table • Changed *ADC asynchronous clock source* specs in "16-bit ADC characteristics" table • Changed *Gain* spec in "16-bit ADC with PGA characteristics" table • Added typical *Input DC current* to "16-bit ADC with PGA characteristics" table • Changed *Input offset voltage* and *ENOB* notes field in "16-bit ADC with PGA characteristics" table • Changed *Analog comparator initialization delay* in "Comparator and 6-bit DAC electrical specifications" • Changed *Code-to-code settling time*, *DAC output voltage range low*, and *Temperature coefficient offset voltage* in "12-bit DAC operating behaviors" table • Moved *Output resistance* to "TRIAMP operating behaviors" tables • Changed *Supply current*, *Input offset current*, *AC input impedance* in "TRIAMP operating behaviors" tables • Changed *Temperature drift* and *Load regulation* in "VREF full-range operating behaviors" table • Changed *Regulator output voltage* in "USB VREG electrical specifications" table • Changed I_{LIM} description and specs in "USB VREG electrical specifications" table • Changed *DSPI_SCK cycle time* specs in "DSPI timing" tables • Changed $\overline{\text{DSPI\_SS}}$ specs in "Slave mode DSPI timing (low-speed mode)" table • Changed *DSPI_SCK to DSPI_SOUT valid* spec in "Slave mode DSPI timing (high-speed mode)" table • Changed *Reference oscillator current source base current* spec and added *Low-power current adder* footer in "TSI electrical specifications" table

Table continues on the next page...

Table 58. Revision History (continued)

Rev. No.	Date	Substantial Changes
6	01/2012	• Added AC electrical specifications. • Replaced TBDs with silicon data throughout. • In "Power mode transition operating behaviors" table, removed entry times. • Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. • Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". • Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. • Updated I_{DD_RUN} numbers in 'Power consumption operating behaviors' section. • Clarified 'Diagram: Typical IDD_RUN operating behavior' section and updated 'Run mode supply current vs. core frequency — all peripheral clocks disabled' figure. • In 'Voltage reference electrical specifications' section, updated C_L, V_{tdrift}, and V_{vdrift} values. • In 'USB electrical specifications' section, updated V_{DP_SRC}, I_{DDstby}, and '$V_{Reg33out}$ values.
7	02/2013	• In "ESD handling ratings", added a note for I_{LAT}. • Updated "Voltage and current operating requirements". • Updated "Voltage and current operating behaviors". • Updated "Power mode transition operating behaviors". • Updated "EMC radiated emissions operating behaviors" to add MAPBGA data. • In "MCG specifications", updated the description of f_{ints_t}. • In "16-bit ADC operating conditions", updated the max spec of V_{ADIN}. • In "16-bit ADC electrical characteristics", updated the temp sensor slope and voltage specs. • Updated "I2C switching specifications". • In "SDHC specifications", removed the operating voltage limits and updated the SD1 and SD6 specs. • In "I2S switching specifications", added separate specification tables for the full operating voltage range.