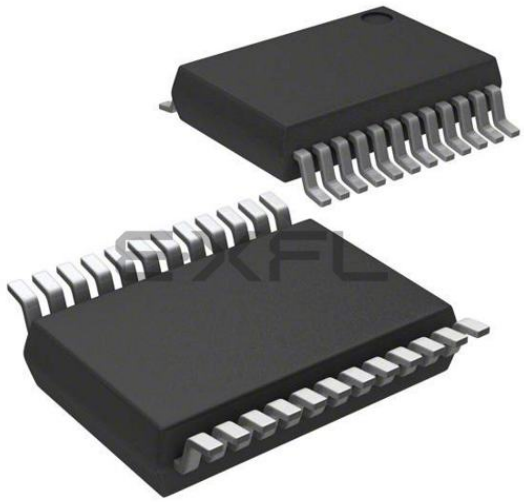

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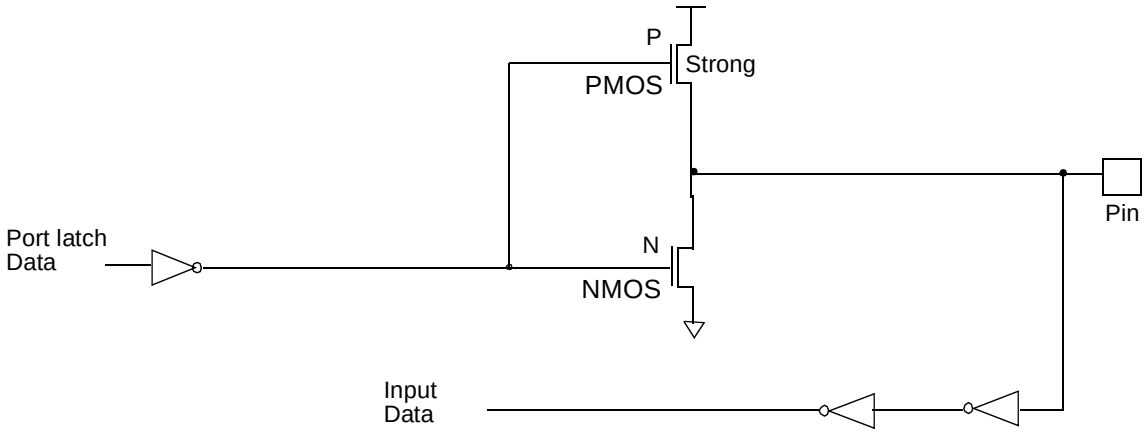
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

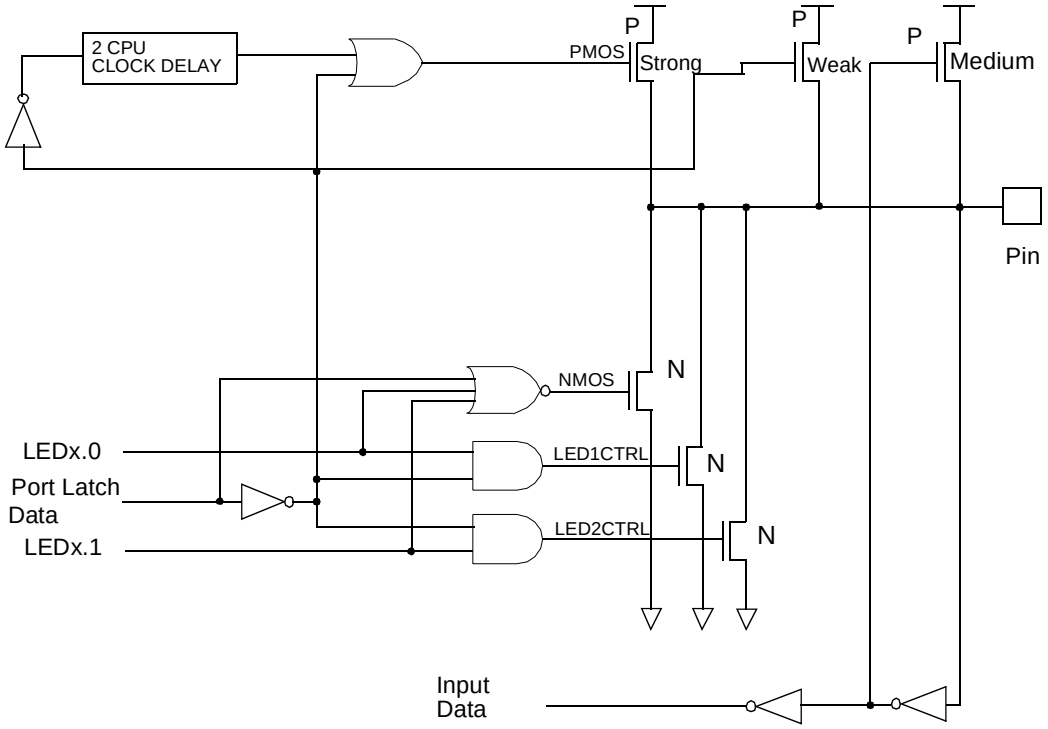
Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	16MHz
Connectivity	SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	Flash RAM
EEPROM Size	16K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 5.4V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.209", 5.30mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5121-icsul

Figure 6. Push-pull Output Configuration



LED Output Configuration The input only configuration is shown in Figure 7.

Figure 7. LED Source Current Configuration



Note: The port can be configured in quasi bi-directional mode and the level of current can be programmed by means of LEDCON0 and LEDCON1 registers before switching the led on by writing a logical 0 in Port latch.

Table 2. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000	LEDCON XXXX 0000							F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000	RCON XXXX OXXX							D7h
C8h									CFh
C0h									C7h
B8h	IPL0 XXX0 0000	SADEN 0000 0000	ISEL 0000 0100					DCCKPS XXXX XX11	BFh
B0h	P3 1111 1111	IE1 XXXX 0XXX	IPL1 XXXX 0XXX	IPH1 XXXX 0XXX	0 SCWT0 * 1000 0000	0 SCWT1 * 0010 0101	0 SCWT2 * 0000 0000	IPH0 XXX0 0000	B7h
					1 SCGT0 * 0000 1100	1 SCGT1* 0000 0000	1 SCICR * 0000 0000		
A8h	IE0 0XX0 0000	SADDR 0000 0000	SCTBUF* 0000 0000	SCSR XXX0 1000	0 SCCON * 0X000	0 SCISR* 10X0 0000	0 SCIIR* 0X00 0000	CKCON1 XXXX 0XXX	AFh
			SCRBUF 0000 000		1 SCETU0 0111 0100	1 SCETU1 0XXX	1 SCIER * 0X00 0000		
A0h	P2 1111 1111		AUXR1 XXX XXX0				WDTRST XXXX XXXX	WDTPRG XXXX X0000	A7h
98h	SCON XXX0 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000					9Fh
90h	P1 XX11 1111	SIOCON 00XX 0000						CKRL XXXX 111X	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 00XX XX00	CKCON0 X0X0 X000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000	20			PCON 00XX XX00	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

SCRS Bit (SCSR.0)	(*)
0	SFR value
1	SFR value

The ports status under Power-down is the status which was valid before entering this mode.

The INT1 interrupt is a multiplexed input (see Interrupt paragraph) with CPRES (Card detection) and Rxd (UART Rx). So these three inputs can be used to exit from Power-down mode. The configurations which must be set are detailed below:

Rxd input:

RXEN (ISEL.0) must be set

EX1 (IE0.2) must be set

A low level detected during more than 100 microseconds exit from Power-down

CPRES input:

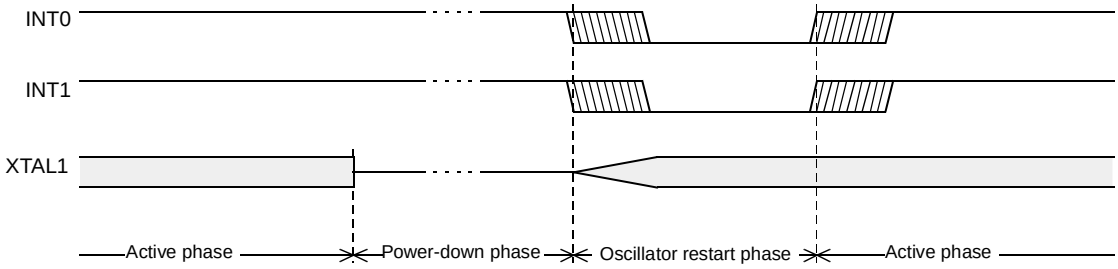
PRSEN (ISEL.1) must be set

EX1 (IEO.2) must be set

EA (IE0.7) must be set

In the INT1 interrupt vector, the CPLEV Bit (ISEL.7) must be inverted and PRESIT Bit (ISEL.5) must be reset.

Figure 10. Power-down Exit Waveform



Exiting from Power-down by reset redefines all the SFRs, exiting from Power-down by external interrupt does no affect the SFRs.

Exiting from Power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with Power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

SCI Control

Prior to entering Power-down mode, a de-activation of the Smart Card system must be performed.

LED Control

Prior to entering Power-down mode, if the LED mode output is used, the medium pull-up must be disconnected by setting the LEDPD bit in the PCON Register (PCON 3).

Low Power Mode

Only in Power-down mode, in order to reduce the power consumption, the user can choose to select this low-power mode.

The activation reference is the following.

First select the Low-power mode by setting the LP bit in the AUXR Register (AUXR. 6)

The activation of Power-down can then be done.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated.

Only in case of PLCC52 version, in order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0 (See Table 4). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Power Modes Control Registers

Table 3. PCON Register

PCON (S:87h)
Power Configuration Register

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	-	LEDPD	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	Double Baud Rate bit Set to double the Baud Rate when Timer 1 is used and mode 1, 2 or 3 is selected in SCON register.
6	SMOD0	SCON Select bit When cleared, read/write accesses to SCON.7 are to SM0 bit and read/write accesses to SCON.6 are to SM1 bit. When set, read/write accesses to SCON.7 are to FE bit and read/write accesses to SCON.6 are to OVR bit. SCON is Serial Port Control register.
5		Reserved
4		Reserved
3	LEDPD	LED Control Power-Down Mode bits When cleaned the I/O pull-up is the standard C51 pull-up control. When set the medium pull-up is disconnected.
2	GF0	General-purpose flag 0 One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
1	PD	Power-down Mode bit Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	Idle Mode bit Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value = X0XX XX00b

Table 5. IE0 Register

IE0
Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	-	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable Timer 0 overflow interrupt. Set to enable Timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b

the different counters. One of the most important counters is the guard time counter that gives time slots corresponding to the character frame.

It is enabled only in UART mode.

The transition from the receipt mode to the transmit mode is done automatically. Priority is given to the transmission.

ETU Counter

The ETU (Elementary Timing Unit) counter controls the working frequency of the barrel shifter, in fact, it generates the enable signal of the barrel shifter.

It is 11 bits wide and there is a special compensation mode activated with the most significant bit that allows non integer ETU value with a working clock equal to the card clock .

But the decimal value is limited to a half clock cycle. In fact the bit duration is not fixed. It takes turns in n clock cycles and n-1 clock cycles. The character duration (10 bits) is also equal to 10*(n+1/2) clock cycles.

This allows to reach the required precision of the character duration specified by the ISO7816 standard.

example: F = 372 D = 32 = > ETU = 11.625 clock cycles.

ETU = (ETU[10-0] -0.5 * COMP)*f with ETU[10-0] = 12, COMP = 1 (bit 7 of SCETU1)

To achieve this clock rate we activated the compensation mode and we programmed the ETU duration to 12 clock cycles.

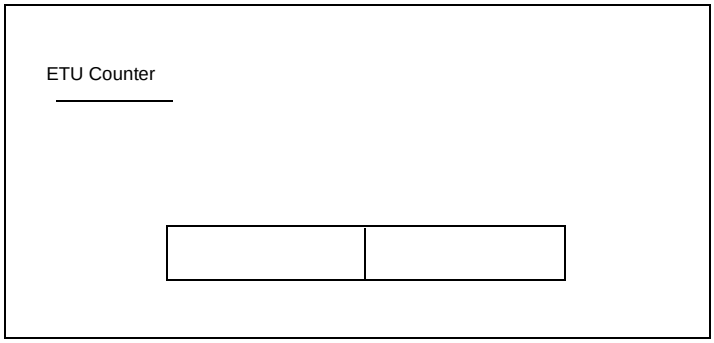
The result will be a full character duration (10 bits) equal to 11.5 clock cycles.

Guard Time Counter

The minimum time between the leading edge of the start bit of a character and the leading edge of the start bit of the following character transmitted (Guard time) is controlled by one counter.

It is 9 bits wide and is incremented at the ETU rate.

Figure 15. Guard Time Counter



Waiting Time Counter (WT)

The WT counter is a 24 bits down counter which can be loaded with the value contained in the SCWT2, SCWT1, SCWT0 registers. Its main purpose is time out signal generation. It is 24 bits wide and is decremented at the ETU rate. The ETU counter acts as a prescaler (See Figure 16).

When the WT counter timeout, an interrupt is generated and the SCIB function is locked: reception and emission are disabled. It can be enabled by resetting the macro or reloading the counter.

Figure 16. Waiting Time Counter

The counter is loaded, if WTEN = 0, during the write of SCWT2 register.

This counter is available in both UART and manual modes. But the behaviour depends

Table 16. SCCON Register

SCCON (S:ACh, SCRS = 0)
Smart Card Contacts Register

7	6	5	4	3	2	1	0
CLK	-	CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC

Bit Number	Bit Mnemonic	Description
7	CLK	Card Clock Selection Clear this bit to use the CardClk bit (CARDCLK) to drive Card CLK pin. Set this bit to use XTAL signal to drive the Card CLK pin. Note: internal synchronization avoids any glitch on the CLK pin when switching this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CARDC8	Card C8 Clear this bit to drive a low level on the Card C8 pin. Set this bit to set a high level on the Card C8 pin.
4	CARDC4	Card C4 Clear this bit to drive a low level on the Card C4 pin. Set this bit to set a high level on the Card C4 pin.
3	CARDIO	Card I/O When the UART bit is cleared in SCICR Register, the value of this bit is driven to the Card I/O pin. Then this pin can be used as a pseudo bi-directional I/O when this bit is set. To be used as an input, this bit must contain a 1.
2	CARDCLK	Card CLK When the CLK bit is cleared in SCCON Register, the value of this bit is driven to the Card CLK pin.
1	CARDRST	Card RST Clear this bit to drive a low level on the Card RST pin. Set this bit to set a high level on the Card RST pin. Read is not allowed if VCARDOK=0
0	$CARDV_{CC}$	Card VCC Control Clear this bit to desactivate the Card interface and set its power-off. The other bits of SCC register have no effect while this bit is cleared. Set this bit to power-on the Card interface. The activation sequence shall be handled by software.

Reset Value = 0X00 0000b

Table 24. SCETU0 Register

SCETU0 (S:ACh, SCRS = 1)
Smart Card ETU Register 0

7	6	5	4	3	2	1	0
ETU7	ETU6	ETU5	ETU4	ETU3	ETU2	ETU1	ETU0

Bit Number	Bit Mnemonic	Description
7-0	ETU[7:0]	ETU LSB The Elementary Time Unit is (ETU[10:0] - 0.5*COMP)/f, where f is the Card CLK frequency. According to ISO7816, ETU[10:0] can be set between 11 and 2047. The default reset value of ETU[10:0] is 372 (F = 372, D = 1).

Reset Value = 0111 0100b

Table 25. SCGT1 Register

SCGT1 (S:B5h, SCRS = 1)
Smart Card Transmit Guard Time Register 1

7	6	5	4	3	2	1	0
							GT8

Bit Number	Bit Mnemonic	Description
7-1		Reserved The value read from these bits is indeterminate. Do not change these bits .
0	GT8	Transmit Guard Time MSB Used together with the Transmit Guard Time LSB (see SCGT0 Register).

Reset Value = XXXX XXX0b

Table 26. SCGT0 Register

SCGT0 (S:B4h, SCRS = 1)
Smart Card Transmit Guard Time Register 0

7	6	5	4	3	2	1	0
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

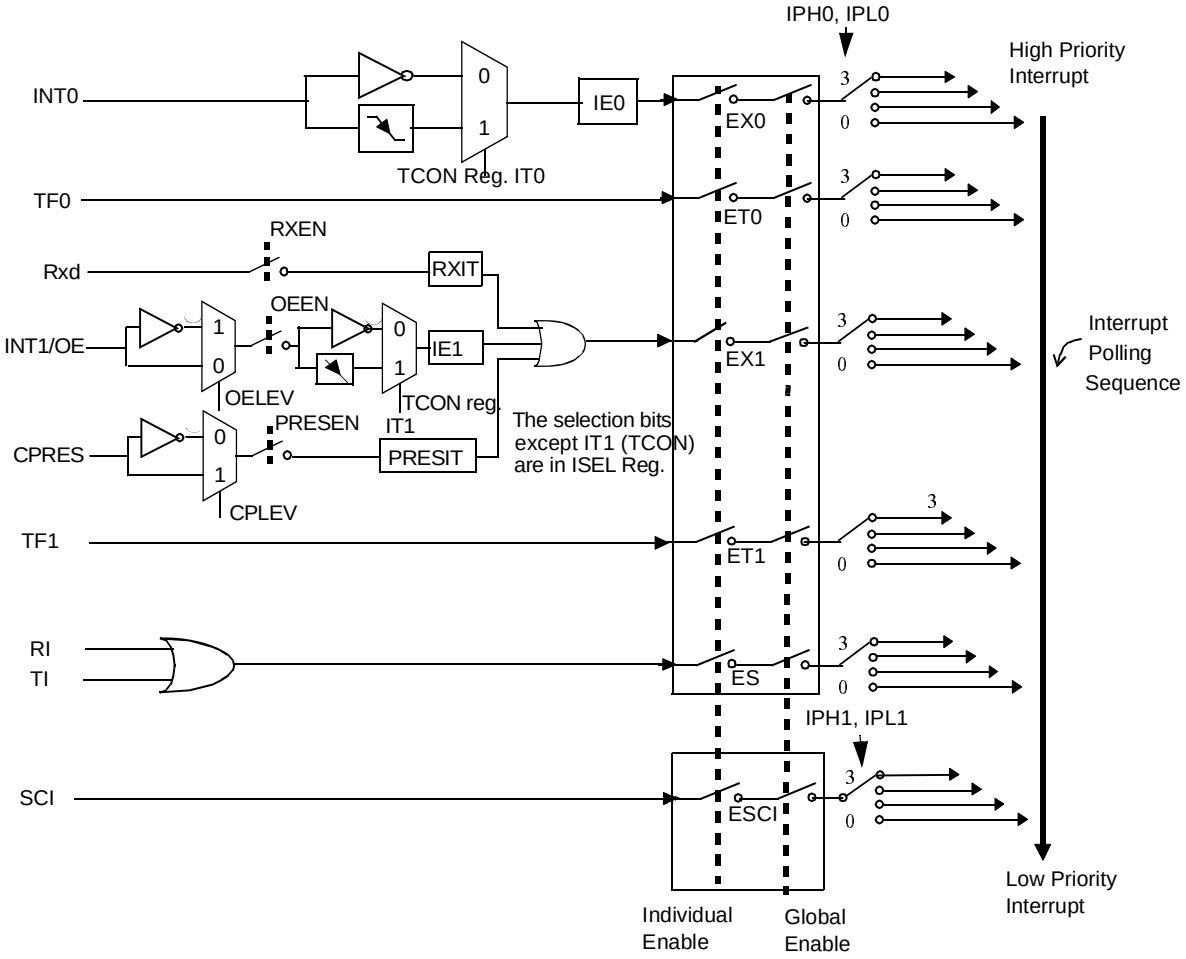
Bit Number	Bit Mnemonic	Description
7-0	GT[7:0]	Transmit Guard Time LSB The minimum time between two consecutive start bits in transmit mode is GT[8:0] * ETU. According to ISO 7816, GT can be set between 11 and 266 (11 to 254+12 ETU).

Reset Value = 0000 1100b

Interrupt System

The T8xC5121 has a total of 6 interrupt vectors: four external interrupts ($\overline{INT0}$, $\overline{INT1}$/OE, CPRES, RxD), two Timer 0 interrupts (Timer 0s 0 and 1), serial port interrupt and Smart Card Interface interrupt. These interrupts are shown in Figure 23.

Figure 23. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (see Figure 32). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority register (see Figure 36) and in the Interrupt Priority High register (see Figure 38). Table 30 shows the bit values and priority levels associated with each combination.

Table 30. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

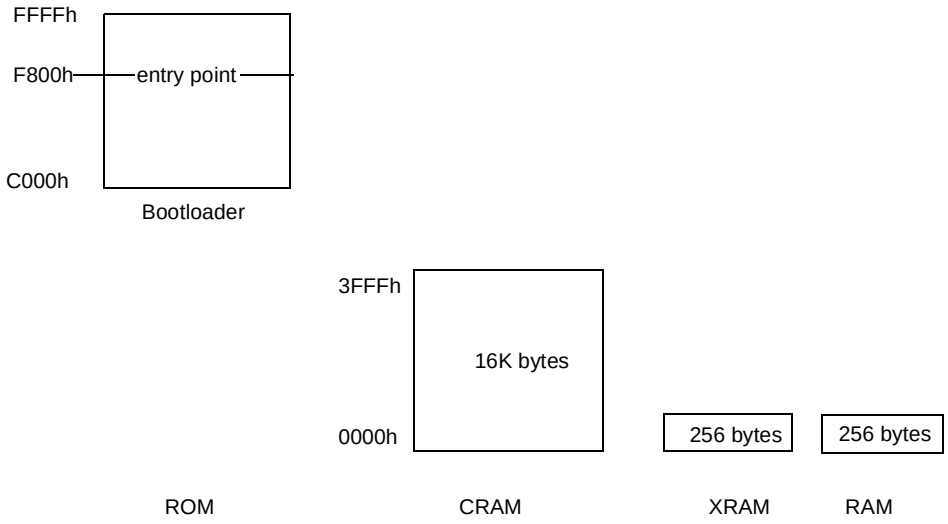
Table 33. IE1 Register

7	6	5	4	3	2	1	0
-	-	-	-	ESCI	-	-	-

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	ESCI	SCI Interrupt Enable Clear to disable the SCI interrupt. Set to enable the SCI interrupt.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	-	Reserved The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 0XXXb

Figure 25. CRAM and ROM Mappings



T83C5121 with Mask ROM Version

In this version, the customer program is masked in 16 Kbytes ROM.

The customer program is masked in ROM during the final production phase. The ROM size will be determined at mask generation process depending of the program size.

In-System Programming

The In-System Programming (ISP) mode is only implemented in the following product versions:

EEPROM version

CRAM version

(The ROM product version is masked with the customer program and does not need ISP mode)

The ISP is used to download an Application program in the device and to run it.

The communication protocols which are implemented are: UART and TWI.

Hardware Interface

The hardware in relation with the two communication protocols is detailed below:

TWI protocol

Serial protocol

Figure 31. Timer 0/Counter 0 in Mode 3: Two 8-bit Counters

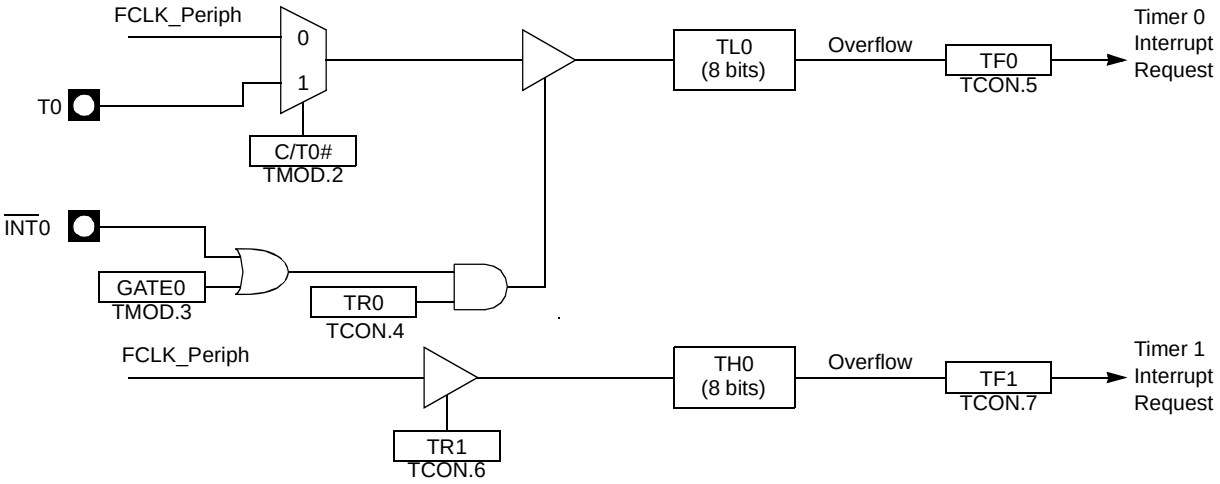


Figure 34. UART Timings in Mode 1

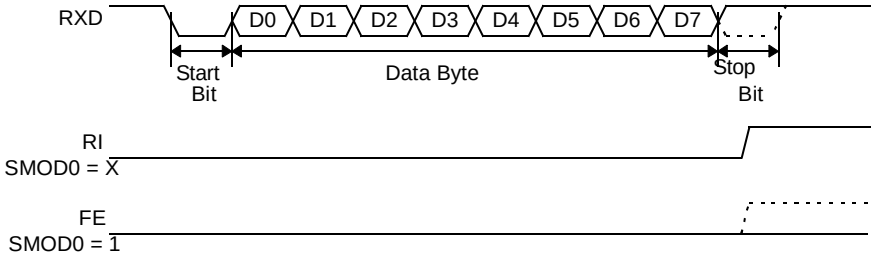
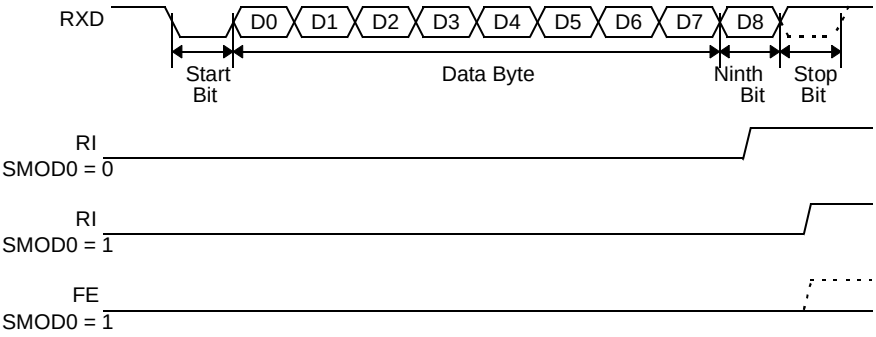


Figure 35. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device s address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e., setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don t care bits (defined by zeros) to form the device s given address. The don t care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias .....-25°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS}.....-0.5V to + 6.0V
Voltage on Any Pin to V_{SS}..... -0.5V to V_{CC} + 0.5V

Note: Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.85V to 5.4V; F = 7.36 to 16 MHz

Table 72. Core DC Parameters (XTAL, $\overline{RST}$, P0, P2, ALE, $\overline{PSEN}$, $\overline{EA}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, $\overline{RST}$	.2 V_{CC} + .9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, Port 0 and 2			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage, Port 0 and 2	0.9 x V_{CC}			V	I_{OH} = -40 µA
DI_{CC}	Digital Supply Output Current		6	10	mA	C_L = 100 nF
DV_{CC}	Digital Supply Voltage	2.5	2 .9	3.0	V	C_L = 100 nF DIcc=10mA
Icc	Normal Power Down mode		80	100	µA	25°C
Icc	Pulsed Power Down mode		20	30	µA	50°C Vcc=3V
Iccop	Power Supply current	I_{ccop} = 0.25 Freq (MHz) +4 mA I_{ccIDLE} = 0.03 Freq (MHz) +5 mA				V_{CC} = 5.4V and Bootloader execution
V_{PFDP}	Power-fail high level threshold		2 .55		V	
V_{PFDM}	Power-fail low level threshold		2 .45		V	
t_G	Power Fail glitch time			50	ns	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 µs		600	sec.	