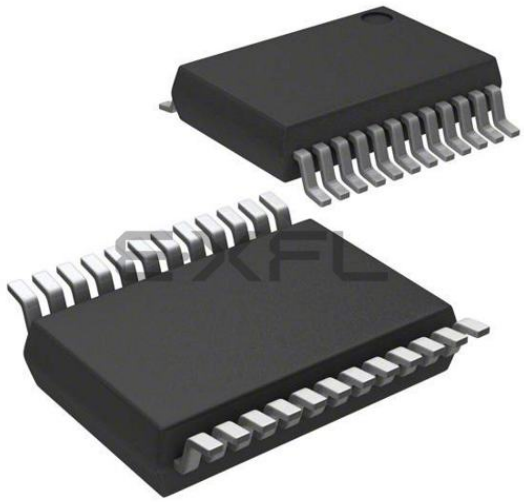

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	16MHz
Connectivity	SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	Flash RAM
EEPROM Size	16K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 5.4V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.209", 5.30mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5121-ysul

Description

T8xC5121 is a high performance CMOS ROM/CRAM derivative of the 80C51 CMOS single chip 8-bit microcontrollers.

T8xC5121 retains the features of the Atmel 80C51 with extended ROM capacity (16 Kbytes), 512 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) with baud rate generator (BRG) and an on-chip oscillator.

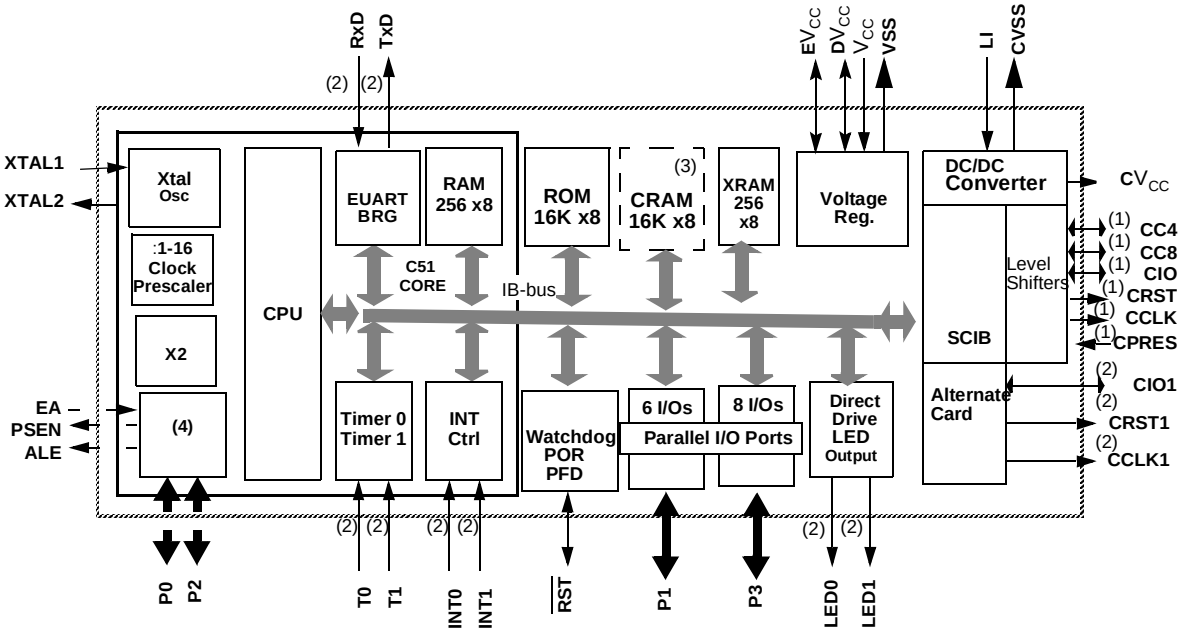
In addition, the T8xC5121 have, a Multi protocol Smart Card Interface, a dual data pointer, 2 programmable LED current sources (2-4-10 mA) and a hardware Watchdog.

T89C5121 Flash RAM version and T85C5121 Code RAM version can be loaded by In-System Programming (ISP) software residing in the on-chip ROM from a low-cost external serial EEPROM or from R232 interface.

T8xC5121 have 2 software-selectable modes of reduced activity for further reduction in power consumption.

Block Diagram

Figure 1. Block Diagram



Notes:
1. Alternate function of Port 1
2. Alternate function of Port 3
3. Only for the Code RAM version
4. Only for PLCC52

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P3.0	RxD		EV_{CC}		I	**UART function** Receive data input
					I/O	**Input/Output function** P3.0 is a bi-directional I/O port with internal pull-ups.
					I	**Reset configuration** Input (high level)
P3.1	TxD		EV_{CC}		O	**UART function** Transmit data output OE active at low or high level depending of PMSOEN bits in SIOCON Reg.
					I/O	**Input/Output function** P3.1 is a bi-directional I/O port with internal pull-ups.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.2	INT0		DV_{CC}		I	**External interrupt 0** $\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$.
					I/O	**Input/Output function** P3.2 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0: Gate input** INT0 serves as external run control for Timer 0 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.3	INT1	OE	EV_{CC}		I	**External Interrupt 1** $\overline{INT1}$ input set OEIT in ISEL Register, IE1 in the TCON register. If bit IT1 in this register is set, bits OEIT and IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits OEIT and IE1 is set by a low level on $\overline{INT1}$
					I	**UART function** Output enable. A low or high level (depending OELEV bit in ISEL Register) on this pin disables the PMOS transistors of TxD (P3.1) and T0 (P3.4). This function can be disabled by software
					I/O	**Input/Output function** P3.3 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: Gate input** INT1 serves as external run control for Timer 1 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.4		T0	EV_{CC}		O	**UART function** OE active at low or high level depending of PMSOEN bits in SIOCON Reg.

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
					I/O	**Input/Output function** P3.4 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0 function: External clock input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.5	CIO1		DV_{CC}		I/O	**Alternate card function** Card I/O
					I/O	**Input/Output function** P3.5 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: External clock input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.
					I	**Reset configuration** Input (high level due to internal pull-up)
P3.6	CCLK1	LED0	DV_{CC}		O	**Alternate card function** Card clock
					O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.6 is a LED port.
					I	**Reset configuration** Input at high level
P3.7	CRST1		DV_{CC}		O	**Alternate card function** Card reset
P3.7	CRST1	LED1	DV_{CC}		O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.7 is a a LED port.
					I	**Reset configuration** Input at high level

Table 17. SCISR Register

SCISR (S:ADh, SCRS = 0)
Smart Card UART Interface Status Register

7	6	5	4	3	2	1	0
SCTBE	**CARDIN**	**CIccOVF**	**CVccOK**	**SCWTO**	**SCTC**	**SCRC**	**SCPE**

Bit Number	Bit Mnemonic	Description
7	SCTBE	**SCIB transmit buffer empty** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when SCTBUF is written to.
6	CARDIN	**Card presence status** This bit is set when a card is detected (debouncing filter has to be done in software). It is cleared otherwise.
5	CIccOVF	**ICC overflow on card** This bit is set when the current on card is above the limit It shall be cleared by the hardware .
4	CVccOK	**Card voltage status** This bit is set when the output voltage is within the voltage range specified by CVcc field. It is cleared otherwise.
3	SCWTO	**Smart card wait Timeout** This bit is set by hardware when the Smart card wait time counter times out. It shall be cleared by the reload of the counter or by the reset of the SCIB.
2	SCTC	**Smart card transmitted character** This bit is set by hardware when the Smart Card UART has transmitted a character. It shall be cleared by software after this register has been read.
1	SCRC	**Smart card received character** This bit is set by hardware when the Smart Card UART has received a character It is cleared by hardware when SCBUF is read.
0	SCPE	**Smart card parity error** This bit is set at the same time as SCTI or SCRI if a parity error is detected. It shall be cleared by software after this register has been read.

Reset Value = 1000 0000b

Table 18. SCIIR Register

SCIIR (S:AEh, SCRS = 0)
Smart Card UART Interrupt
Identification Register (read only)

7	6	5	4	3	2	1	0
SCTBI	**-**	**CIccERR**	**CVccERR**	**SCWTI**	**SCTI**	**SCRI**	**SCPI**

Bit Number	Bit Mnemonic	Description
7	SCTBI	**SCIB transmit buffer interrupt** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when this register is read.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CIccERR	**Card current status** This bit is set when the output current goes out of the current range. It is cleared by hardware when this register is read.
4	CVccERR	**Card voltage status** This bit is set when the output voltage goes out of the voltage range specified by CVcc field. It is cleared by hardware when this register is read.
3	SCWTI	**Smart card wait Timeout interrupt** This bit is set by hardware when the Smart Card Timer 0 times out. It is cleared by hardware when this register is read.
2	SCTI	**Smart card transmit interrupt** This bit is set by hardware when the Smart Card UART completes a character transmission. It is cleared by hardware when this register is read.
1	SCRI	**Smart card receive interrupt** This bit is set by hardware when the Smart Card UART completes a character reception. It is cleared by hardware when this register is read.
0	SCPI	**Smart card parity error interrupt** This bit is set at the same time as SCTI or SCRI if a parity error is detected. It is cleared by hardware when this register is read.

Reset Value = 0X00 0000b

Table 19. SCIER Register

SCIER (S:AEh, SCRS = 1)
Smart Card UART Interrupt Enable Register

7	6	5	4	3	2	1	0
ESCTBI	**-**	**CIccER**	**ECVccER**	**ESCWTI**	**ESCTI**	**ESCRI**	**ESCPI**

Bit Number	Bit Mnemonic	Description
7	ESCTBI	**Smart Card UART Transmit Buffer Empty Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit Buffer Empty interrupt. Set this bit to enable the Smart Card UART Transmit Buffer Empty interrupt.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit .
5	CIccER	**Card Current Error Interrupt Enable** Clear this bit to disable the Card Current Error interrupt. Set this bit to enable the Card Current Error interrupt.
4	ECVccER	**Card Voltage Error Interrupt Enable** Clear this bit to disable the Card Voltage Error interrupt. Set this bit to enable the Card Voltage Error interrupt.
3	ESCWTI	**Smart Card Wait Timeout Interrupt Enable** Clear this bit to disable the Smart Card Wait timeout interrupt. Set this bit to enable the Smart Card Wait timeout interrupt.
2	ESCTI	**Smart Card Transmit Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit interrupt. Set this bit to enable the Smart Card UART Transmit interrupt.
1	ESCRI	**Smart Card Receive Interrupt Enable** Clear this bit to disable the Smart Card UART Receive interrupt. Set this bit to enable the Smart Card UART Receive interrupt.
0	ESCPI	**Smart Card Parity Error Interrupt Enable** Clear this bit to disable the Smart Card UART Parity Error interrupt. Set this bit to enable the Smart Card UART Parity Error interrupt.

Reset Value = 0X00 0000b

Table 20. SCSR Register

SCSR (S:ABh) Smart Card Selection Register

7	6	5	4	3	2	1	0
-	-	-	CREPSEL	ALTKPS1	ALTKPS0	SCCLK1	SCRS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	CREPSEL	**Character repetition selection** Clear this bit to select 5 times repetition before parity error indication Set this bit to select 4 times repetition before parity error indication
3-2	ALTKPS1 ALTKPS0	**Alternate Card Clock prescaler factor** 00ALTKPS = 0: prescaler factor equals 1 01ALTKPS = 1: prescaler factor equals 2 10ALTKPS = 2: prescaler factor equals 4 (reset value) 11ALTKPS = 3: prescaler factor equals 8
1	SCCLK1	**Alternate card clock selection** Set to select the prescaled clock (CCLK1) Clear to select the standard port configuration (P3.6)
0	SCRS	**Smart card register selection** The SCRS bit selects which set of the SCIB registers is accessed.

Reset Value = XXX0 1000b

Table 21. SCTBUF Register

SCTBUF (S:AA, write-only, SCRS = 0) Smart Card Transmit Buffer Register

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
–	–	Can store a new byte to be transmitted on the I/O pin when SCTBE is set. Bit ordering on the I/O pin depends on the Convention (see SCICR Register).

Reset Value = 0000 0000b

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 31. Interrupt Vector Addresses

Interrupt Source	Vector Address
IE0	0003h
TF0	000Bh
IE1 & RxIt & PrIt	0013h
TF1	001Bh
RI & TI	0023h
SCI	0053h

INT1 Interrupt Vector

The INT1 interrupt is multiplexed with the three following inputs:

- INT1/$\overline{OE}$: Standard 8051 interrupt input
- Rxd: Received data on UART
- CPRES: Insertion or removall of the main card

The setting configurations for each input is detailed below:

INT1/$\overline{OE}$ Input

This interrupt input is active under the following conditions:

- It must be enabled thanks to OEEN Bit (ISEL Register)
- It can be active on a level or falling edge: thanks to IT1 Bit (TCON Register)
- If level triggering selection is set, the active level 0 or 1 can be selected with OELEV Bit (ISEL Register)

The Bit IE1 (TCON Register) is set by hardware when external interrupt detected. It is cleared when interrupt is processed.

Rxd Input

A second vector interrupt input is the reception of a character. UART Rx input can generate an interrupt if enabled with Bit RXEN (ISEL.0). The global enable bits EX1 and EA must also be set.

Then, the Bit RXIT (ISEL Register) is set by hardware when a low level is detected on P3.0/RXD input.

CPRES Input

The third input is the detection of a level change on CPRES input (P1.2). This input can generate an interrupt if enabled with PRESEN (ISEL.1), EX1 (IE0.2) and EA (IE0.7) Bits.

This detection is done according to the level selected with Bit CPLEV (ISEL.7).

Then the Bit PRESIT (ISEL.5) is set by hardware when the triggering conditions are met. This Bit must be cleared by software.

Dual Data Pointer

T8xC5121 contains a Dual Data Pointer accelerating data memory block moves. The Standard 80C52 Data Pointer is a 16-bit value that is used to address off-chip data RAM or peripherals. In T8xC5121, the standard 16-bit data pointer is called DPTR and located at SFR location 82H and 83H. The second Data Pointer named DPTR1 is located at the same address than the previous one. The DPTR select bit (DPS / bit0) chooses the active pointer and it is located into the AUXR1 register. It should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

The user switches between data pointers by toggling the LSB of the AUXR1. The increment (INC) is a solution for this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual Data Pointer saves code and resources when moves of blocks need to be accomplished.

The second Data Pointer can be used to address the on-chip XRAM.

Table 41. DPL Register

DPL - Low Byte of DPTR1 (82h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 42. DPH Register

DPH - High Byte of DPTR1 (83h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 43. AUXR1 Register

AUXR1 - Dual Pointer Selection Register (A2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data pointer 1** Clear to select DPTR0 as Data Pointer. Set to select DPTR1 as Data Pointer.

Reset value = XXXX XXX0b

UART Timings

The following description will be included in L version:

Mode Selection

SM0 and SM1 bits in SCON register (see Table 67) are used to select a mode among the single synchronous and the three asynchronous modes according to Table 64.

Table 64. Serial I/O Port Mode Selection

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Synchronous Shift Register	Fixed / Variable
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

Baud Rate Generator

Depending on the mode and the source selection, the baud rate can be generated from either the Timer 1 or the Internal Baud Rate Generator. The Timer 1 can be used in Modes 1 and 3 while the Internal Baud Rate Generator can be used in Modes 0, 1 and 3.

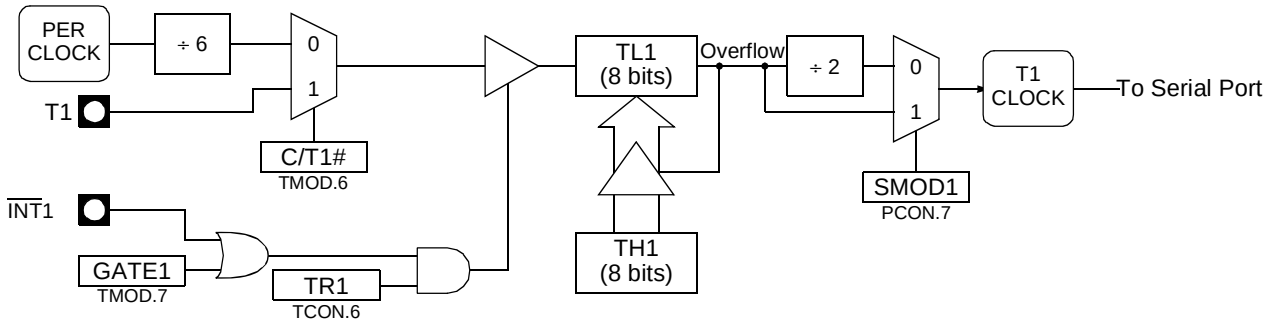
The addition of the Internal Baud Rate Generator allows freeing of the Timer 1 for other purposes in the application. It is highly recommended to use the Internal Baud Rate Generator as it allows higher and more accurate baud rates than with Timer 1.

Baud rate formulas depend on the modes selected and are given in the following mode sections.

Timer 1

When using the Timer 1, the Baud Rate is derived from the overflow of the timer. As shown in Figure 36 the Timer 1 is used in its 8-bit auto-reload mode (detailed in Section “Timer 0/Counter Operations”, page 73). SMOD1 bit in PCON register allows doubling of the generated baud rate.

Figure 36. Timer 1 Baud Rate Generator Block Diagram



Internal Baud Rate Generator

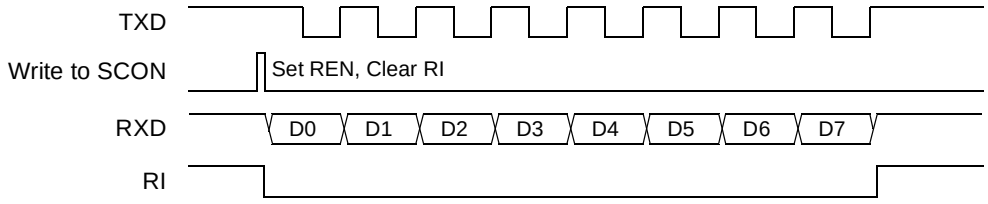
When using the Internal Baud Rate Generator, the Baud Rate is derived from the overflow of the timer. As shown in Figure 37, the Internal Baud Rate Generator is an 8-bit auto-reload timer feed by the peripheral clock or by the peripheral clock divided by 6 depending on the SPD bit in BDRCON register (see Table 68). The Internal Baud Rate Generator is enabled by setting BBR bit in BDRCON register. SMOD1 bit in PCON register allows doubling of the generated baud rate.

Reception (Mode 0)

To start a reception in mode 0, write to SCON register clearing SM0, SM1 and RI bits and setting the REN bit.

As shown in Figure 40, Clock is pulsed and the LSB (D0) is sampled on the RXD pin. The D0 bit is then shifted into the shift register. After eight sampling, the MSB (D7) is shifted into the shift register, and hardware asserts RI bit to indicate a completed reception. Software can then read the received byte from SBUF register.

Figure 40. Reception Waveforms (Mode 0)



Baud Rate Selection (Mode 0)

In mode 0, baud rate can be either fixed or variable.

As shown in Figure 41, the selection is done using M0SRC bit in BDRCON register. Figure 42 gives the baud rate calculation formulas for each baud rate source.

Figure 41. Baud Rate Source Selection (Mode 0)

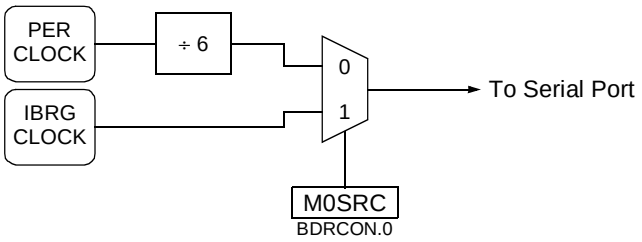


Figure 42. Baud Rate Formulas (Mode 0)

$$\text{Baud\_Rate} = \frac{F_{PER}}{6}$$

a. Fixed Formula

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot (256 - BRL)}$$

$$BRL = 256 - \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot \text{Baud\_Rate}}$$

b. Variable Formula

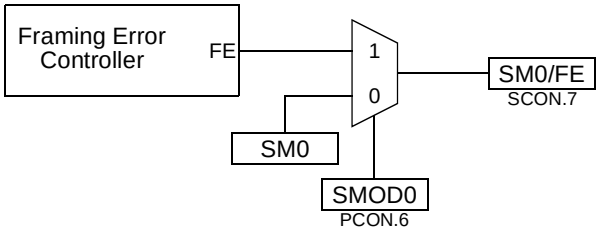
Framing Error Detection (Modes 1, 2 and 3)

Framing error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register as shown in Figure 46.

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two devices. If a valid stop bit is not found, the software sets FE bit in SCON register.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a chip reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When the framing error detection feature is enabled, RI rises on stop bit instead of the last data bit as detailed in Figure 36.

Figure 46. Framing Error Block Diagram



Baud Rate Selection (Modes 1 and 3)

In modes 1 and 3, the Baud Rate is derived either from the Timer 1 or the Internal Baud Rate Generator and allows different baud rate in reception and transmission.

As shown in Figure 47 the selection is done using RBCK and TBCK bits in BDRCON register.

Figure 48 gives the baud rate calculation formulas for each baud rate source while Table 65 details Internal Baud Rate Generator configuration for different peripheral clock frequencies and giving baud rates closer to the standard baud rates.

Figure 47. Baud Rate Source Selection (Modes 1 and 3)

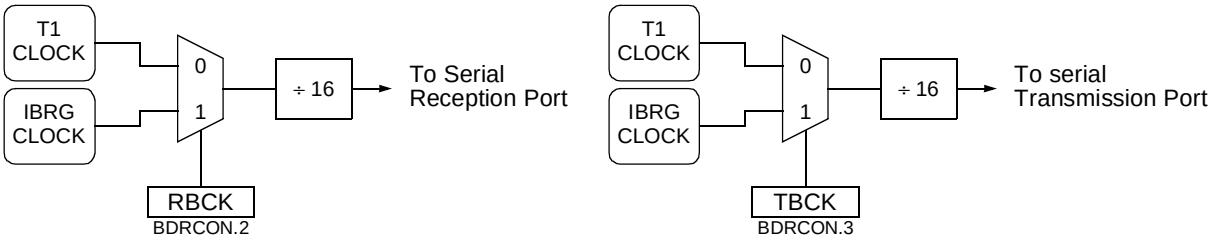


Figure 48. Baud Rate Formulas (Modes 1 and 3)

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot (256 - BRL)}$$

$$BRL = 256 \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot \text{Baud\_Rate}}$$

a. BRG Formula

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6 \cdot 32 \cdot (256 - TH1)}$$

$$TH1 = 256 \frac{2^{SMOD1} \cdot F_{PER}}{192 \cdot \text{Baud\_Rate}}$$

b. T1 Formula

Table 65. Internal Baud Rate Generator Value

Baud Rate	F_{PER} = 6 MHz[1]				F_{PER} = 8 MHz[1]			
	SPD	SMOD1	BRL	Error %	SPD	SMOD1	BRL	Error %
115200	-	-	-	-	-	-	-	-
57600	-	-	-	-	1	1	247	3.55
38400	1	1	246	2.34	1	1	243	0.16
19200	1	1	236	2.34	1	1	230	0.16
9600	1	1	217	0.16	1	1	204	0.16
4800	1	1	178	0.16	1	1	152	0.16

Baud Rate	F_{PER} = 12 MHz[2]				F_{PER} = 16 MHz[2]			
	SPD	SMOD1	BRL	Error %	SPD	SMOD1	BRL	Error %
115200	-	-	-	-	1	1	247	3.55
57600	1	1	243	0.16	1	1	239	2.12
38400	1	1	236	2.34	1	1	230	0.16
19200	1	1	217	0.16	1	1	204	0.16
9600	1	1	178	0.16	1	1	152	0.16
4800	1	1	100	0.16	1	1	48	0.16

Notes: 1. These frequencies are achieved in X1 mode, $F_{PER} = F_{OSC} \div 2$.
2. These frequencies are achieved in X2 mode, $F_{PER} = F_{OSC}$.

Baud Rate Selection (Mode 2)

In mode 2, the baud rate can only be programmed to two fixed values: 1/16 or 1/32 of the peripheral clock frequency.

As shown in Figure 49, the selection is done using SMOD1 bit in PCON register.

Figure 50 gives the baud rate calculation formula depending on the selection.

Figure 49. Baud Rate Generator Selection (Mode 2)

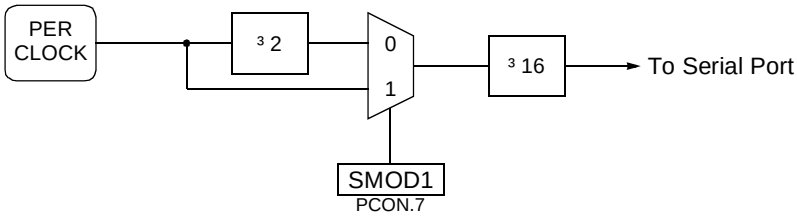


Figure 50. Baud Rate Formula (Mode 2)

$$Baud\_Rate = \frac{2^{SMOD1} \cdot FPER}{32}$$

Table 69. SIOCON Register
Serial Input Output Configuration Register
Register (91h)

7	6	5	4	3	2	1	0
PMSOEN1	**PMSOEN0**	**-**	**-**	**CPRES RES**	**EVAUTO**	**VEXT0**	**VEXT1**

Bit Number	Bit Mnemonic	Description
7 - 6	PMOSEN1 PMOSEN0	**Output Enable function on Txd/P3.1 and T0/P3.4:** PMSOEN1 PMSOEN0 0 0 PMOS is always off (reset value) 0 1 PMOS is always driven according to P3.1 or P3.4 value 1 0 PMOS is driven only when OE is high 1 1 PMOS is driven only when OE is low
5 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	CPRES RES	**Card Presence pull-up resistor** 0 Internal pull-up is connected 1 Internal pull-up is disconnected
2	EVAUTO	**EVCC Auto setup** Set to enable the Automatic mode of EV_{CC}regulator Clear to disable the Automatic mode of EV_{CC} regulator
1 - 0	VEXT0 VEXT1	**EVCC voltage configuration:** VEXT0 VEXT1 0 0 Power-down, EV_{CC} is external (reset value) 0 1 EV_{CC} = 1.8V 1 0 EV_{CC} = 2.3V 1 1 EV_{CC} = 2.7V

Reset Value = 00XX 0000b

Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias	-25°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V_{CC} to V_{SS}	-0.5V to + 6.0V
Voltage on Any Pin to V_{SS}	-0.5V to V_{CC} + 0.5V

Note: Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.85V to 5.4V; F = 7.36 to 16 MHz

Table 72. Core DC Parameters (XTAL, $\overline{RST}$, P0, P2, ALE, $\overline{PSEN}$, $\overline{EA}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, $\overline{RST}$	.2 V_{CC} + .9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, Port 0 and 2			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage, Port 0 and 2	0.9 x V_{CC}			V	I_{OH} = -40 µA
DI_{CC}	Digital Supply Output Current		6	10	mA	C_L = 100 nF
DV_{CC}	Digital Supply Voltage	2.5	2 .9	3.0	V	C_L = 100 nF DIcc=10mA
Icc	Normal Power Down mode		80	100	µA	25°C
Icc	Pulsed Power Down mode		20	30	µA	50°C Vcc=3V
Iccop	Power Supply current	I_{ccop} = 0.25 Freq (MHz) +4 mA I_{ccIDLE} = 0.03 Freq (MHz) +5 mA				V_{CC} = 5.4V and Bootloader execution
V_{PFDP}	Power-fail high level threshold		2 .55		V	
V_{PFDM}	Power-fail low level threshold		2 .45		V	
t_G	Power Fail glitch time			50	ns	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 µs		600	sec.	

Table 73. Serial Interface DC parameters (P3.0, P3.1, P3.3 and P3.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5 -0.5 -0.5		0.4 0.5 0.5	V V V	EV_{CC} = 1.8V EV_{CC} = 2.3V EV_{CC} = 2.8V External EVcc Automatic EVcc
V_{IH}	Input High Voltage	1.4 1.6 2.0 0.7 x EV_{CC}	EV_{CC}	2.3 2.8 3.3 EV_{CC} + 0.5	V V V V	EV_{CC} = 1.8V EV_{CC} = 2.3V EV_{CC} = 2.8V External EV_{CC} Automatic EVcc
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.2 mA
V_{OH}	Output High Voltage	1.6 1.8 2.2 0.8 x EV_{CC}		1.8 2.3 2.7 EV_{CC}	V V V V	EV_{CC} = 1.8V I_{OH} = 1 µA EV_{CC} = 2.3V EV_{CC} = 2.8V I_{OH} = 10µA External EV_{CC}
EI_{CC}	Extra Supply Current			+3	mA	C_L = 100 nF
EV_{CC}	Extra Supply Voltage	1.6 2.1 2.6 1.6	1.7 2.2 2.7	1.8 2.3 2.8 V_{CC}	V V V V	C_L = 100 nF, 1.8V C_L = 100 nF, 2.3V C_L = 100 nF, 2.8V External EV_{CC} Automatic EVcc
Ts	Sampling time					Automatic EVcc

Table 74. LED outputs DC Parameters (P3.6 and P3.7)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1 2 5	2 4 10	4 8 20	mA mA mA	2 mA configuration 4 mA configuration 10 mA configuration (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2V ± 20%)

Table 82. Smart Card RST, CC4, CC8, DC Parameters (Port P1.5, P1.3, P1.1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0(1) 0(1)		0.12 x CV_{CC} 0.4	V	I_{OL} = 20 µA I_{OL} = 50 µA
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	CV_{CC} - 0.5 0.8 x CV_{CC}		CV_{CC} CV_{CC} (1)	V	I_{OH} = 50 µA I_{OH} = 20 µA
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall delays			0.8	µs	C_{IN} = 30 pF
	Voltage stability	-0.25 CV_{CC}-0.5		0.4 x CV_{CC} CV_{CC} + 0.25		Low level High level

Note: 1. The voltage on RST should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 83. Alternate Card RST DC Parameters (Port P3.7) : 5V tolerant

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0 (1)		0.2 x DV_{CC}	V	I_{OL} = 200 µA
V_{OH}	Output High Voltage	0.8 x DV_{CC} 0.8 x DV_{CC}		DV_{CC} (1) DV_{CC}	V	I_{OH} = 20 µA (1.8V) I_{OH} = 200 µA (3V)
t_R t_F	Rise and Fall delays			400	µs	C_{IN} = 30 pF

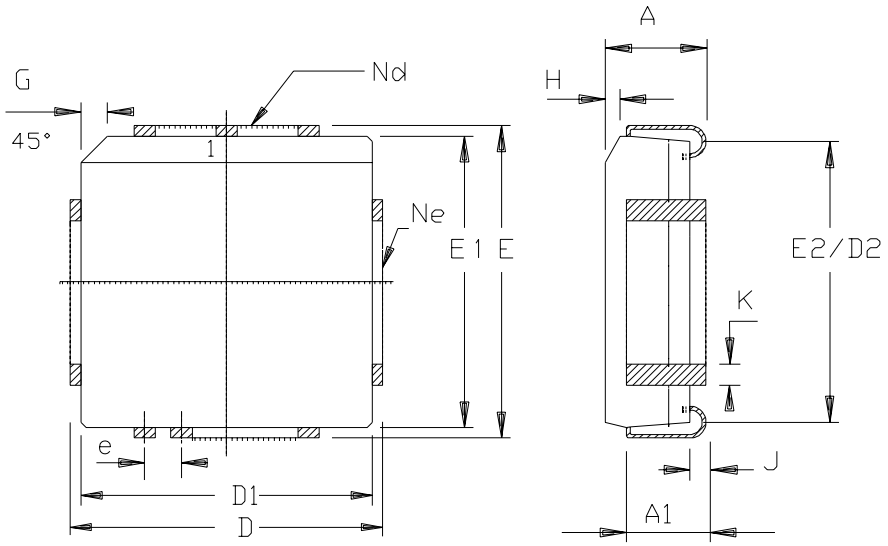
Note: 1. The voltage on RST should remain between -0.3V and DV_{CC} + 0.3V during dynamic operation.

Table 84. Card Presence DC Parameters (P1.2)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL1}	CPRES weak pull-up output current	3	10	25	µA	P1.2 = 1, short to V_{SS} (internal pull-up enabled)

6. Distance between Device pads and Smart Card connector must be less than 4 centimeters.
7. C6,C7 should be as close as possible to the Smart Card connector to reduce noise and interferences.

PLCC52



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.30	.090	.130
D	19.94	20.19	.785	.795
D1	19.05	19.25	.750	.758
D2	17.53	18.54	.690	.730
E	19.94	20.19	.785	.795
E1	19.05	19.25	.750	.758
E2	17.53	18.54	.690	.730
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	13		13	
Ne	13		13	
PKG STD	00			