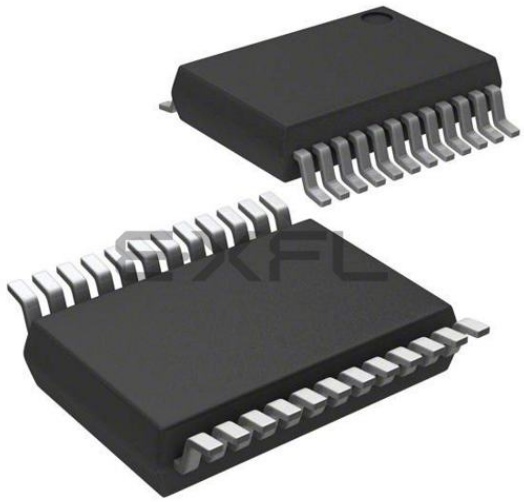

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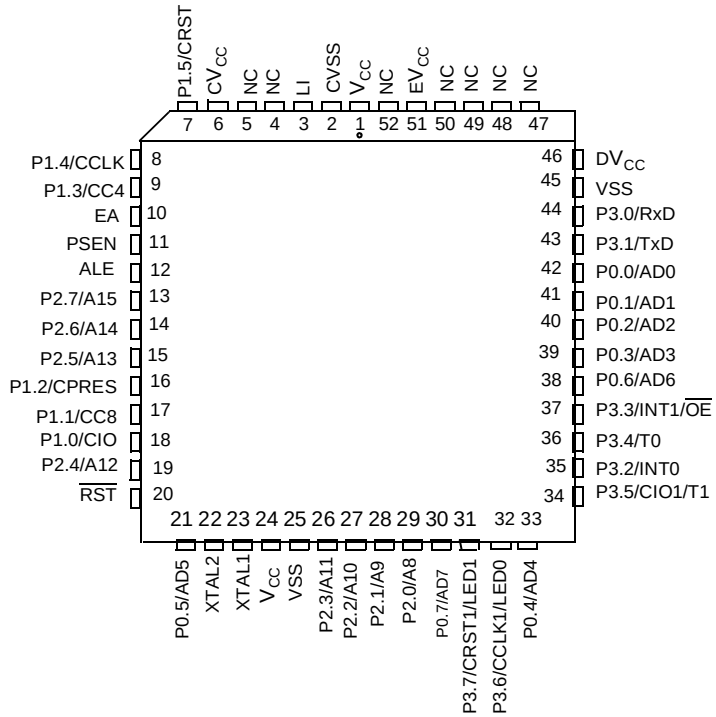
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	16MHz
Connectivity	SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	Code RAM
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 5.4V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.209", 5.30mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t85c5121-icsil

Figure 4. PLCC52 Pinout



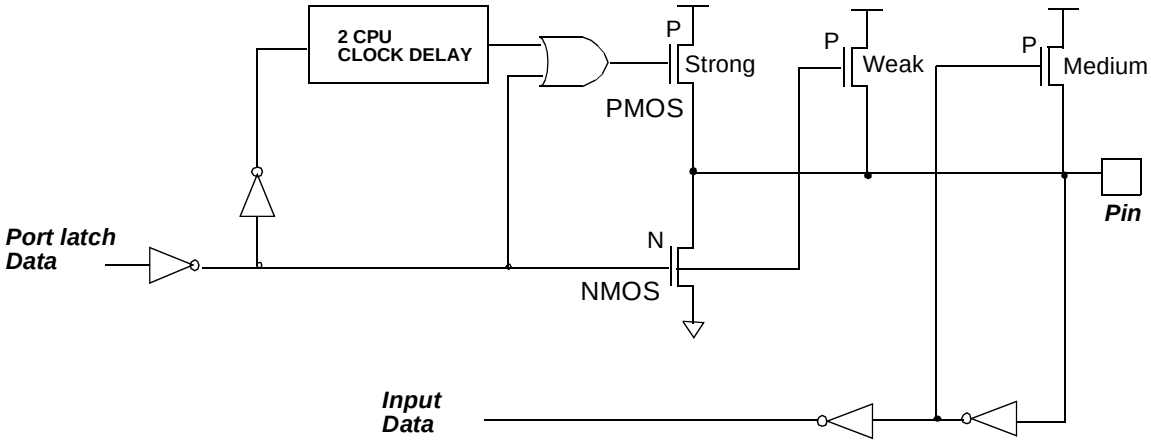
Port Structure Description

The different ports structures are described as follows.

Quasi Bi-directional Output Configuration

The default port output configuration for standard I/O ports is the quasi bi-directional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the port outputs a logic low state, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi bi-directional output that serve different purposes. One of these pull-ups, called the weak pull-up, is turned on whenever the port latch for the pin contains a logic 1. The weak pull-up sources a very small current that will pull the pin high if it is left floating. A second pull-up, called the medium pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the medium pull-up turns off, and only the weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the medium pull-up and take the voltage on the port pin below its input threshold.

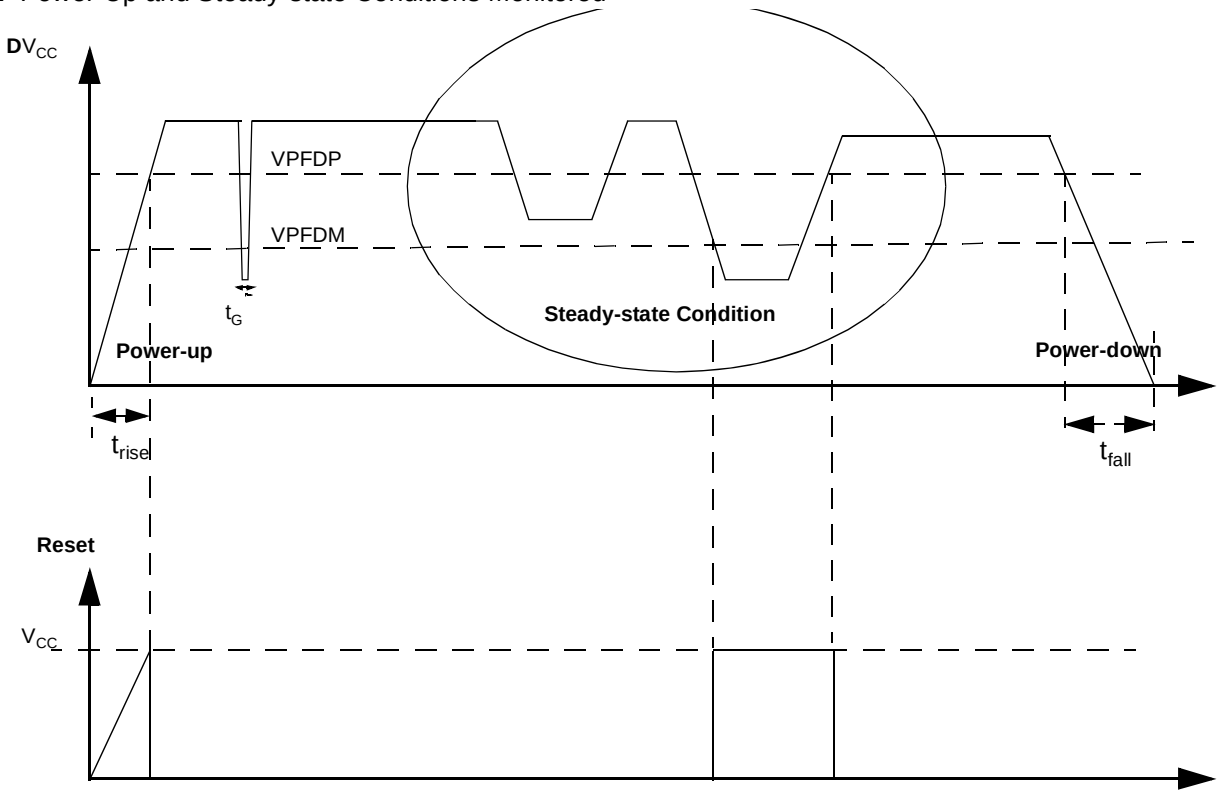
Figure 5. Quasi Bi-directional Output Configuration



Push-pull Output Configuration

The Push-pull output configuration has the same pull-down structure as the quasi bi-directional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The Push-pull mode may be used when more source current is needed from a port output. The Push-pull port configuration is shown in Figure 5.

Figure 9. Power-Up and Steady-state Conditions Monitored



Such device when it is integrated in a microcontroller, forces the CPU in reset mode when V_{DD} reaches a voltage condition which is out of the specification.

The thresholds and their functions are:

- V_{PFDP}: the output voltage of the regulator has reached a minimum functional value at the power-up. The circuit leaves the RESET mode.
- V_{PFDM}: the output voltage of the regulator has reached a low threshold functional value for the microcontroller. An internal RESET is set.

Glitch filtering prevents the system from RESET when short duration glitches are carried on V_{DD} power supply.

The electrical parameters V_{PFDP}, V_{PFDM}, t_{rise}, t_{fall}, t_G are specified in the DCparameters section.

Table 4. AUXR Register

AUXR (S:8Eh)
Auxiliary Register

7	6	5	4	3	2	1	0
-	LP	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	LP	**Low Power mode selection** Clear to select standard mode Set to select low consumption mode
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM select** **(ONLY for PLCC52 version)** Clear to map XRAM datas in internal XRAM memory. Set to map XRAM datas in external XRAM memory.
0	AO	**ALE Output bit** **(ONLY for PLCC52 version)** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = 00XX XX00b

Table 18. SCIIR Register

SCIIR (S:AEh, SCRS = 0)
Smart Card UART Interrupt
Identification Register (read only)

7	6	5	4	3	2	1	0
SCTBI	**-**	**CIccERR**	**CVccERR**	**SCWTI**	**SCTI**	**SCRI**	**SCPI**

Bit Number	Bit Mnemonic	Description
7	SCTBI	**SCIB transmit buffer interrupt** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when this register is read.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CIccERR	**Card current status** This bit is set when the output current goes out of the current range. It is cleared by hardware when this register is read.
4	CVccERR	**Card voltage status** This bit is set when the output voltage goes out of the voltage range specified by CVcc field. It is cleared by hardware when this register is read.
3	SCWTI	**Smart card wait Timeout interrupt** This bit is set by hardware when the Smart Card Timer 0 times out. It is cleared by hardware when this register is read.
2	SCTI	**Smart card transmit interrupt** This bit is set by hardware when the Smart Card UART completes a character transmission. It is cleared by hardware when this register is read.
1	SCRI	**Smart card receive interrupt** This bit is set by hardware when the Smart Card UART completes a character reception. It is cleared by hardware when this register is read.
0	SCPI	**Smart card parity error interrupt** This bit is set at the same time as SCTI or SCRI if a parity error is detected. It is cleared by hardware when this register is read.

Reset Value = 0X00 0000b

Table 22. SCRBUF Register

SCRBUF (S:AA read-only, SCRS = 1)
Smart Card Receive Buffer Register

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Bit Number	Bit Mnemonic	Description
–	–	**Provides the byte received from the I/O pin when SCRI is set.** Bit ordering on the I/O pin depends on the Convention (see SCICR Register).

Reset Value = 0000 0000b

Table 23. SCETU1 Register

SCETU1 (S:ADh, SCRS = 1)
Smart Card ETU Register 1

7	6	5	4	3	2	1	0
COMP	–	–	–	–	**ETU10**	**ETU9**	**ETU8**

Bit Number	Bit Mnemonic	Description
7	COMP	**Compensation** Clear this bit when no time compensation is needed (i.e. when the ETU to Card CLK period ratio is close to an integer with an error less than 1/4 of Card CLK period). Set this bit otherwise and reduce the ETU period by 1 Card CLK cycle for even bits.
6-3	–	**Reserved** The value read from these bits is indeterminate. Do not change these bits .
2-0	ETU[10:8]	**ETU MSB** Used together with the ETU LSB (see SCETU0 Register).

Reset Value = 0XXX X001b

Table 35. ISEL Register

7	6	5	4	3	2	1	0
CPLEV	**OEIT**	**PRESIT**	**RXIT**	**OELEV**	**OEEN**	**PRESEN**	**RXEN**

Bit Number	Bit Mnemonic	Description
7	CPLEV	**Card presence detection level** This bit indicates which CPRES level will bring about an interrupt Set this bit to indicate that Card Presence IT will appear if CPRES is at high level. Clear this bit to indicate that Card Presence IT will appear if CPRES is at low level.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PRESIT	**Card presence detection interrupt flag** Set by hardware Must be cleared by software
4	RXIT	**Received data interrupt flag** Set by hardware Must be cleared by software
3	OELEV	**OE/INT1 signal active level** Set this bit to indicate that high level is active. Clear this bit to indicate that low level is active.
2	OEEN	**OE/INT1 Interrupt Disable bit** Clear to disable INT1 interrupt Set to enable INT1 interrupt
1	PRESEN	**Card presence detection Interrupt Enable bit** Clear to disable the card presence detection interrupt coming from SCIB. Set to enable the card presence detection interrupt coming from SCIB.
0	RXEN	**Received data Interrupt Enable bit** Clear to disable the RxD interrupt. Set to enable the RxD interrupt (a minimal bit width of 0.1 ms is required to wake up from Power-Down).

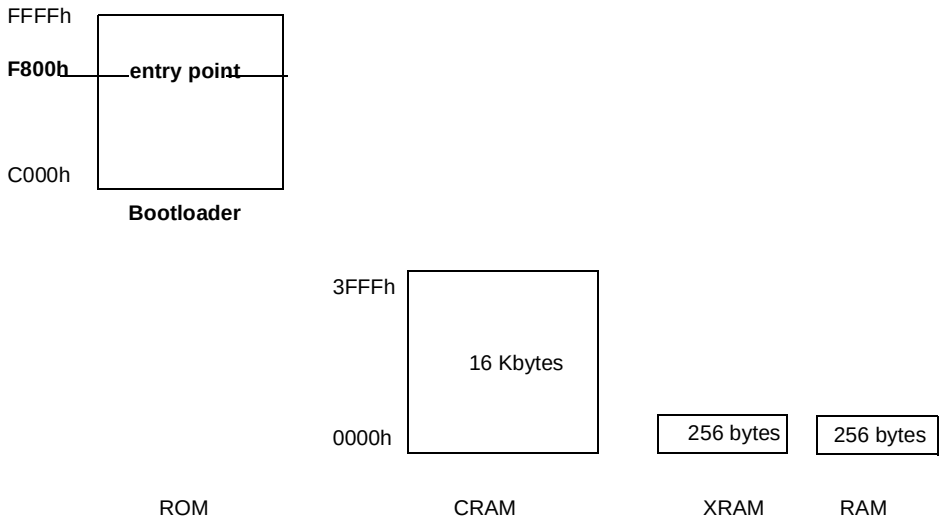
Reset Value = 0000 0100b

If a serial communication device (as described above: TWI or RS232) is detected, the program download its content in the internal EEPROM and in CRAM.

Else, the program is internally downloaded from the internal EEPROM into the program CRAM memory (16 Kbytes)

Then, in the two cases, the Bootloader executes a Long Jump at address 0000h which initializes the Program counter at the lower address (0000h) of the executable CRAM.

Figure 24. CRAM with ROM and EEPROM Memory Mappings



T85C121 Code RAM Version

Two memory blocks are implemented:

- The ROM memory contains the Bootloader program.
- The CRAM is the Application program memory.

After Reset, the program is downloaded, as described in last paragraph, from either an external EEPROM or from an host connected on RS232 serial link into the program CRAM memory of 16 Kbytes. Then the Program Counter is set at address 0000h of the CRAM space and the program is executed.

Source	Target	Case	Protection
UART ISP	Intern. EEP	Programming	SSB level 1 must be set (done, if selected, at ISP Programming or Ext EEP Donwload)
UART ISP	CRAM	Program access	SSB level 1 IN Int EEP protects as, first, the Int EEP is programmed before CRAM
UART ISP	SSB in EEP and CRAM	level 2 to level 1	Protected by Bootloader
UART ISP	SSB in EEP and CRAM	level 1 to level 0	Protected by Bootloader

Timers/Counters

Introduction

The T8xC5121 implements two general-purpose, 16-bit Timer 0s/Counters. Although they are identified as Timer 0, Timer 1, you can independently configure each to operate in a variety of modes as a Timer 0 or as an event Counter. When operating as a Timer 0, a Timer 0/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer 0/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

The Timer 0 registers and associated control registers are implemented as addressable Special Function Registers (SFRs). Two of the SFRs provide programmable control of the Timer 0s as follows:

- Timer 0/Counter mode control register (TMOD) and Timer 0/Counter control register (TCON) control respectively Timer 0 and Timer 1.

The various operating modes of each Timer 0/Counter are described below.

Timer 0/Counter Operations

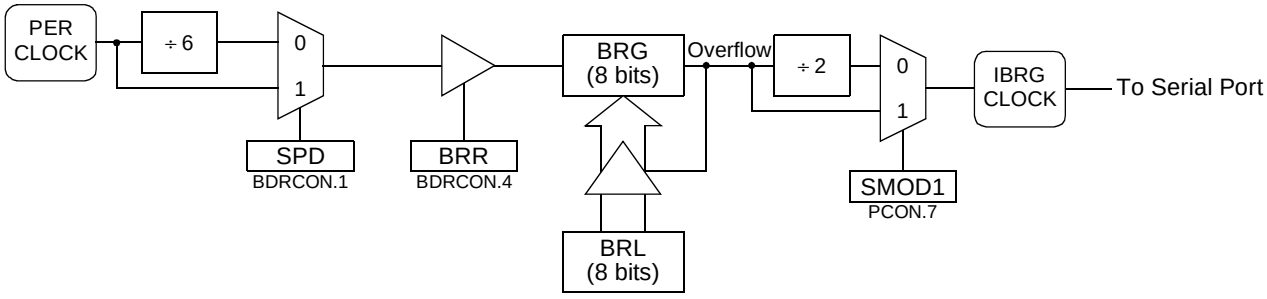
For example, a basic operation is Timer 0 registers THx and TLx (x = 0, 1) connected in cascade to form a 16-bit Timer 0. Setting the run control bit (TRx) in the TCON register (see Figure 55) turns the Timer 0 on by allowing the selected input to increment TLx. When TLx overflows it increments THx and when THx overflows it sets the Timer 0 overflow flag (TFx) in the TCON register. Setting the TRx does not clear the THx and TLx Timer 0 registers. Timer 0 registers can be accessed to obtain the current count or to enter preset values. They can be read at any time but the TRx bit must be cleared to preset their values, otherwise the behavior of the Timer 0/Counter is unpredictable.

The C/Tx# control bit selects Timer 0 operation or Counter operation by selecting the divided-down system clock or the external pin Tx as the source for the counted signal. The TRx bit must be cleared when changing the operating mode, otherwise the behavior of the Timer 0/Counter is unpredictable.
For Timer 0 operation (C/Tx# = 0), the Timer 0 register counts the divided-down system clock. The Timer 0 register incremented once every peripheral cycle.

Exceptions are the Timer 0 2 Baud Rate and Clock-Out modes in which the Timer 0 register is incremented by the system clock divided by two.

For Counter operation (C/Tx# = 1), the Timer 0 register counts the negative transitions on the Tx external input pin. The external input is sampled during every S5P2 state. The Programmer's Guide describes the notation for the states in a peripheral cycle. When the sample is high in one cycle and low in the next one, the Counter is incremented. The new count value appears in the register during the next S3P1 state after the transition has been detected. Since it takes 12 states (24 oscillator periods) to recognize a negative transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full peripheral cycle.

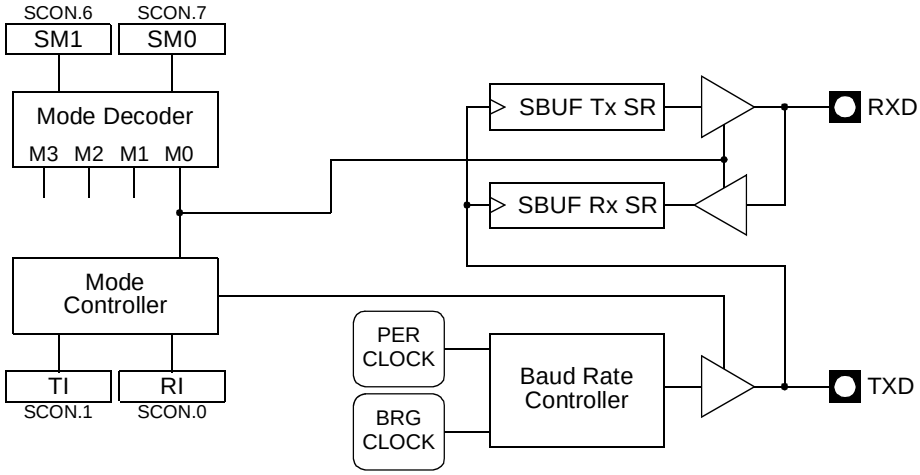
Figure 37. Internal Baud Rate Generator Block Diagram



Synchronous Mode (Mode 0)

Mode 0 is a half-duplex, synchronous mode, which is commonly used to expand the I/0 capabilities of a device with shift registers. The transmit data (TXD) pin outputs a set of eight clock pulses while the receive data (RXD) pin transmits or receives a byte of data. The 8-bit data are transmitted and received least-significant bit (LSB) first. Shifts occur at a fixed Baud Rate. Figure 38 shows the serial port block diagram in Mode 0.

Figure 38. Serial I/O Port Block Diagram (Mode 0)

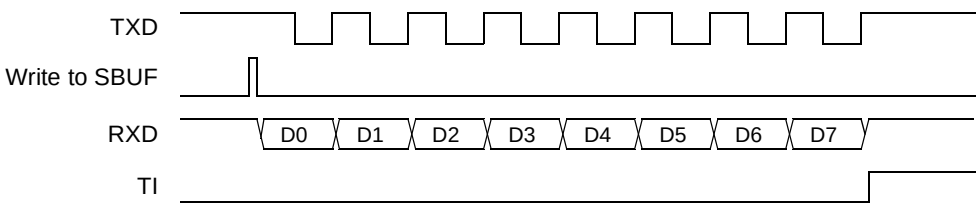


Transmission (Mode 0)

To start a transmission mode 0, write to SCON register clearing bits SM0, SM1.

As shown in Figure 39, writing the byte to transmit to SBUF register starts the transmission. Hardware shifts the LSB (D0) onto the RXD pin during the first clock cycle composed of a high level then low level signal on TXD. During the eighth clock cycle the MSB (D7) is on the RXD pin. Then, hardware drives the RXD pin high and asserts TI to indicate the end of the transmission.

Figure 39. Transmission Waveforms (Mode 0)

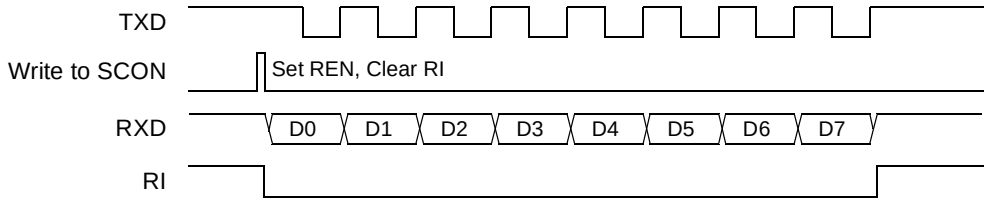


Reception (Mode 0)

To start a reception in mode 0, write to SCON register clearing SM0, SM1 and RI bits and setting the REN bit.

As shown in Figure 40, Clock is pulsed and the LSB (D0) is sampled on the RXD pin. The D0 bit is then shifted into the shift register. After eight sampling, the MSB (D7) is shifted into the shift register, and hardware asserts RI bit to indicate a completed reception. Software can then read the received byte from SBUF register.

Figure 40. Reception Waveforms (Mode 0)



Baud Rate Selection (Mode 0)

In mode 0, baud rate can be either fixed or variable.

As shown in Figure 41, the selection is done using M0SRC bit in BDRCON register. Figure 42 gives the baud rate calculation formulas for each baud rate source.

Figure 41. Baud Rate Source Selection (Mode 0)

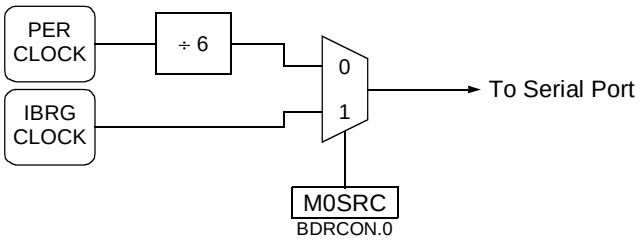


Figure 42. Baud Rate Formulas (Mode 0)

$$\text{Baud\_Rate} = \frac{F_{PER}}{6}$$

a. Fixed Formula

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot (256 - BRL)}$$

$$BRL = 256 - \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot \text{Baud\_Rate}}$$

b. Variable Formula

Table 67. SCON Register
SCON (S:98h)
Serial Control Registe

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit** To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.
	SM0	**Serial Port Mode bit 0** To select this function, clear SMOD0 bit in PCON register. Software writes to bits SM0 and SM1 to select the Serial Port operating mode. Refer to SM1 bit for the mode selections.
6	SM1	**Serial Port Mode bit 1** To select this function, set SMOD0 bit in PCON register. Software writes to bits SM1 and SM0 to select the Serial Port operating mode. SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register $F_{OSC}/12$ or variable if SRC bit in BDRCON is set 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{OSC}/32$ or $F_{OSC}/64$ 1 1 3 9-bit UART Variable
5	SM2	**Serial Port Mode bit 2** Software writes to bit SM2 to enable and disable the multiprocessor communication and automatic address recognition features. This allows the Serial Port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN	**Receiver Enable bit** Clear to disable reception in mode 1, 2 and 3, and to enable transmission in mode 0. Set to enable reception in all modes.
3	TB8	**Transmit bit 8** Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.
2	RB8	**Receiver bit 8** Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.
1	TI	**Transmit Interrupt flag** Set by the transmitter after the last data bit is transmitted. Must be cleared by software.
0	RI	**Receive Interrupt flag** Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.

Reset Value = XXX0 0000b

Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the Watchdog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x $T_{CLK\ PERIPH}$, where $T_{CLK\ PERIPH}= 1/F_{CLK\ PERIPH}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16 ms to 2s @ F_{OSCA} = 12 MHz. To manage this feature, refer to WDTPRG register description, Table 70. The WDTPRG register should be configured before the WDT activation sequence, and can not be modified until next reset.

Table 70. WDTRST Register

WDTRST - Watchdog Reset Register (0A6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias	-25°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V_{CC} to V_{SS}	-0.5V to + 6.0V
Voltage on Any Pin to V_{SS}	-0.5V to V_{CC} + 0.5V

Note: Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.85V to 5.4V; F = 7.36 to 16 MHz

Table 72. Core DC Parameters (XTAL, $\overline{RST}$, P0, P2, ALE, $\overline{PSEN}$, $\overline{EA}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, $\overline{RST}$	.2 V_{CC} + .9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, Port 0 and 2			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage, Port 0 and 2	0.9 x V_{CC}			V	I_{OH} = -40 µA
DI_{CC}	Digital Supply Output Current		6	10	mA	C_L = 100 nF
DV_{CC}	Digital Supply Voltage	2.5	2 .9	3.0	V	C_L = 100 nF DIcc=10mA
Icc	Normal Power Down mode		80	100	µA	25°C
Icc	Pulsed Power Down mode		20	30	µA	50°C Vcc=3V
Iccop	Power Supply current	I_{ccop} = 0.25 Freq (MHz) +4 mA I_{ccIDLE} = 0.03 Freq (MHz) +5 mA				V_{CC} = 5.4V and Bootloader execution
V_{PFDP}	Power-fail high level threshold		2 .55		V	
V_{PFDM}	Power-fail low level threshold		2 .45		V	
t_G	Power Fail glitch time			50	ns	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 µs		600	sec.	

Table 75. Smart Card 5V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	60		121 105 102	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	4.6		5.4	V	CIcc = 60 mA
CV_{CC}	Ripple on CVcc			200	mV	0<CIcc<60 mA
CV_{CC}	Spikes on CVcc	4.6		5.4	V	Maxi. charge 20 nA.s Max. duration 400 ns Max. variation CIcc 100 mA (1)
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 76. Smart Card 3V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	60		110 89 110	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	2.76		3.24	V	CIcc = 60 mA
CV_{CC}	Ripple on CVcc			200	mV	0<CIcc<60 mA
CV_{CC}	Spikes on CVcc	2.76		3.24	V	Max. charge 10 ns Max. duration 400 ns Max. variation CIcc 50 mA
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 77. Smart Card 1.8V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	20		109 100 82	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	1.68		1.92	V	CIcc = 20 mA
CV_{CC}	Spikes on CVcc	1.68		1.92	V	
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 78. Smart Card Clock DC Parameters (Port P1.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0(1) 0(1)		0.2 x CV_{CC} 0.4	V	I_{OL} = 20 µA (1.8,3 V) I_{OL} = 50 µA (5V)
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	0.7 x CV_{CC} 0.7 x CV_{CC} CV_{CC} - 0.5		CV_{CC} CV_{CC} CV_{CC}	V V V	I_{OH} = 20 µA (1.8V) I_{OH} = 20 µA (3V) I_{OH} = 50 µA (5V)
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall time			16 22.5 50	ns	C_{IN} = 30 pF(5V) C_{IN} = 30 pF(3V) C_{IN} = 30 pF(1.8V)
	Voltage Stability	-0.25 CV_{CC}-0.5		0.4 x CV_{CC} CV_{CC} + 0.25	V	Low level High level

Note: 1. The voltage on CLK should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 79. Alternate Card Clock DC parameters (Port P3.6): 5V tolerant

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0 (1) 0(1)		0.2 x DV_{CC} 0.5	V	I_{OL} = 20 µA I_{OL} = -200 µA
V_{OH}	Output High Voltage	0.7 x DV_{CC}		DV_{CC} (1)	V	I_{OH} = 20 µA
t_R t_F	Rise and Fall times			18	ns	C_{IN} = 30 pF

Note: 1. The voltage on CLK should remain between -0.3V and V_{CC} + 0.3V during dynamic operation.

Table 82. Smart Card RST, CC4, CC8, DC Parameters (Port P1.5, P1.3, P1.1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0(1) 0(1)		0.12 x CV_{CC} 0.4	V	I_{OL} = 20 µA I_{OL} = 50 µA
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	CV_{CC} - 0.5 0.8 x CV_{CC}		CV_{CC} CV_{CC} (1)	V	I_{OH} = 50 µA I_{OH} = 20 µA
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall delays			0.8	µs	C_{IN} = 30 pF
	Voltage stability	-0.25 CV_{CC}-0.5		0.4 x CV_{CC} CV_{CC} + 0.25		Low level High level

Note: 1. The voltage on RST should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 83. Alternate Card RST DC Parameters (Port P3.7) : 5V tolerant

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0 (1)		0.2 x DV_{CC}	V	I_{OL} = 200 µA
V_{OH}	Output High Voltage	0.8 x DV_{CC} 0.8 x DV_{CC}		DV_{CC} (1) DV_{CC}	V	I_{OH} = 20 µA (1.8V) I_{OH} = 200 µA (3V)
t_R t_F	Rise and Fall delays			400	µs	C_{IN} = 30 pF

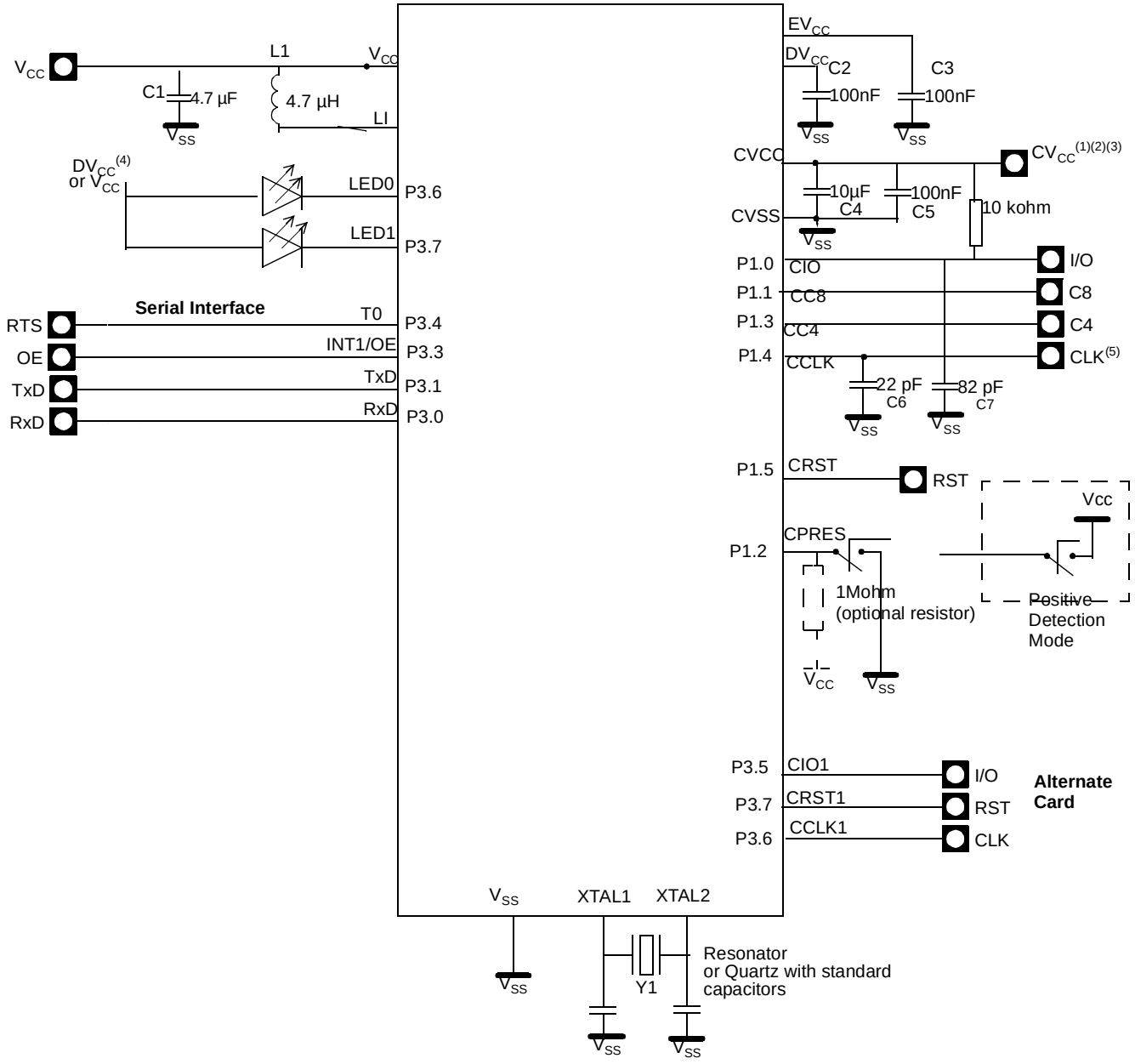
Note: 1. The voltage on RST should remain between -0.3V and DV_{CC} + 0.3V during dynamic operation.

Table 84. Card Presence DC Parameters (P1.2)

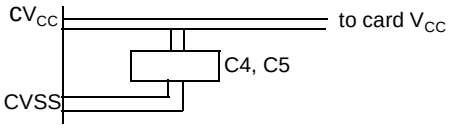
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL1}	CPRES weak pull-up output current	3	10	25	µA	P1.2 = 1, short to V_{SS} (internal pull-up enabled)

Typical Application

Figure 54. Typical Application Diagram



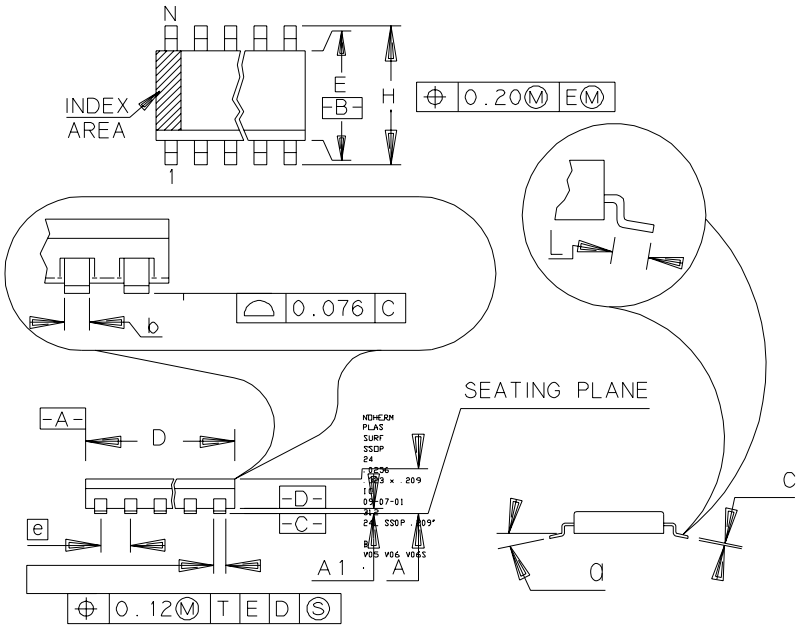
Notes:
1. C4 and C5 must be placed near IC and have low ESR (<250mΩ)
2. Straight and short connections avoid any loop between:
   - CVSS and V_{SS}
   - CV_{CC} and C4, C5
3. V_{CC} connection of the master card must be placed as follows:



4. Current is limited to 10 mA.
5. CCLK should be routed far from CRST, CIO, CC4, CC8 and armored by ground plane.

Package Drawings

SSOP24



	MM		INCH	
A	1.73	1.99	.068	.078
A1	0.05	0.21	.002	.008
b	0.25	0.38	.010	.015
C	0.09	0.20	.004	.008
D	8.07	8.33	.318	.328
E	5.20	5.38	.205	.212
e	0.65	BSC	.0256	BSC
H	7.65	7.90	.301	.311
L	0.63	0.95	.025	.037
N	24		24	
a	0°	8°	0°	8°