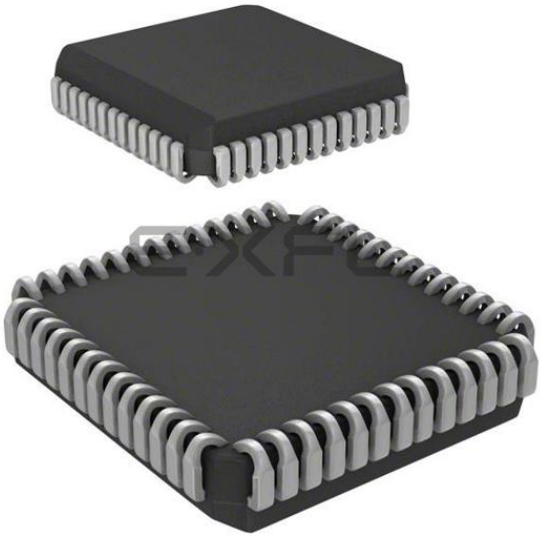

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	16MHz
Connectivity	SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	Code RAM
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 5.4V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.15x19.15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t85c5121-s3sil

Signals

All the T8xC5121 signals are detailed in Table 1.

The port structure is described in Section “Port Structure Description”.

Table 1. Ports Description

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P1.0	CIO		CV_{CC}	4 kV	I/O	**Smart card interface function** Card I/O.
					I/O	**Input/Output function** P1.0 is a bi-directional I/O port .
					I	**Reset configuration** Input .
P1.1	CC8		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 8
					O	**Output function** P1.1 is a Push-pull port.
					I	**Reset configuration** Input
P1.2	CPRES		V_{CC}	4 kV	I	**Smart card interface function** Card presence
					I/O	**Input/Output function** P1.2 is a bi-directional I/O port with internal pull-ups- (External Pull-up configuration can be selected).
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.3	CC4		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 4
					O	**Output function** P1.3 is a Push-pull port.
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.4	CCLK		CV_{CC}	4 kV	O	**Smart card interface function** Card clock
					I/O	**Input/Output function** P1.4 is a a Push-pull port.
					O	**Reset configuration** Output at low level
P1.5	CRST		CV_{CC}	4 kV	O	**Smart card interface function** Card reset
					I/O	**Input/Output function** P1.5 is a a Push-pull port.
					O	**Reset configuration** Output at low level

PowerMonitor

The PowerMonitor function supervises the evolution of the voltages feeding the microcontroller, and if needed, suspends its activity when the detected value is out of specification.

It is guaranteed to start up properly when T8xC5121 is powered up and prevents code execution errors when the power supply becomes lower than the functional threshold.

This section describes the functions of the PowerMonitor.

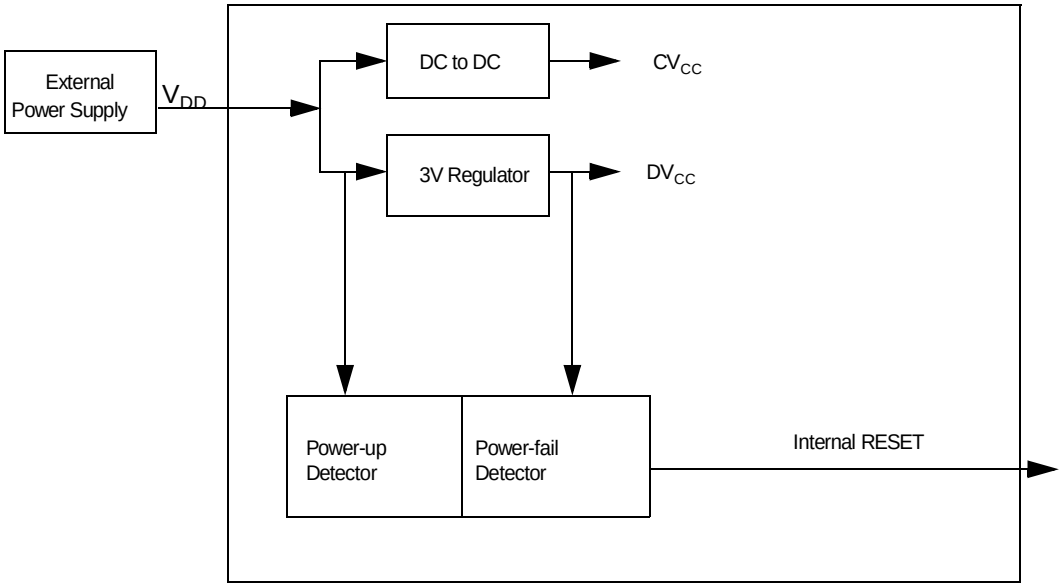
Description

In order to start up and to properly maintain the microcontroller operation, V_{DD} has to be stabilized in the V_{DD} operating range and the oscillator has to be stabilised with a nominal amplitude compatible with logic threshold.

This control is carried out during three phases which are the power-up, normal operation and stop. It complies with the following requirements:

- It guarantees an operational Reset when the microcontroller is powered
- and a protection if the power supply goes out from the functional range of the microcontroller.

Figure 8. PowerMonitor Block Diagram



PowerMonitor Diagram

The target of the PowerMonitor is to survey the power supply in order to detect any voltage drops which are not in the target specification. This PowerMonitor block checks two kind of situations that occur:

- During the power-up condition, when V_{DD} is reaching the product specification
- During a steady-state condition, when V_{DD} is stable but disturbed by any undesirable voltage drops.

Figure 9 shows some configurations that can be met by the PowerMonitor.

Table 5. IE0 Register

IE0
Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**-**	**-**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable Timer 0 overflow interrupt. Set to enable Timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b

Smart Card Interface Block (SCIB)

Introduction

The SCIB provides all signals to directly interface a smart card. Compliance with the ISO7816, EMV'2000, GSM and WHQL standards has been certified.

Both synchronous (e.g. memory card) and asynchronous smart cards (e.g. microprocessor card) are supported. The component supplies the different voltages requested by the smart card. The power-off sequence is directly managed by the SCIB.

The card presence switch of the smart card connector is used to detect card insertion or card removal. In case of card removal, the SCIB de-activates the smart card using the de-activation sequence. An interrupt can be generated when a card is inserted or removed.

Any malfunction is reported to the microcontroller (interrupt + control register).

The different operating modes are configured by internal registers.

Main Features

- Support of ISO/IEC7816
- Character mode
- 1 transmit buffer + 1 receive buffer
- 11 bits ETU counter
- 9 bits guard time counter
- 24 bits waiting time counter
- Auto-character repetition on error signal detection in transmit mode
- Auto-error signal generation on parity error detection in receive mode
- Power-on and power-off sequence generation
- Manual mode to directly drive the card I/O

Table 16. SCCON Register

SCCON (S:ACh, SCRS = 0)
Smart Card Contacts Register

7	6	5	4	3	2	1	0
CLK	-	CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC

Bit Number	Bit Mnemonic	Description
7	CLK	**Card Clock Selection** Clear this bit to use the CardClk bit (CARDCLK) to drive Card CLK pin. Set this bit to use XTAL signal to drive the Card CLK pin. **Note:** internal synchronization avoids any glitch on the CLK pin when switching this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CARDC8	**Card C8** Clear this bit to drive a low level on the Card C8 pin. Set this bit to set a high level on the Card C8 pin.
4	CARDC4	**Card C4** Clear this bit to drive a low level on the Card C4 pin. Set this bit to set a high level on the Card C4 pin.
3	CARDIO	**Card I/O** When the UART bit is cleared in SCICR Register, the value of this bit is driven to the Card I/O pin. Then this pin can be used as a pseudo bi-directional I/O when this bit is set. To be used as an input, this bit must contain a 1.
2	CARDCLK	**Card CLK** When the CLK bit is cleared in SCCON Register, the value of this bit is driven to the Card CLK pin.
1	CARDRST	**Card RST** Clear this bit to drive a low level on the Card RST pin. Set this bit to set a high level on the Card RST pin. Read is not allowed if VCARDOK=0
0	$CARDV_{CC}$	**Card VCC Control** Clear this bit to desactivate the Card interface and set its power-off. The other bits of SCC register have no effect while this bit is cleared. Set this bit to power-on the Card interface. The activation sequence shall be handled by software.

Reset Value = 0X00 0000b

Table 19. SCIER Register

SCIER (S:AEh, SCRS = 1)
Smart Card UART Interrupt Enable Register

7	6	5	4	3	2	1	0
ESCTBI	**-**	**CIccER**	**ECVccER**	**ESCWTI**	**ESCTI**	**ESCRI**	**ESCPI**

Bit Number	Bit Mnemonic	Description
7	ESCTBI	**Smart Card UART Transmit Buffer Empty Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit Buffer Empty interrupt. Set this bit to enable the Smart Card UART Transmit Buffer Empty interrupt.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit .
5	CIccER	**Card Current Error Interrupt Enable** Clear this bit to disable the Card Current Error interrupt. Set this bit to enable the Card Current Error interrupt.
4	ECVccER	**Card Voltage Error Interrupt Enable** Clear this bit to disable the Card Voltage Error interrupt. Set this bit to enable the Card Voltage Error interrupt.
3	ESCWTI	**Smart Card Wait Timeout Interrupt Enable** Clear this bit to disable the Smart Card Wait timeout interrupt. Set this bit to enable the Smart Card Wait timeout interrupt.
2	ESCTI	**Smart Card Transmit Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit interrupt. Set this bit to enable the Smart Card UART Transmit interrupt.
1	ESCRI	**Smart Card Receive Interrupt Enable** Clear this bit to disable the Smart Card UART Receive interrupt. Set this bit to enable the Smart Card UART Receive interrupt.
0	ESCPI	**Smart Card Parity Error Interrupt Enable** Clear this bit to disable the Smart Card UART Parity Error interrupt. Set this bit to enable the Smart Card UART Parity Error interrupt.

Reset Value = 0X00 0000b

Table 22. SCRBUF Register

SCRBUF (S:AA read-only, SCRS = 1)
Smart Card Receive Buffer Register

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Bit Number	Bit Mnemonic	Description
–	–	**Provides the byte received from the I/O pin when SCRI is set.** Bit ordering on the I/O pin depends on the Convention (see SCICR Register).

Reset Value = 0000 0000b

Table 23. SCETU1 Register

SCETU1 (S:ADh, SCRS = 1)
Smart Card ETU Register 1

7	6	5	4	3	2	1	0
COMP	–	–	–	–	**ETU10**	**ETU9**	**ETU8**

Bit Number	Bit Mnemonic	Description
7	COMP	**Compensation** Clear this bit when no time compensation is needed (i.e. when the ETU to Card CLK period ratio is close to an integer with an error less than 1/4 of Card CLK period). Set this bit otherwise and reduce the ETU period by 1 Card CLK cycle for even bits.
6-3	–	**Reserved** The value read from these bits is indeterminate. Do not change these bits .
2-0	ETU[10:8]	**ETU MSB** Used together with the ETU LSB (see SCETU0 Register).

Reset Value = 0XXX X001b

Dual Data Pointer

T8xC5121 contains a Dual Data Pointer accelerating data memory block moves. The Standard 80C52 Data Pointer is a 16-bit value that is used to address off-chip data RAM or peripherals. In T8xC5121, the standard 16-bit data pointer is called DPTR and located at SFR location 82H and 83H. The second Data Pointer named DPTR1 is located at the same address than the previous one. The DPTR select bit (DPS / bit0) chooses the active pointer and it is located into the AUXR1 register. It should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

The user switches between data pointers by toggling the LSB of the AUXR1. The increment (INC) is a solution for this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual Data Pointer saves code and resources when moves of blocks need to be accomplished.

The second Data Pointer can be used to address the on-chip XRAM.

Table 41. DPL Register

DPL - Low Byte of DPTR1 (82h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 42. DPH Register

DPH - High Byte of DPTR1 (83h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 43. AUXR1 Register

AUXR1 - Dual Pointer Selection Register (A2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data pointer 1** Clear to select DPTR0 as Data Pointer. Set to select DPTR1 as Data Pointer.

Reset value = XXXX XXX0b

Memory Management

Program Memory

All the T8xC5121 versions implement 16 Kbytes of ROM memory, 256 Bytes RAM and 256 Bytes XRAM.

The hardware configuration byte and the split of internal memory spaces depends on the product and is detailed below.

ROM Configuration Byte

Table 44. ROM Configuration Byte Hardware Register

7	6	5	4	3	2	1	0
-	BLJRB	-	-	-	-	-	

Bit Number	Bit Mnemonic	Description
7		**Reserved**
6	BLJRB	**Bootloader Jump RAM Bit** Set to configure User Code in ROM Clear to configure Bootlader in ROM
5-0		**Reserved**

The BLJRB depends of the product version:

- 1: ROM mask version
- 0: EEPROM/CRAM versions

This bit defines if, after reset, either the Customer ROM program or the Bootloader program is executed (for In System programming).

Program ROM Lock Bits

The program Lock system protects the on-chip program against software piracy.

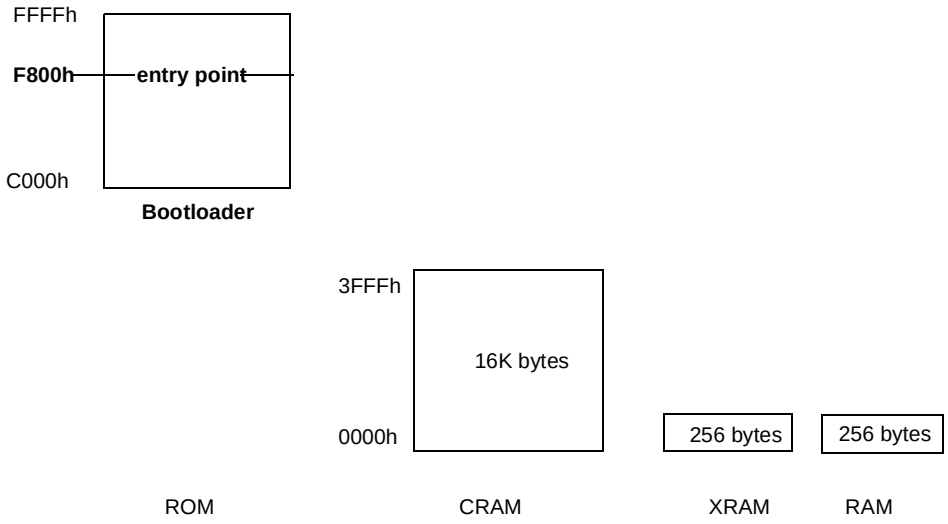
The T8xC5121 products are delivered with the highest protection level.

Table 45. T8xC5121 Products Protection Level

Program Lock Bits			Protection Description
Security Level	LB1	LB2	
3	P	P	**SSOP24 version:** Read function is disabled.But checksum control is still enabled **PLCC52 version:** MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset. But checksum control is still enabled. External execution is possible.

P = Programmed

Figure 25. CRAM and ROM Mappings



T83C5121 with Mask ROM Version

In this version, the customer program is masked in 16 Kbytes ROM.

- The customer program is masked in ROM during the final production phase. The ROM size will be determined at mask generation process depending of the program size.

In-System Programming

The In-System Programming (ISP) mode is only implemented in the following product versions:

- EEPROM version
- CRAM version

(The ROM product version is masked with the customer program and does not need ISP mode)

The ISP is used to download an Application program in the device and to run it.

The communication protocols which are implemented are: UART and TWI.

Hardware Interface

The hardware in relation with the two communication protocols is detailed below:

- TWI protocol
- Serial protocol

Timer 1

Timer 1 is identical to Timer 0 except for Mode 3 which is a hold-count mode. The following comments help to understand the differences:

- Timer 1 functions as either a Timer 0 or an event Counter in the three operating modes. Figure 28 through Figure 30 show the logical configuration for modes 0, 1, and 2. Mode 3 of Timer 1 is a hold-count mode.
- Timer 1 is controlled by the four high-order bits of the TMOD register (see Figure 56) and bits 2, 3, 6 and 7 of the TCON register (see Figure 55). The TMOD register selects the method of Timer 0 gating (GATE1), Timer 0 or Counter operation (C/T1#) and the operating mode (M11 and M01). The TCON register provides Timer 1 control functions: overflow flag (TF1), run control bit (TR1), interrupt flag (IE1) and the interrupt type control bit (IT1).
- Timer 1 can serve as the Baud Rate Generator for the Serial Port. Mode 2 is best suited for this purpose.
- For normal Timer 0 operation (GATE1 = 0), setting TR1 allows TL1 to be incremented by the selected input. Setting GATE1 and TR1 allows external pin $\overline{INT1}$ to control Timer 0 operation.
- Timer 1 overflow (count rolls over from all 1s to all 0s) sets the TF1 flag and generates an interrupt request.
- When Timer 0 is in mode 3, it uses Timer 1's overflow flag (TF1) and run control bit (TR1). For this situation, use Timer 1 only for applications that do not require an interrupt (such as a Baud Rate Generator for the Serial Port) and switch Timer 1 in and out of mode 3 to turn it off and on.
- It is important to stop the Timer 0/Counter before changing modes.

Mode 0 (13-bit Timer 0)

Mode 0 configures Timer 1 as a 13-bit Timer 0, which is set up as an 8-bit Timer 0 (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register (see Figure 28). The upper 3 bits of TL1 register are ignored. Prescaler overflow increments the TH1 register.

Mode 1 (16-bit Timer 0)

Mode 1 configures Timer 1 as a 16-bit Timer 0 with TH1 and TL1 registers connected in cascade (see Figure 29). The selected input increments the TL1 register.

Mode 2 (8-bit Timer 0 with Auto-Reload)

Mode 2 configures Timer 1 as an 8-bit Timer 0 (TL1 register) with automatic reload from the TH1 register on overflow (see Figure 30). TL1 overflow sets the TF1 flag in the TCON register and reloads TL1 with the contents of TH1, which is preset by the software. The reload leaves TH1 unchanged.

Mode 3 (Halt)

Placing Timer 1 in mode 3 causes it to halt and hold its count. This can be used to halt Timer 1 when the TR1 run control bit is not available i.e., when Timer 0 is in mode 3.

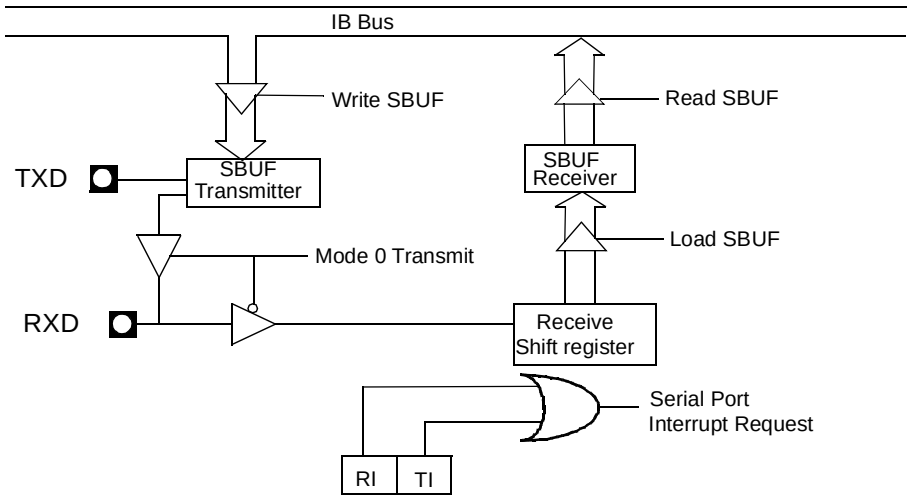
Serial I/O Port

The serial I/O port is entirely compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

Serial I/O port includes the following enhancements:

- Framing error detection and Automatic Address Recognition
- Internal Baud Rate Generator

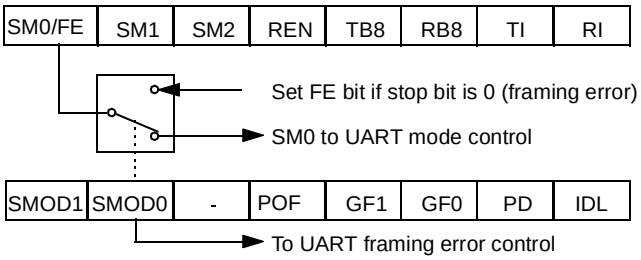
Figure 32. Serial I/O UART Port Block Diagram



Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register.

Figure 33. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 34 and Figure 35).

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.
For example:

SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb

Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b

Slave C:SADDR1111 0011b
SADEN1111 1101b
Given1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).
For slave A, bit 1 is a 0; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves A and B, but not slave C, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't care bits, e.g.:

SADDR0101 0110b
SADEN1111 1100b
SADDR OR SADEN1111 111Xb

The use of don't care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 1X11b,

Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 1X11B,

Slave C:SADDR = 1111 0010b
SADEN1111 1101b
Given1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

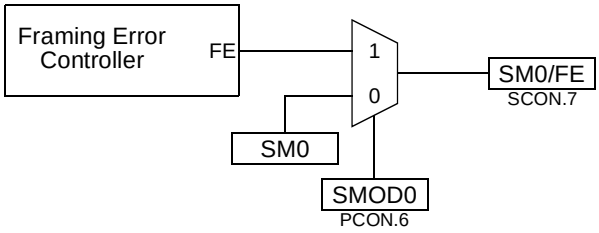
Framing Error Detection (Modes 1, 2 and 3)

Framing error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register as shown in Figure 46.

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two devices. If a valid stop bit is not found, the software sets FE bit in SCON register.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a chip reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When the framing error detection feature is enabled, RI rises on stop bit instead of the last data bit as detailed in Figure 36.

Figure 46. Framing Error Block Diagram



Baud Rate Selection (Modes 1 and 3)

In modes 1 and 3, the Baud Rate is derived either from the Timer 1 or the Internal Baud Rate Generator and allows different baud rate in reception and transmission.

As shown in Figure 47 the selection is done using RBCK and TBCK bits in BDRCON register.

Figure 48 gives the baud rate calculation formulas for each baud rate source while Table 65 details Internal Baud Rate Generator configuration for different peripheral clock frequencies and giving baud rates closer to the standard baud rates.

Figure 47. Baud Rate Source Selection (Modes 1 and 3)

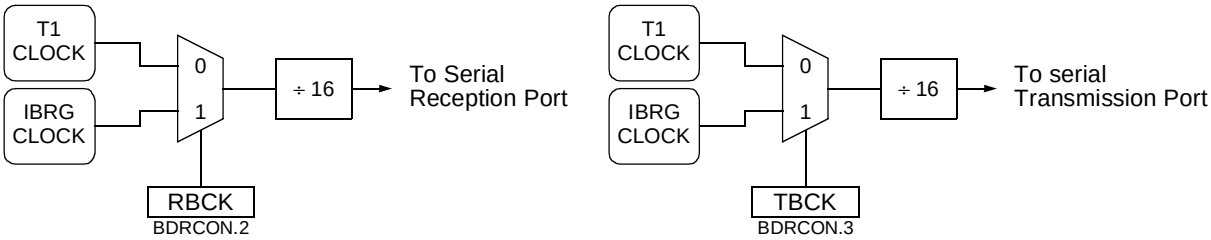


Figure 48. Baud Rate Formulas (Modes 1 and 3)

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot (256 - BRL)}$$

$$BRL = 256 \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot \text{Baud\_Rate}}$$

a. BRG Formula

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6 \cdot 32 \cdot (256 - TH1)}$$

$$TH1 = 256 \frac{2^{SMOD1} \cdot F_{PER}}{192 \cdot \text{Baud\_Rate}}$$

b. T1 Formula

Table 67. SCON Register
SCON (S:98h)
Serial Control Registe

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit** To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.
	SM0	**Serial Port Mode bit 0** To select this function, clear SMOD0 bit in PCON register. Software writes to bits SM0 and SM1 to select the Serial Port operating mode. Refer to SM1 bit for the mode selections.
6	SM1	**Serial Port Mode bit 1** To select this function, set SMOD0 bit in PCON register. Software writes to bits SM1 and SM0 to select the Serial Port operating mode. SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register $F_{OSC}/12$ or variable if SRC bit in BDRCON is set 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{OSC}/32$ or $F_{OSC}/64$ 1 1 3 9-bit UART Variable
5	SM2	**Serial Port Mode bit 2** Software writes to bit SM2 to enable and disable the multiprocessor communication and automatic address recognition features. This allows the Serial Port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN	**Receiver Enable bit** Clear to disable reception in mode 1, 2 and 3, and to enable transmission in mode 0. Set to enable reception in all modes.
3	TB8	**Transmit bit 8** Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.
2	RB8	**Receiver bit 8** Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.
1	TI	**Transmit Interrupt flag** Set by the transmitter after the last data bit is transmitted. Must be cleared by software.
0	RI	**Receive Interrupt flag** Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.

Reset Value = XXX0 0000b

Table 69. SIOCON Register
Serial Input Output Configuration Register
Register (91h)

7	6	5	4	3	2	1	0
PMSOEN1	**PMSOEN0**	**-**	**-**	**CPRES RES**	**EVAUTO**	**VEXT0**	**VEXT1**

Bit Number	Bit Mnemonic	Description
7 - 6	PMOSEN1 PMOSEN0	**Output Enable function on Txd/P3.1 and T0/P3.4:** PMSOEN1 PMSOEN0 0 0 PMOS is always off (reset value) 0 1 PMOS is always driven according to P3.1 or P3.4 value 1 0 PMOS is driven only when OE is high 1 1 PMOS is driven only when OE is low
5 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	CPRES RES	**Card Presence pull-up resistor** 0 Internal pull-up is connected 1 Internal pull-up is disconnected
2	EVAUTO	**EVCC Auto setup** Set to enable the Automatic mode of EV_{CC}regulator Clear to disable the Automatic mode of EV_{CC} regulator
1 - 0	VEXT0 VEXT1	**EVCC voltage configuration:** VEXT0 VEXT1 0 0 Power-down, EV_{CC} is external (reset value) 0 1 EV_{CC} = 1.8V 1 0 EV_{CC} = 2.3V 1 1 EV_{CC} = 2.7V

Reset Value = 00XX 0000b

Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the Watchdog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x $T_{CLK\ PERIPH}$, where $T_{CLK\ PERIPH}= 1/F_{CLK\ PERIPH}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16 ms to 2s @ F_{OSCA} = 12 MHz. To manage this feature, refer to WDTPRG register description, Table 70. The WDTPRG register should be configured before the WDT activation sequence, and can not be modified until next reset.

Table 70. WDTRST Register

WDTRST - Watchdog Reset Register (0A6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 71. WDTPRG Register

WDTPRG - Watchdog Timer Out Register (0A7h)

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is undetermined. Do not try to set this bit.
6	-	
5	-	
4	-	
3	-	
2	S2	**WDT Time-out select bit 2**
1	S1	**WDT Time-out select bit 1**
0	S0	**WDT Time-out select bit 0**
		S2 S1 S0 Selected Time-out 0 0 0 (2^{14} - 1) machine cycles, 16. 3 ms @ F_{OSCA} =12 MHz 0 0 1 (2^{15} - 1) machine cycles, 32.7 ms @ F_{OSCA}=12 MHz 0 1 0 (2^{16} - 1) machine cycles, 65. 5 ms @ F_{OSCA}=12 MHz 0 1 1 (2^{17} - 1) machine cycles, 131 ms @ F_{OSCA}=12 MHz 1 0 0 (2^{18} - 1) machine cycles, 262 ms @ F_{OSCA}=12 MHz 1 0 1 (2^{19} - 1) machine cycles, 542 ms @ F_{OSCA}=12 MHz 1 1 0 (2^{20} - 1) machine cycles, 1.05 ms @ F_{OSCA}=12 MHz 1 1 1 (2^{21} - 1) machine cycles, 2.09 ms @ F_{OSCA}=12 MHz

Reset Value = XXXX X000

WDT during Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the T8xC5121 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is better to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the T8xC5121 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

Table 73. Serial Interface DC parameters (P3.0, P3.1, P3.3 and P3.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5 -0.5 -0.5		0.4 0.5 0.5	V V V	EV_{CC} = 1.8V EV_{CC} = 2.3V EV_{CC} = 2.8V External EVcc Automatic EVcc
V_{IH}	Input High Voltage	1.4 1.6 2.0 0.7 x EV_{CC}	EV_{CC}	2.3 2.8 3.3 EV_{CC} + 0.5	V V V V	EV_{CC} = 1.8V EV_{CC} = 2.3V EV_{CC} = 2.8V External EV_{CC} Automatic EVcc
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.2 mA
V_{OH}	Output High Voltage	1.6 1.8 2.2 0.8 x EV_{CC}		1.8 2.3 2.7 EV_{CC}	V V V V	EV_{CC} = 1.8V I_{OH} = 1 µA EV_{CC} = 2.3V EV_{CC} = 2.8V I_{OH} = 10µA External EV_{CC}
EI_{CC}	Extra Supply Current			+3	mA	C_L = 100 nF
EV_{CC}	Extra Supply Voltage	1.6 2.1 2.6 1.6	1.7 2.2 2.7	1.8 2.3 2.8 V_{CC}	V V V V	C_L = 100 nF, 1.8V C_L = 100 nF, 2.3V C_L = 100 nF, 2.8V External EV_{CC} Automatic EVcc
Ts	Sampling time					Automatic EVcc

Table 74. LED outputs DC Parameters (P3.6 and P3.7)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1 2 5	2 4 10	4 8 20	mA mA mA	2 mA configuration 4 mA configuration 10 mA configuration (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2V ± 20%)