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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	7.3728MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc908fd-112

4. Block diagram

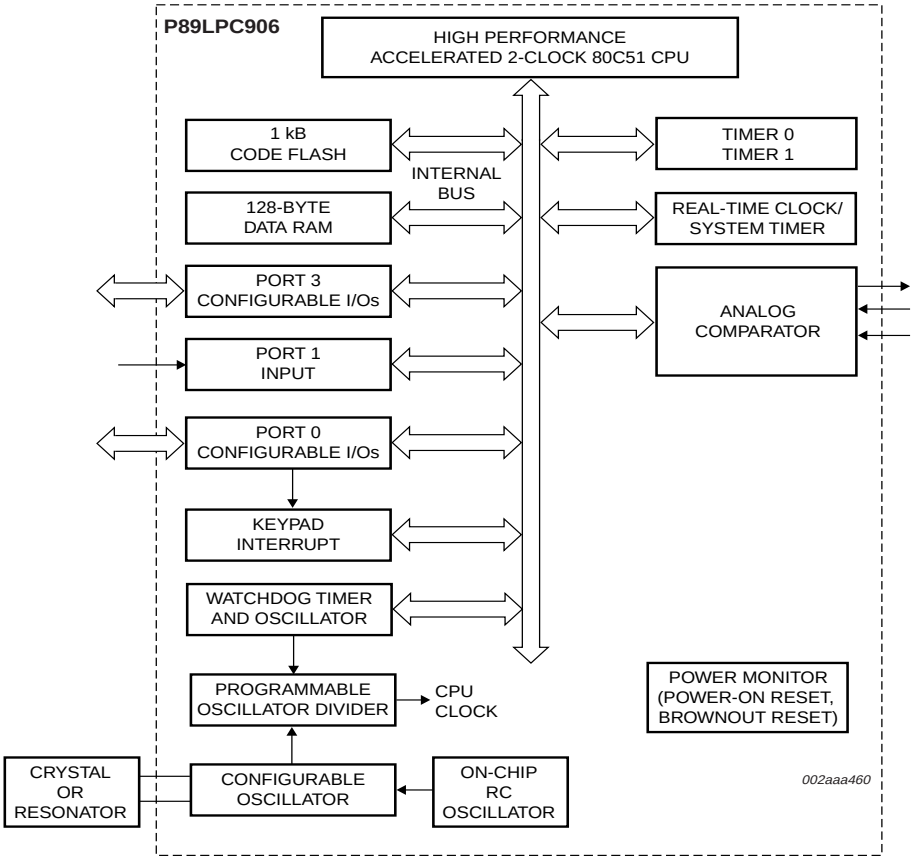

Fig 1. P89LPC906 block diagram.

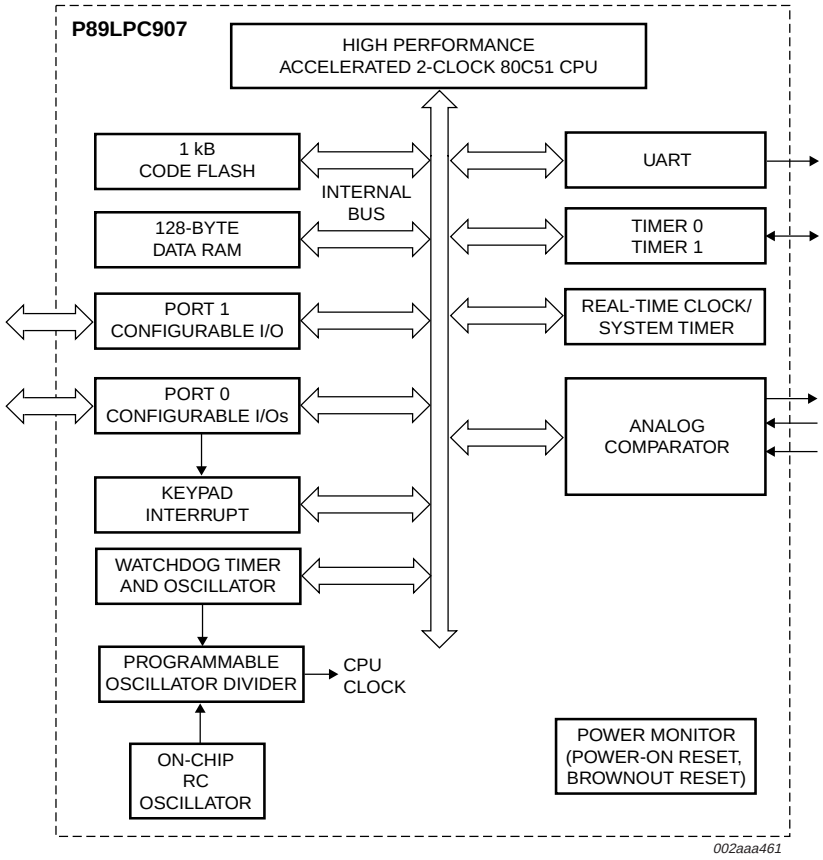

Fig 2. P89LPC907 block diagram.

Table 3: P89LPC906 pin description...*continued*

Symbol	Pin	Type	Description
P3.0 to P3.1		I/O	**Port 3:** Port 3 is an I/O port with a user-configurable output types. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.11.1 "Port configurations" and Table 13 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	5	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK to TRIM.6). It can be used if the CPU clock is the internal RC oscillator, Watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	4	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or Watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V_{SS}	2	I	**Ground:** 0 V reference.
V_{DD}	6	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 4: P89LPC907 pin description

Symbol	Pin	Type	Description
P0.4 to P0.6		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.11.1 "Port configurations" and Table 13 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	8	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator positive input.
		I	**KBI4 —** Keyboard input 4.
	7	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
	3	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.

Table 4: P89LPC907 pin description...*continued*

Symbol	Pin	Type	Description
P1.0 to P1.5			**Port 1:** Port 1 is an I/O port with a user-configurable output types. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.11.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	5	I/O	**P1.0 —** Port 1 bit 0.
		O	**TxD —** Serial port transmitter data.
	4	I/O	**P1.2 —** Port 1 bit 0.
		I/O	**T0 —** Timer 0 external clock input, toggle output, PWM output.
	1	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
V_{SS}	2	I	**Ground:** 0 V reference.
V_{DD}	6	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 5: P89LPC908 pin description

Symbol	Pin	Type	Description
P0.4 to P0.6		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output types. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.11.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	8	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator positive input.
		I	**KBI4 —** Keyboard input 4.
	7	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
	3	I/O	**P0.6 —** Port 0 bit 6.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.

Table 5: P89LPC908 pin description...*continued*

Symbol	Pin	Type	Description
P1.0 to P1.5			**Port 1:** Port 1 is an I/O port with a user-configurable output types. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.11.1 "Port configurations" and Table 13 "DC electrical characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	5	I/O	**P1.0 —** Port 1 bit 0.
		O	**TxD —** Serial port transmitter data.
	4	I/O	**P1.1 —** Port 1 bit 1.
		I	**RxD —** Serial port receiver data.
	1	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
V_{SS}	2	I	**Ground:** 0 V reference.
V_{DD}	6	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

6. Logic symbols

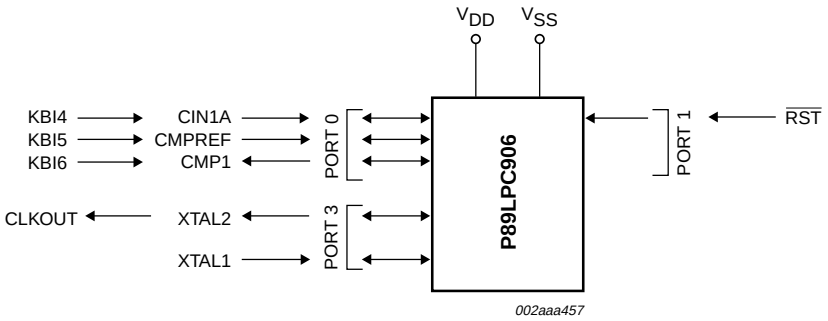

Fig 7. P89LPC906 logic symbol.

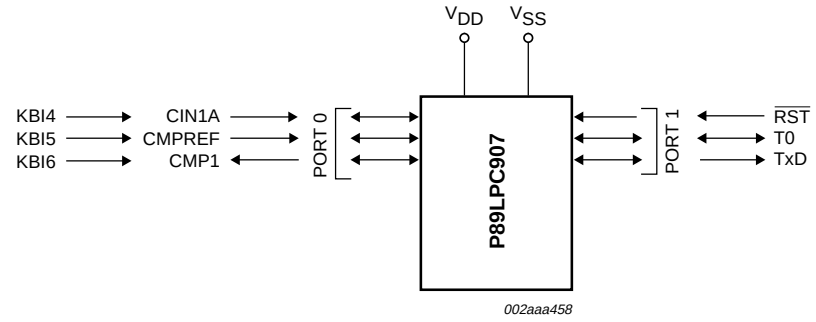

Fig 8. P89LPC907 logic symbol.

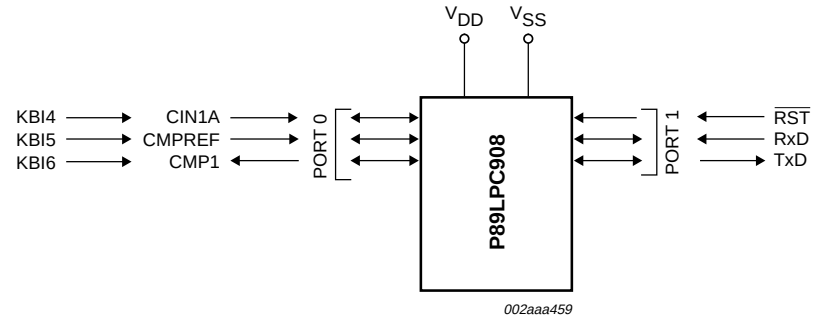

Fig 9. P89LPC908 logic symbol.

Table 6 highlights the differences between these three devices. For a complete list of device features, please see Section 2 “Features” on page 1.

Table 6: Product comparison overview

Type number	External crystal pins	CLKOUT output	T0 PWM output	Analog comparator	UART	
					TxD	Rxd
P89LPC906FD	X	X	-	X	-	-
P89LPC907FD	-	-	X	X	X	-
P89LPC908FD	-	-	-	X	X	X

Table 7: P89LPC906 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	-	-	ENT0	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	00000000
DPL	Data pointer low	82H									00	00000000
FMADRH	Program Flash address high	E7H									00	00000000
FMADRL	Program Flash address low	E6H									00	00000000
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	-	ET1	-	ET0	-	00	00000000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	-	-	-	-	EC	EKBI	-	00[1]	00x00000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0	-	00[1]	x0000000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H	-	00[1]	x0000000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	-	-	-	-	PC	PKBI	-	00[1]	00x00000
IP1H	Interrupt priority 1 high	F7H	-	-	-	-	-	PCH	PKBIH	-	00[1]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00

Table 8: P89LPC907 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	-	PCH	PKBIH	-	00[1]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	-	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	-	KB2	-	KB0	[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	T0	-	TxD		
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	-	(P0M1.6)	(P0M1.5)	(P0M1.4)	-	(P0M1.2)	-	(P0M1.0)	FF	11111111
P0M2	Port 0 output mode 2	85H	-	(P0M2.6)	(P0M2.5)	(P0M2.4)	-	(P0M2.2)	-	(P0M2.0)	00	00000000
P1M1	Port 1 output mode 1	91H	-	-	(P1M1.5)	-	-	(P1M1.2)	-	(P1M1.0)	FF[1]	11111111
P1M2	Port 1 output mode 2	92H	-	-	(P1M2.5)	-	-	(P1M2.2)	-	(P1M2.0)	00[1]	00000000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD		VCPD			-	SPD		00[1]	00000000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	-	-	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1] [6]	011xxx00
RTCH	Real-time clock register high	D2H									00[6]	00000000
RTCL	Real-time clock register low	D3H									00[6]	00000000
SBUF	Serial port data buffer register	99H									xx	xxxxxxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0	SM1	SM2		TB8		TI		00	00000000

Table 8: P89LPC907 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL					00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	00000000
TH0	Timer 0 high	8CH									00	00000000
TH1	Timer 1 high	8DH									00	00000000
TL0	Timer 0 low	8AH									00	00000000
TL1	Timer 1 low	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	-	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.

Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

[3] The RSTSRC register reflects the cause of the P89LPC906/907/908 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after Watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

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Table 9: P89LPC908 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	-	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate low	BEH									00	00000000
BRGR1[2]	Baud rate generator rate high	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	00000000
DPL	Data pointer low	82H									00	00000000
FMADRH	Program Flash address high	E7H									00	00000000
FMADRL	Program Flash address low	E6H									00	00000000
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	00000000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	-	EC	EKBI	-	00[1]	00x00000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x0000000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x0000000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	-	PC	PKBI	-	00[1]	00x00000

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8. Functional description

Remark: Please refer to the *P89LPC906/907/908 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC906/907/908 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC906/907/908 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of the clock sources (see Figure 10 and 11) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU CLOCK (CCLK) modification: DIVM register").

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC906/907/908 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip Watchdog oscillator and an on-chip RC oscillator.

The P89LPC906, in addition, includes an option for an oscillator using an external crystal or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option (P89LPC906)

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option (P89LPC906)

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option (P89LPC906)

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An**

8.11.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC906/907/908 are 3 V devices, however, the pins are 5 V-tolerant (except for XTAL1 and XTAL2). In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.11.6 Port 0 analog functions

The P89LPC906/907/908 incorporates an Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in Section 8.11.4 “Input-only configuration”.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to ‘0’s to enable digital functions.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1. This option must be used for an oscillator frequency above 12 MHz (P89LPC906).)
- Power-on detect
- Brownout detect
- Watchdog Timer
- Software reset
- UART break character detect reset (P89LPC908).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.15 Timers/counters 0 and 1

The P89LPC906/907/908 has two general purpose timers which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different. And additional PWM output mode, Mode 6, is provided on the P89LPC907.

8.15.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.15.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.15.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.15.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator for the P89LPC907 and P89LPC908.

8.15.5 Mode 6 (P89LPC907)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.15.6 Timer overflow toggle output (P89LPC907)

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.16 Real-Time clock/system timer

The P89LPC906/907/908 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.17 UART (P89LPC908)

The P89LPC907 and P89LPC908 devices have an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC907 does not have an RxD pin and thus receiver functions described in this section do not apply to the P89LPC907. Both devices include an independent Baud Rate Generator. The baud rate can be selected from the OSCCLK (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CCLK/32 or CCLK/16.

8.17.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

8.17.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), and a stop bit (logical ‘1’). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.17.5 “Baud rate generator and selection”).

8.17.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = '0'), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = '0').

8.17.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.17.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.18 Analog comparator

An analog comparator is provided on the P89LPC906/907/908. Comparator operation is such that the output is a logical one (which may be read in a register) when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be configured to cause an interrupt when the output value changes.

The connections to the comparator are shown in Figure 16. The comparator functions to V_{DD} = 2.4 V.

When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

8.19 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ±10 %.

8.20 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

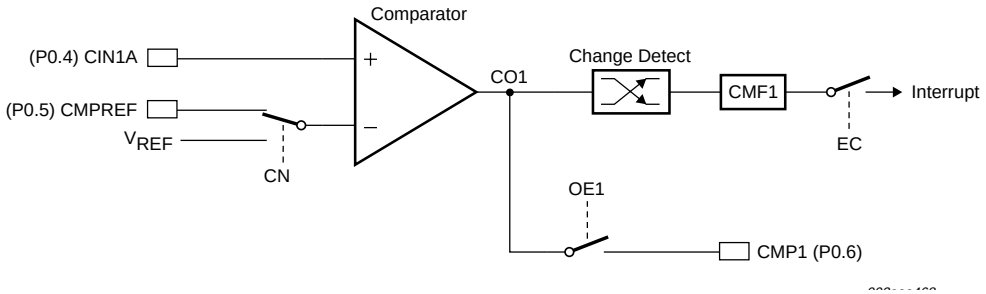

Fig 16. Comparator input and output connections.

8.21 Comparator and power reduction modes

The comparator may remain enabled when Power-down or Idle mode is activated, but the comparator is disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor.

If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.22 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt

data interface using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 KB of user code space.

8.25.5 In-circuit programming (ICP)

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC906/907/908 through a two-wire serial interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector (with V_{DD}, V_{SS}, RST, clock, and data signals) needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC906/907/908 User's Manual*.

8.25.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP-Lite facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming Lite has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC906/907/908 User's Manual*.

8.25.7 Using flash as data storage

The Flash code memory array of this device supports **individual** byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.25.8 User configuration bytes

Some user-configurable features of the P89LPC906/907/908 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC906/907/908 User's Manual* for additional details.

8.25.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC906/907/908 User's Manual* for additional details.

11. Dynamic characteristics

Table 14: AC characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal f = 7.3728 MHz) trimmed to ±1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal f = 400 kHz)		320	520	320	520	kHz
Crystal oscillator (P89LPC906)							
f_{osc}	oscillator frequency		0	12	-	-	MHz
t_{CLCL}	clock cycle	see Figure 19	83	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock (P89LPC906)							
t_{CHCX}	HIGH time	see Figure 19	33	$t_{CLCL} - t_{CLCX}$	33	-	ns
t_{CLCX}	LOW time	see Figure 19	33	$t_{CLCL} - t_{CHCX}$	33	-	ns
t_{CLCH}	rise time	see Figure 19	-	8	-	8	ns
t_{CHCL}	fall time	see Figure 19	-	8	-	8	ns
Shift register (UART mode 0 - P89LPC908)							
t_{XLXL}	serial port clock cycle time	see Figure 18	16 t_{CLCL}	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 18	13 t_{CLCL}	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 18	-	t_{CLCL} + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 18	-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge	see Figure 18	150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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