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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	120
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-128-120-15yi-1

Table 2. MACH 5 Speed Grades

Device	Speed Grade ¹						
	-5	-6	-7	-10	-12	-15	-20
M5-128 ²			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C, I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256 ²			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	C, I	I

Note:

1. C = Commercial grade, I = Industrial grade
2. /1 version recommended for new designs

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL[®] block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options ¹

	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
	5	3.3		5	3.3	5	3.3	5	3.3	5	3.3
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

Note:

1. The I/O options indicated with a "*" are obsolete, please contact factory for more information.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued.
See Ordering Information section for product status.

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

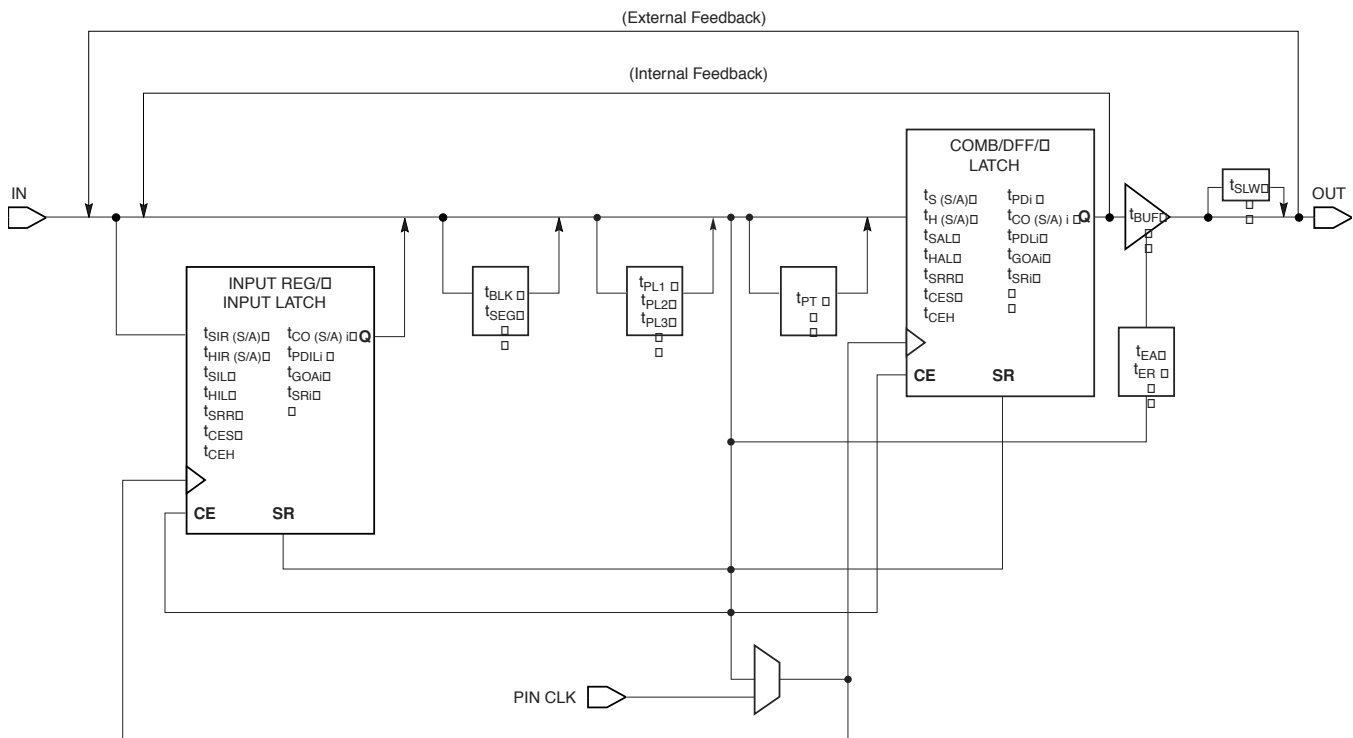


Figure 7. MACH 5 Timing Model

20446G-014

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SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

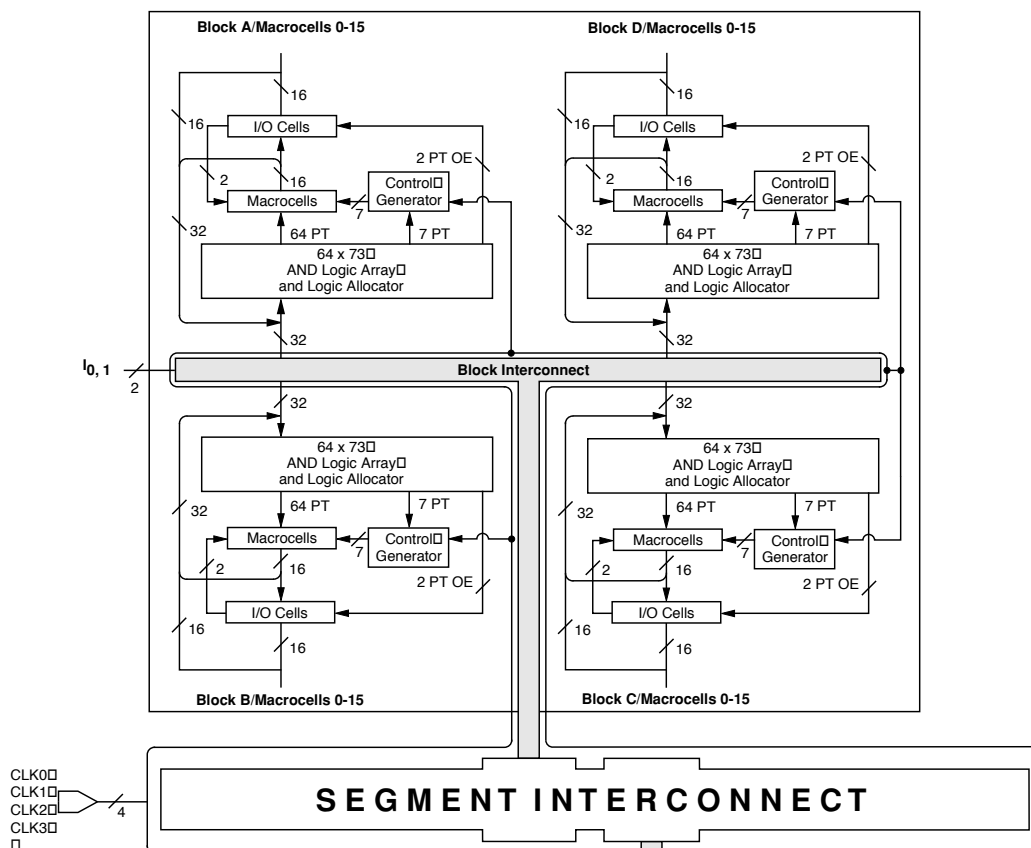
POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

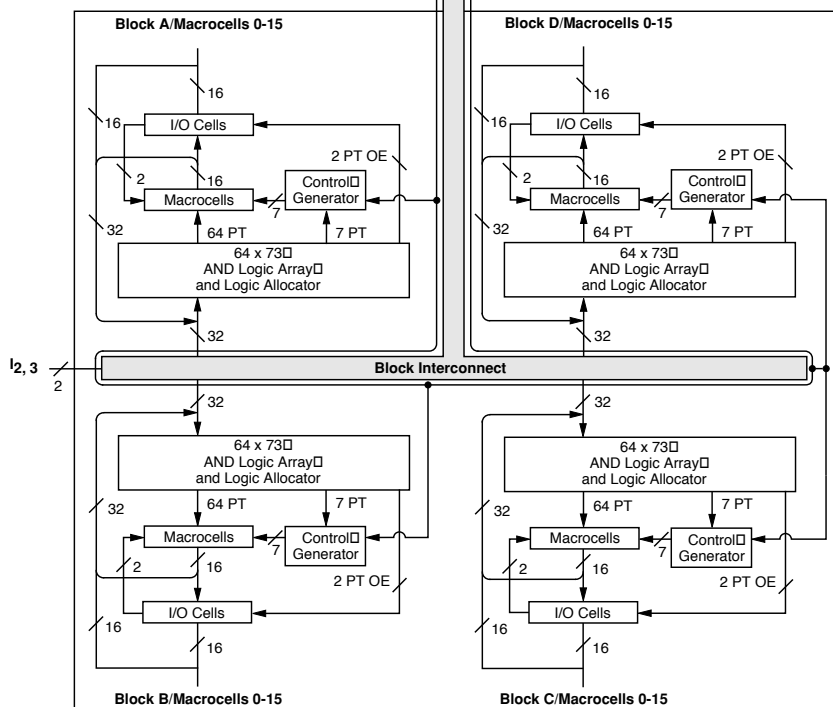
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See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0



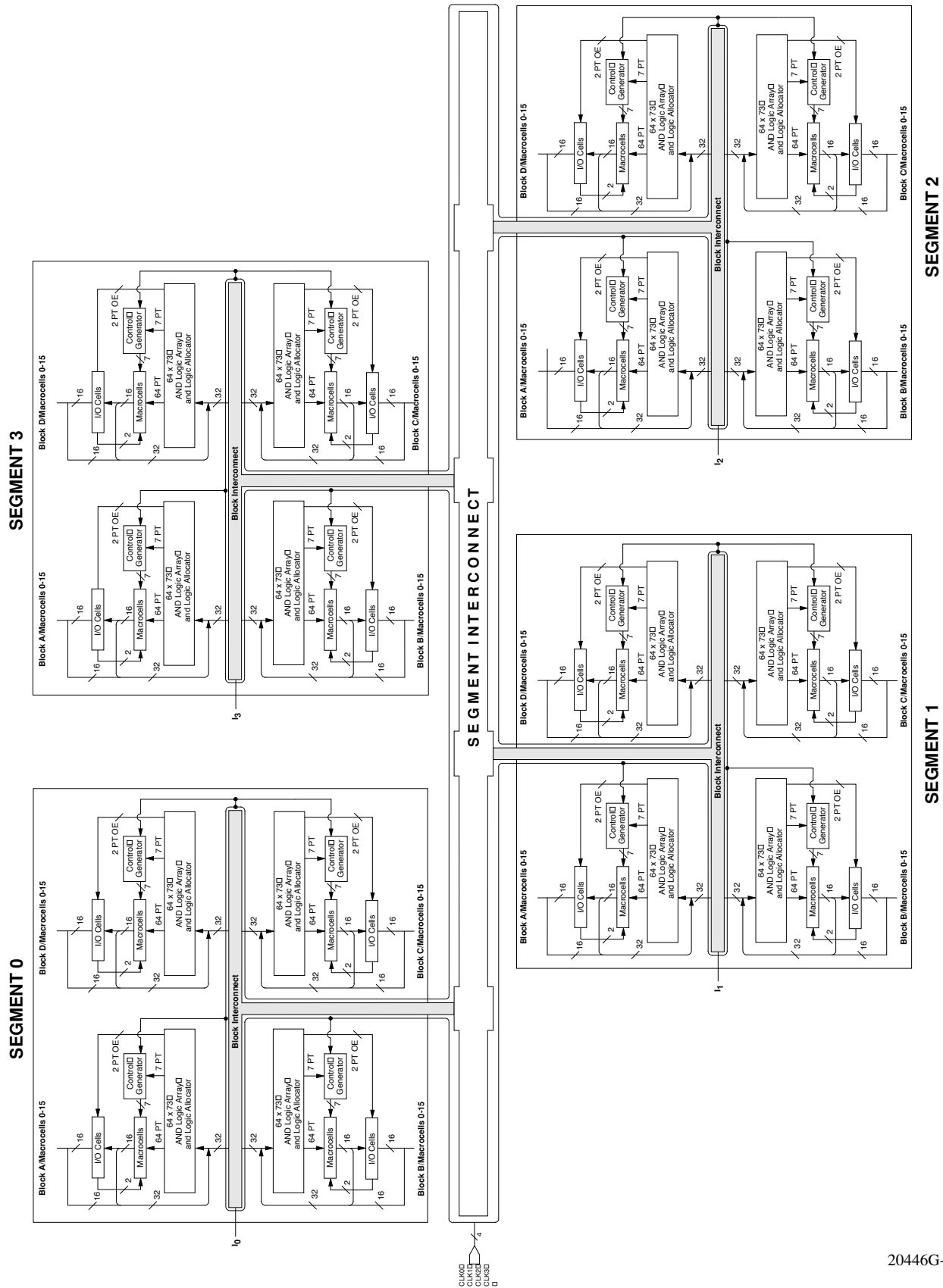
SEGMENT 1



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20446G-007

BLOCK DIAGRAM — M5(LV)-256/XXX



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20446G-009

ABSOLUTE MAXIMUM RATINGS

M5

Storage Temperature. -65°C to +150°C
 Device Junction
 Temperature (Note 1) +130°C or +150°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued.
See Ordering Information section for product status.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = -100 \mu\text{A}$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$		3.3	3.6	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = -2.5 \text{ mA}$, $V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	$I_{OL} = +16 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$, $V_{CC} = \text{Max}$ (Note 4)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$, $V_{CC} = \text{Max}$ (Note 4)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}$, $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 5)	-30		-180	mA

Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.
- Total I_{OL} between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																
t _{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0		18.0	ns
t _{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:																
t _{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		10.0		ns
t _{SA}	Asynchronous clock setup time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{COsi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0		10.0	ns
t _{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0		12.0	ns
t _{COAi}	Asynchronous clock to internal output		6.0		6.0		8.0		10.0		13.0		15.0		18.0	ns
t _{COA}	Asynchronous clock to output		8.0		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:																
t _{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0		10.0	ns
t _{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0		12.0	ns
t _{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0		12.0	ns
t _{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:																
t _{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		4.0		ns
t _{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:																
t _{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
t _{PDILi}	Transparent input latch		5.0		5.0		5.5		6.0		6.0		6.0		6.0	ns
Output Delays:																
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns
t _{ER}	Output disable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns

Select devices have been discontinued.
See Ordering Information section for product status.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Delays:																
t _{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t _{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t _{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t _{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t _{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t _{SRI}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t _{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t _{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

Select devices have been discontinued.
See Ordering Information section for product status.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																
f _{MAX}	External feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{HS})	200		167		167		125		100		83.3		83.3		MHz
f _{MAXA}	External feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{HA})	167		125		125		100		83.3		71.4		62.5		MHz
f _{MAXI}	Maximum input register frequency 1/(t _{SIRS} + t _{HIRS}) or 1/(2 x t _{WICW})	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).

Select devices have been discontinued.
See Ordering Information section for product status.

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	$V_{IN} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	$V_{OUT} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

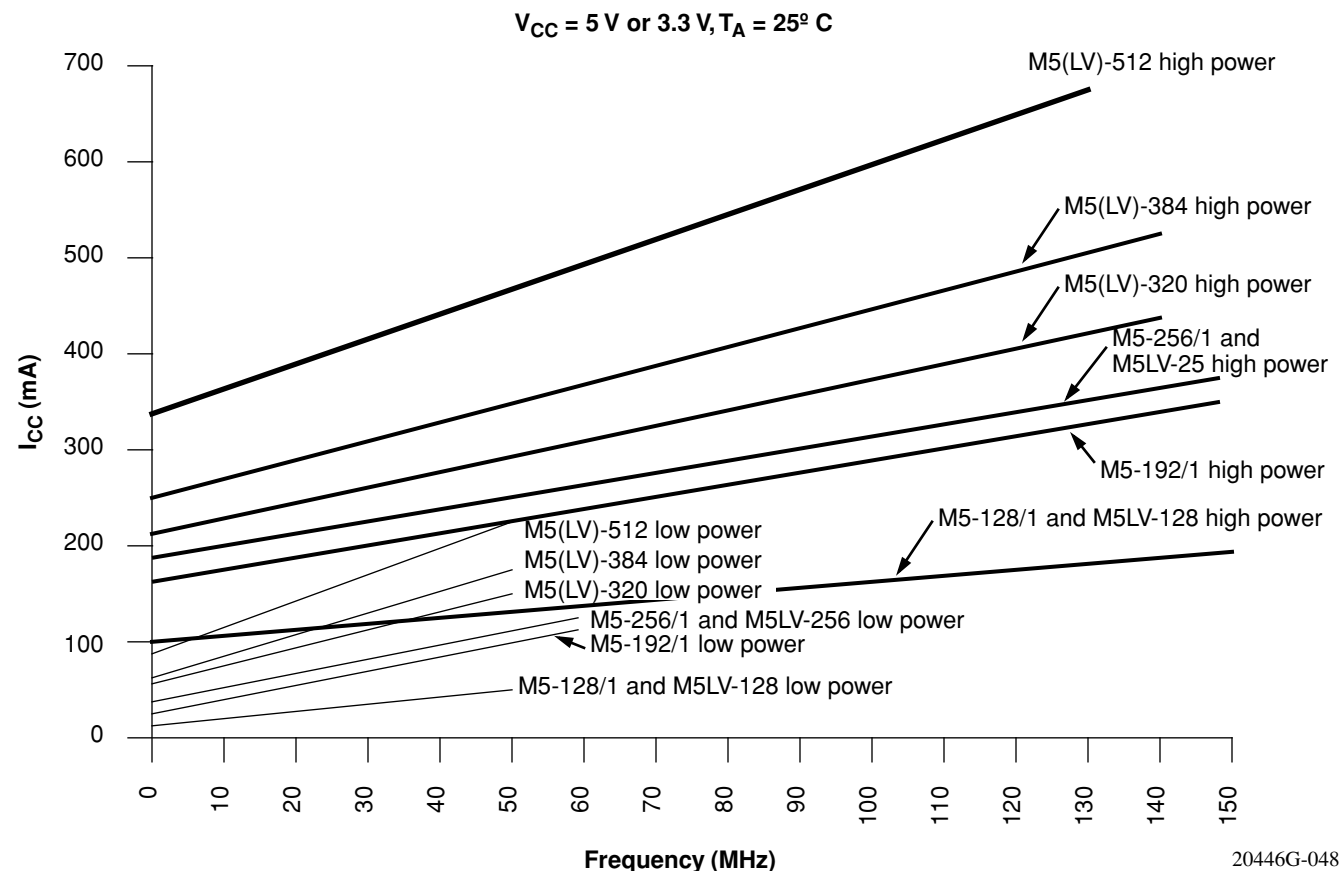


Figure 8. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

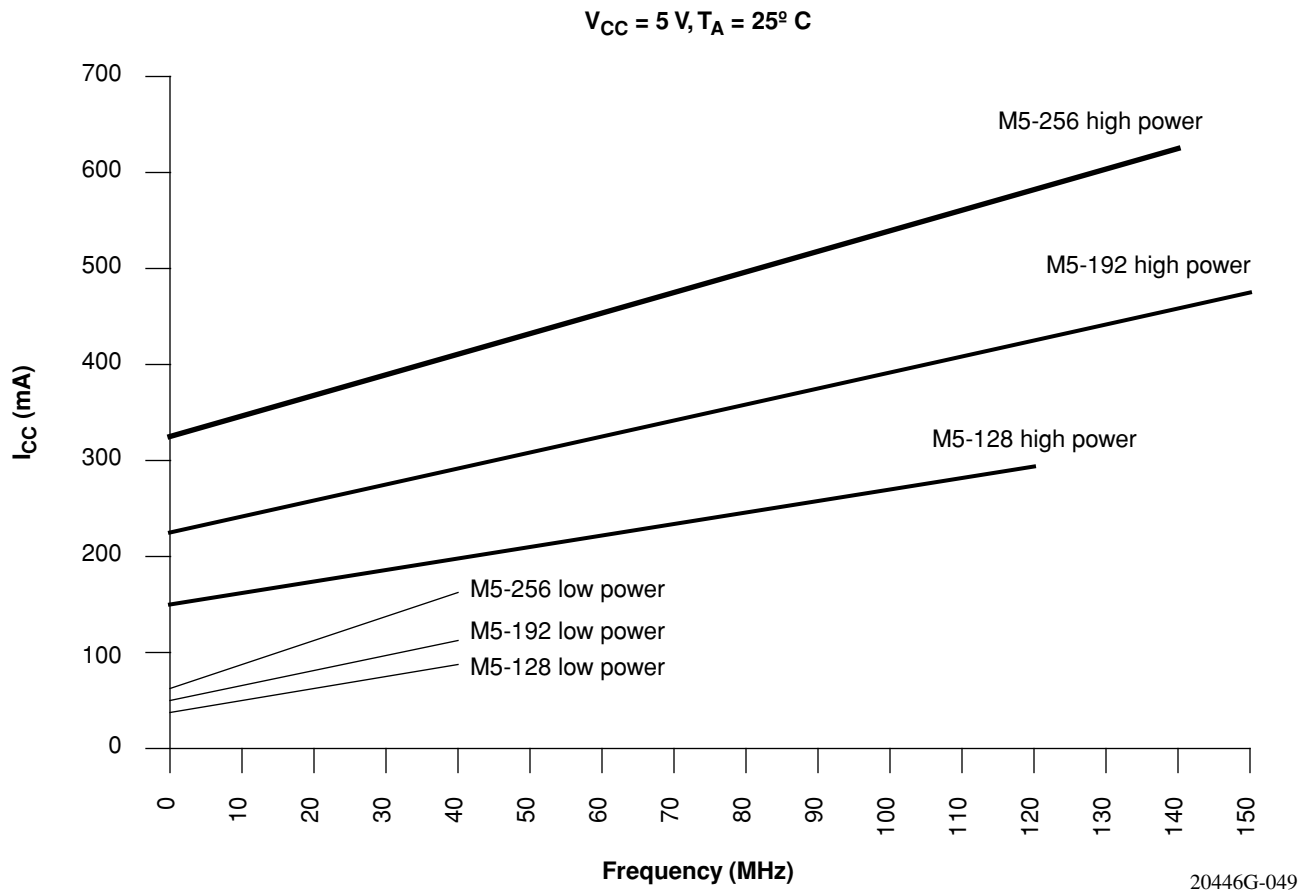


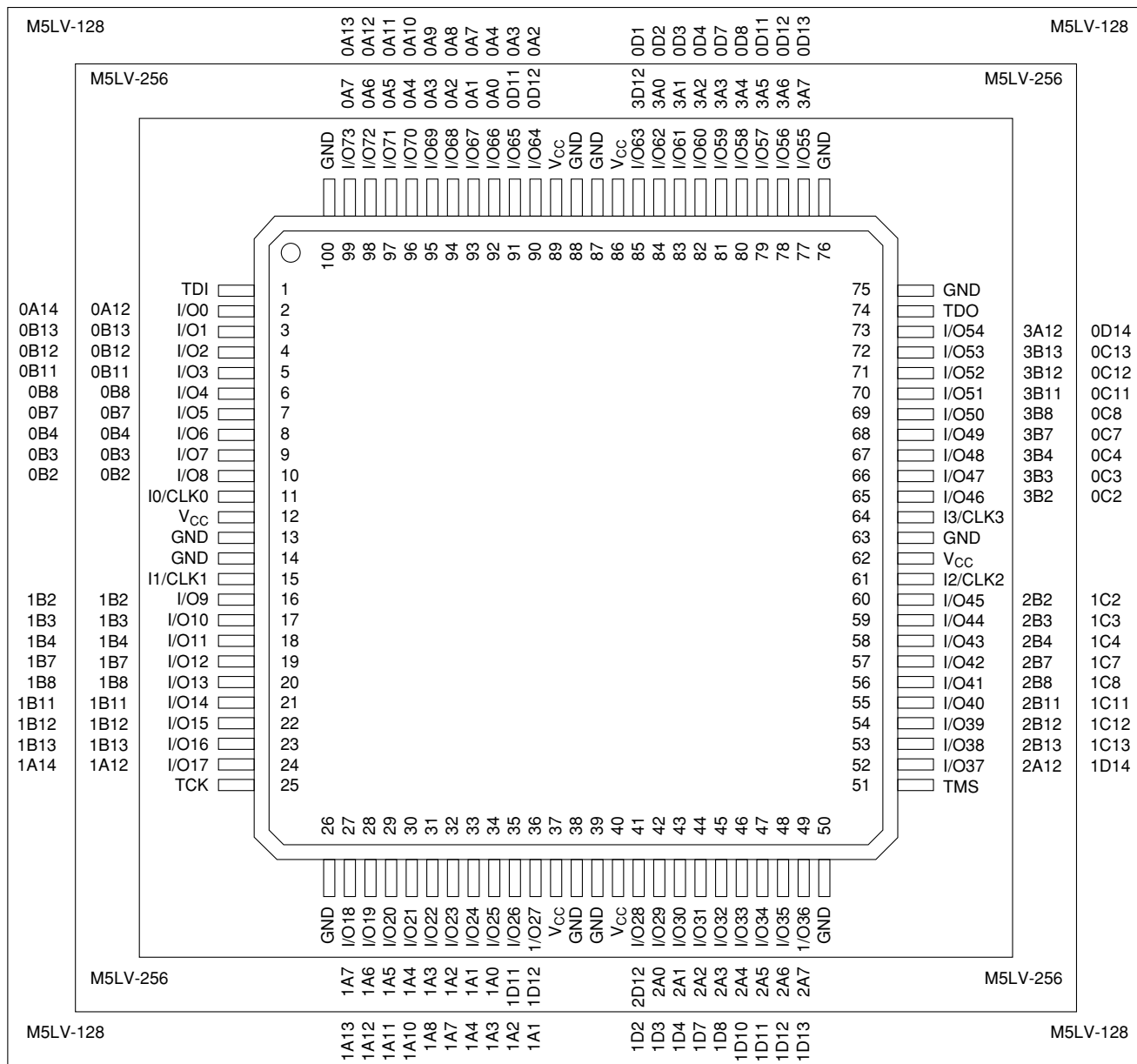
Figure 9. I_{CC} Curves at High/Low Power Modes

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100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)



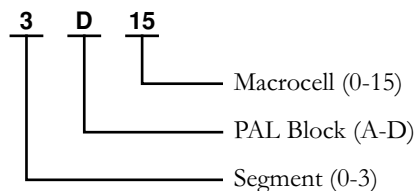
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-018

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

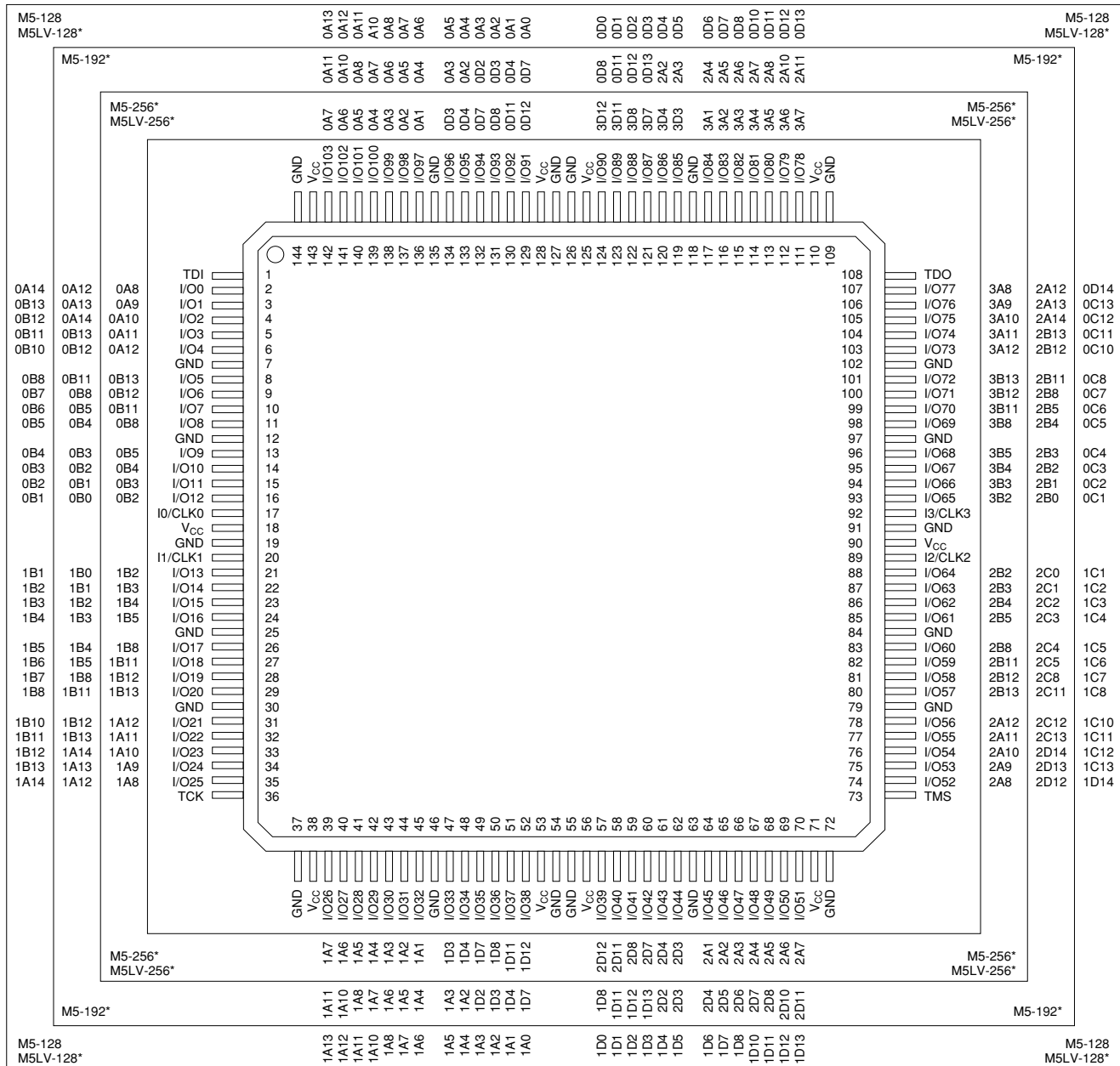
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



144-PIN PQFP CONNECTION DIAGRAM

Top View

144-Pin PQFP



Select devices have been discontinued.
See Ordering Information section for product status.

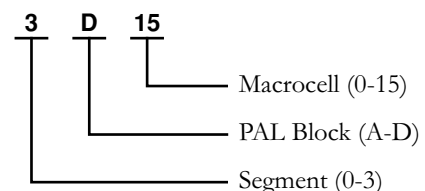
*Package obsolete, contact factory.

20446G-019

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

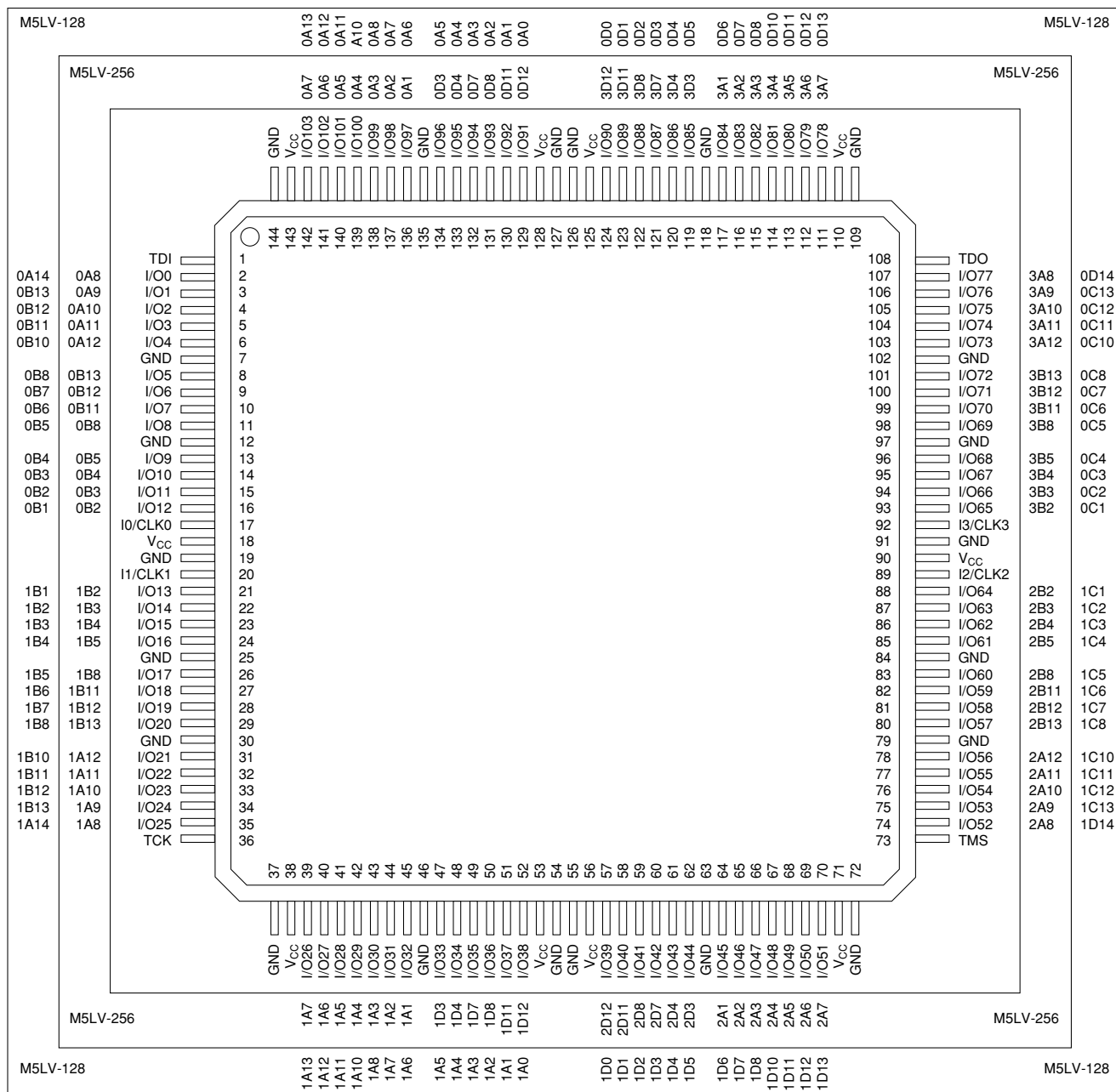
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



144-PIN TQFP CONNECTION DIAGRAM

Top View

144-Pin TQFP



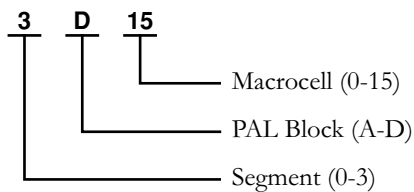
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-020

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

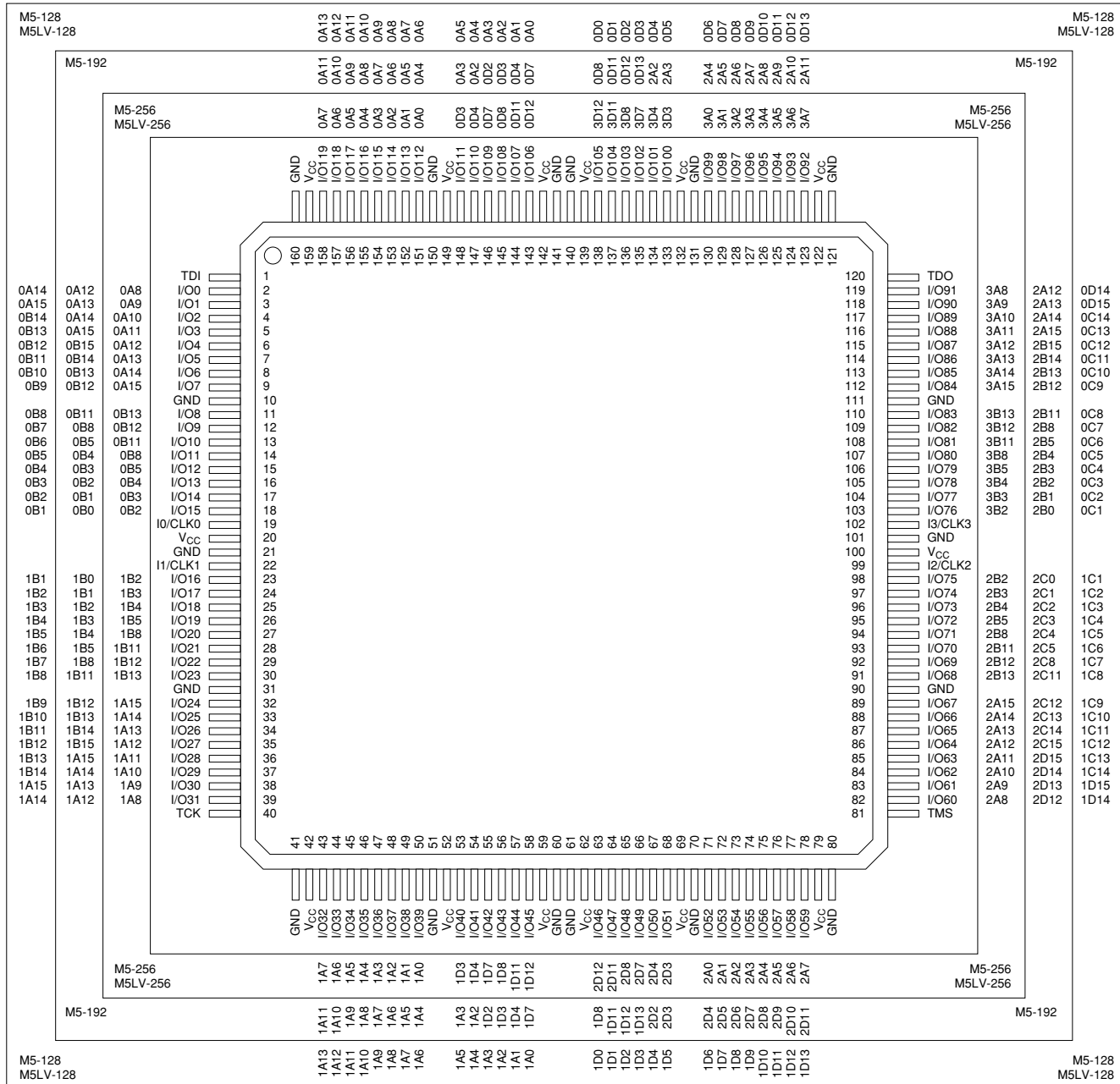


160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

Select devices have been discontinued.
See Ordering Information section for product status.

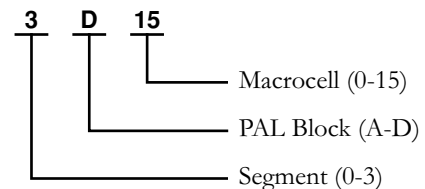


20446G-021

Pin Designations

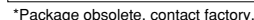
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



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160-Pin PQFP (320, 384, 512 Macrocells)

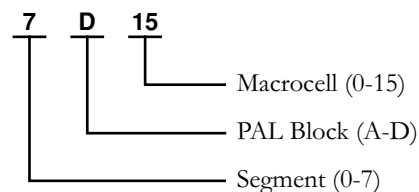


**Select devices have been discontinued.
See Ordering Information section for product status.**

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

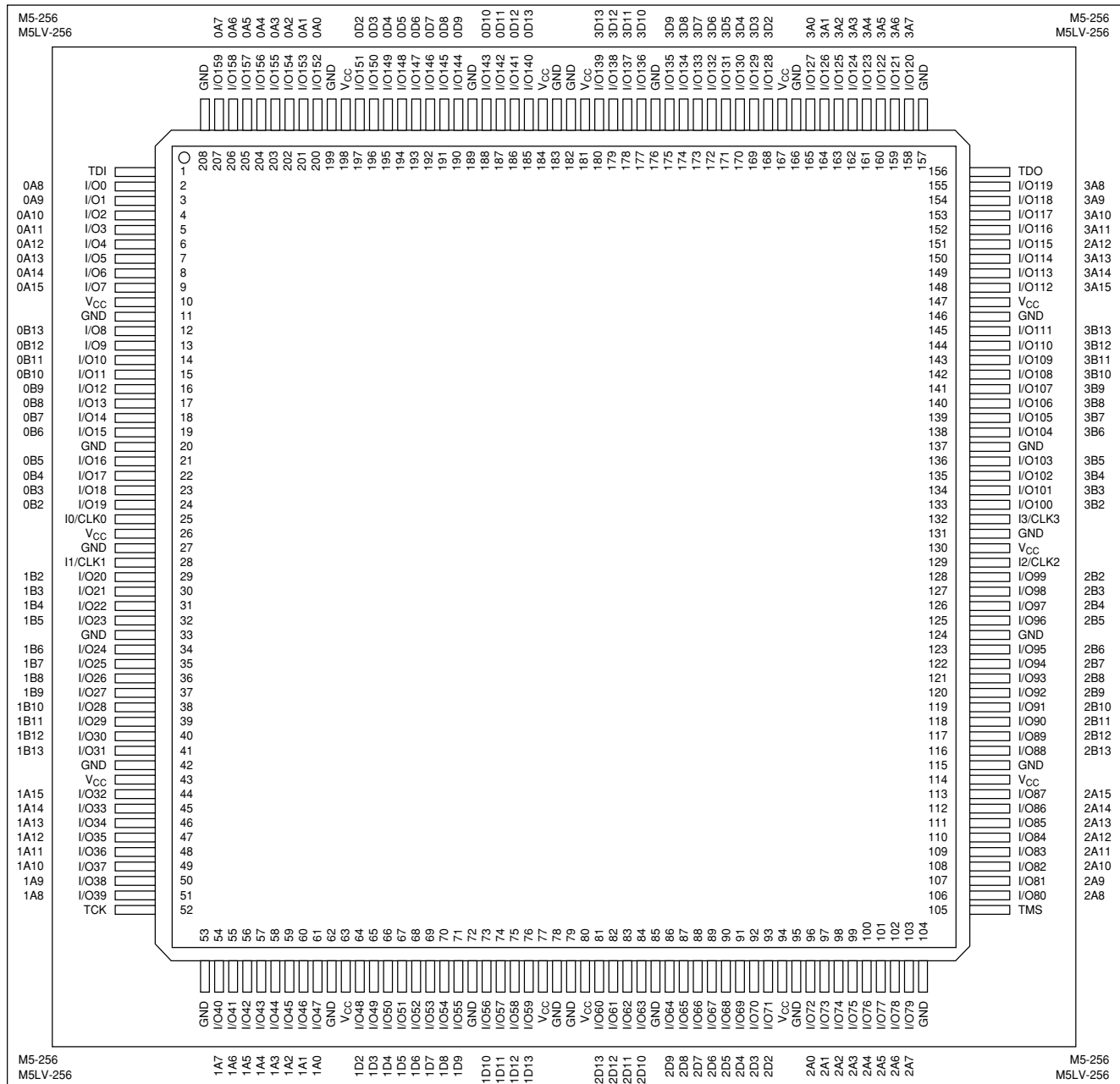
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (256 Macrocells)



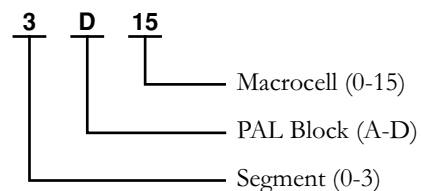
**Select devices have been discontinued.
See Ordering Information section for product status.**

20446G-023

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (Macrocell Association)

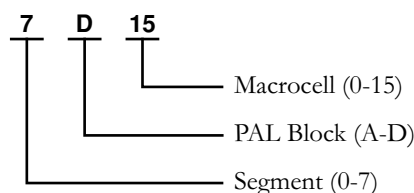
352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF			
1	NC	NC	NC	GND	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A14	3A15	3A13	3A12		
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D1	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	NC	NC		
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I ₂ /CLK ₂	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	NC		
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A14	3A15	3A13	3A12		
5	GND	6A12	6A13	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 7 D 15 Segment (0-7) Macrocell (0-15) PAL Block (A-D)	6A15	6A11	6A7	6A3	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0
6	NC	6A9	6A10	6A15		6A11	6A7	6A3	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0	
7	GND	6A6	6A8	6A11		6A7	6A3	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0		
8	6A1	6A4	6A5	6A7		6A3	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0			
9	6B1	6A0	6A2	6A3		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
10	GND	6B2	6B0	V _{CC}		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
11	6B6	6B5	6B4	6B3		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
12	6B10	6B9	6B8	6B7		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
13	6B14	6B13	6B12	6B11		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
14	GND	7B15	6B15	V _{CC}		6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0				
15	7B14	7B13	7B12	7B11	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
16	NC	7B10	7B9	7B8	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
17	7B7	7B6	7B5	7B4	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
18	GND	7B3	7B2	V _{CC}	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
19	7B1	7B0	7A1	7A4	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
20	7A0	7A2	7A3	7A8	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
21	7A5	7A6	7A7	7A12	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
22	GND	7A9	7A11	7A15	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
23	7A10	7A13	7A14	V _{CC}	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
24	NC	NC	TDI	0A2	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
25	GND	GND	0A1	0A3	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					
26	NC	NC	GND	0A6	6B6	6B10	6B14	GND	7B14	NC	7B7	GND	7B1	7A0	7A5	GND	7A10	NC	GND	0A1	0A3	0A8	0A5	0A0					

20446G-031

Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



20446G-031

Select devices have been discontinued.
See Ordering Information section for product status.

3.3V M5LV ORDERING INFORMATION¹

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68	Industrial: -7, -10, -12, -15	YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15	YC, YI
M5LV-320/160		YC, YI
M5LV-384/120		YC, YI
M5LV-384/160		YC, YI
M5LV-512/120	Industrial: -10, -12, -15, -20	YC, YI
M5LV-512/160		YC, YI
M5LV-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.