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### **Understanding Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### **Applications of Embedded - CPLDs**

#### **Details**

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	120
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-128-120-7yi-1">https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-128-120-7yi-1</a>

Table 1. MACH 5 Device Features <sup>1</sup>

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	160	160	160	256	256
t <sub>PD</sub> (ns)	5.5	5.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	6.5	6.5
t <sub>SS</sub> (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t <sub>COS</sub> (ns)	4.5	4.5	4.5	4.5	4.5	5.0	5.0	5.0	5.0	5.0	5.0
f <sub>CNT</sub> (MHz)	182	182	182	182	182	167	167	167	167	167	167
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

**Note:**

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

## GENERAL DESCRIPTION

The MACH<sup>®</sup> 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E<sup>2</sup>CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued. See Ordering Information section for product status.

Table 2. MACH 5 Speed Grades

Device	Speed Grade <sup>1</sup>						
	-5	-6	-7	-10	-12	-15	-20
M5-128 <sup>2</sup>			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C, I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256 <sup>2</sup>			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	C, I	I

**Note:**

1. C = Commercial grade, I = Industrial grade
2. /1 version recommended for new designs

With Lattice’s unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL<sup>®</sup> block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options <sup>1</sup>

Supply Voltage	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

**Note:**

1. The I/O options indicated with a “\*” are obsolete, please contact factory for more information.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today’s complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued. See Ordering Information section for product status.

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.

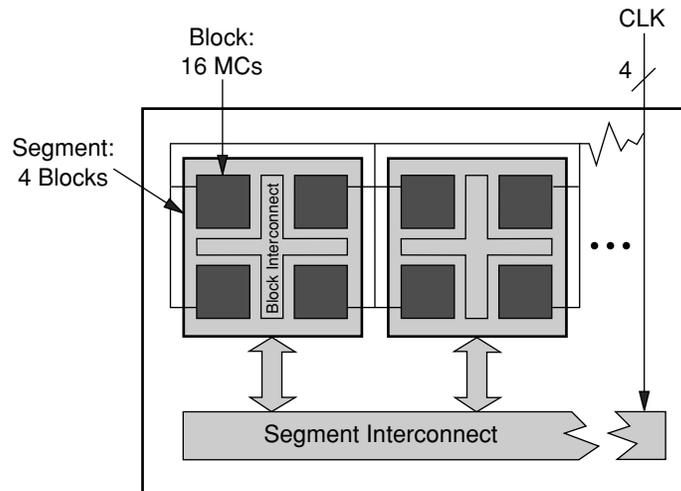


Figure 1. MACH 5 Block Diagram

20446G-001

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Select devices have been discontinued. See Ordering Information section for product status.

## Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.

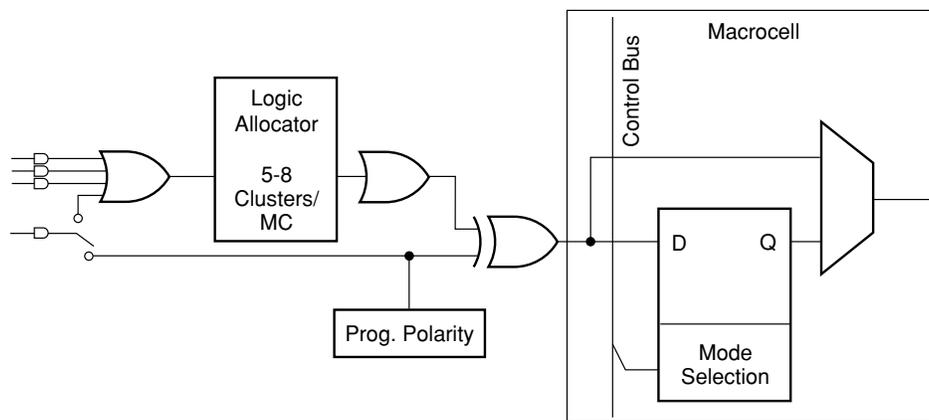


Figure 3. Macrocell Diagram

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## Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

### Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ( $A*B*C$ )
- ◆ Sum-term clock ( $A+B+C$ )

### Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.  
See Ordering Information section for product status.

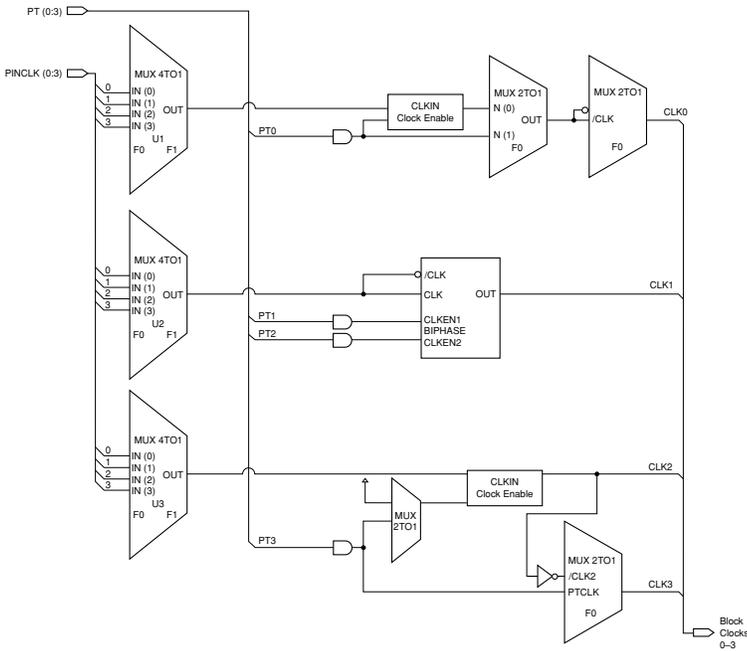
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

**Clock Line 2 Options**

- ◆ Global clock (0, 1, 2, or 3) with clock enable

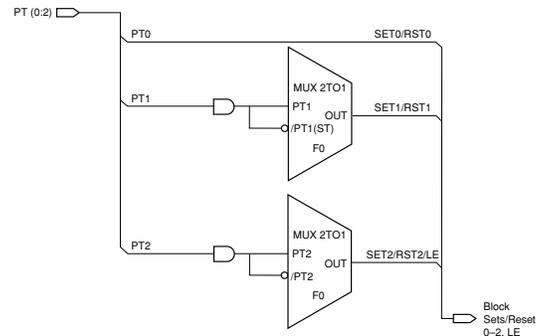
**Clock Line 3 Options**

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

**Figure 4. Clock Generator**



20446G-005

**Figure 5. Set/Reset Generator**

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued. See Ordering Information section for product status.**



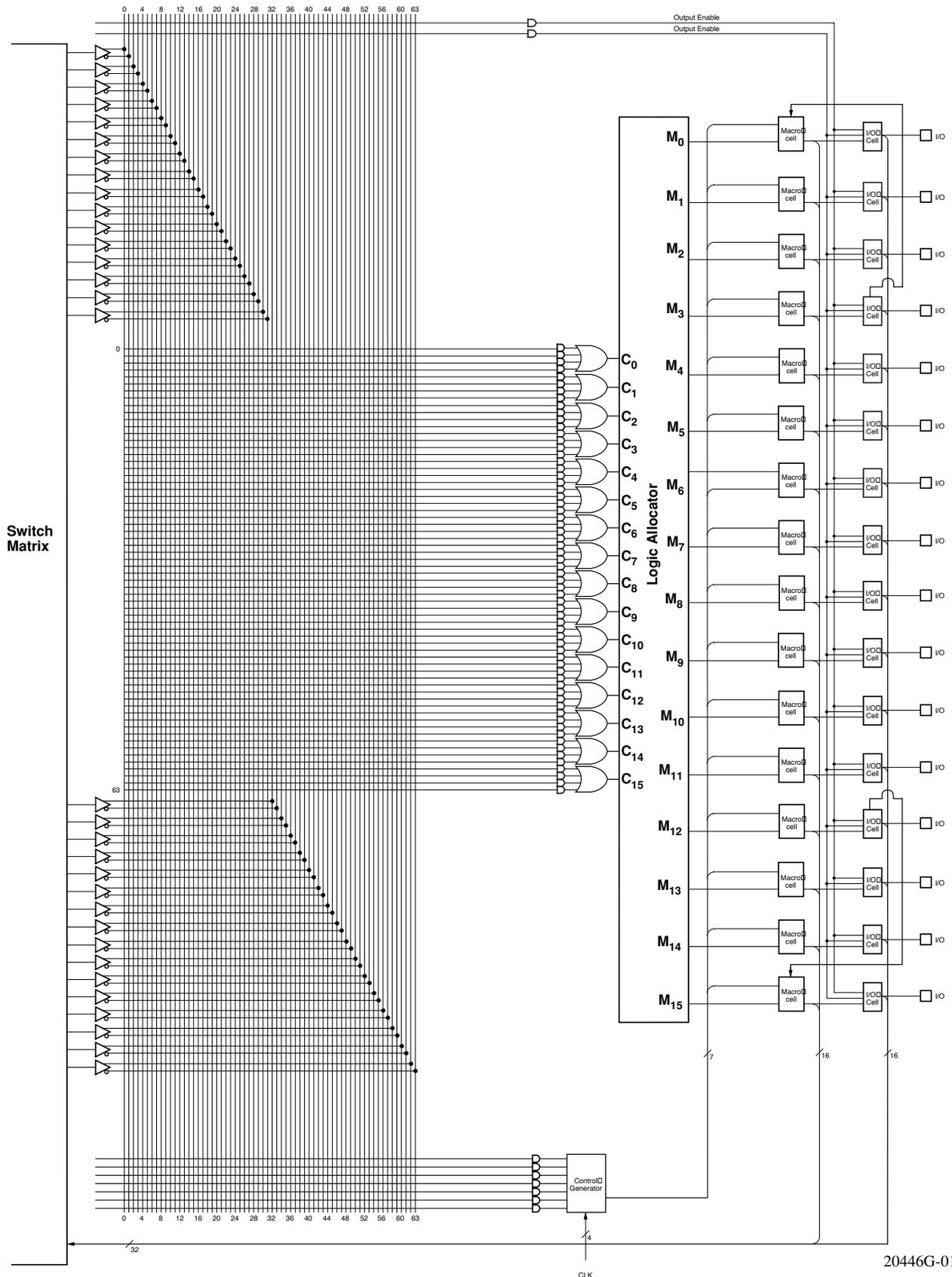
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## SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

**Select devices have been discontinued.  
See Ordering Information section for product status.**

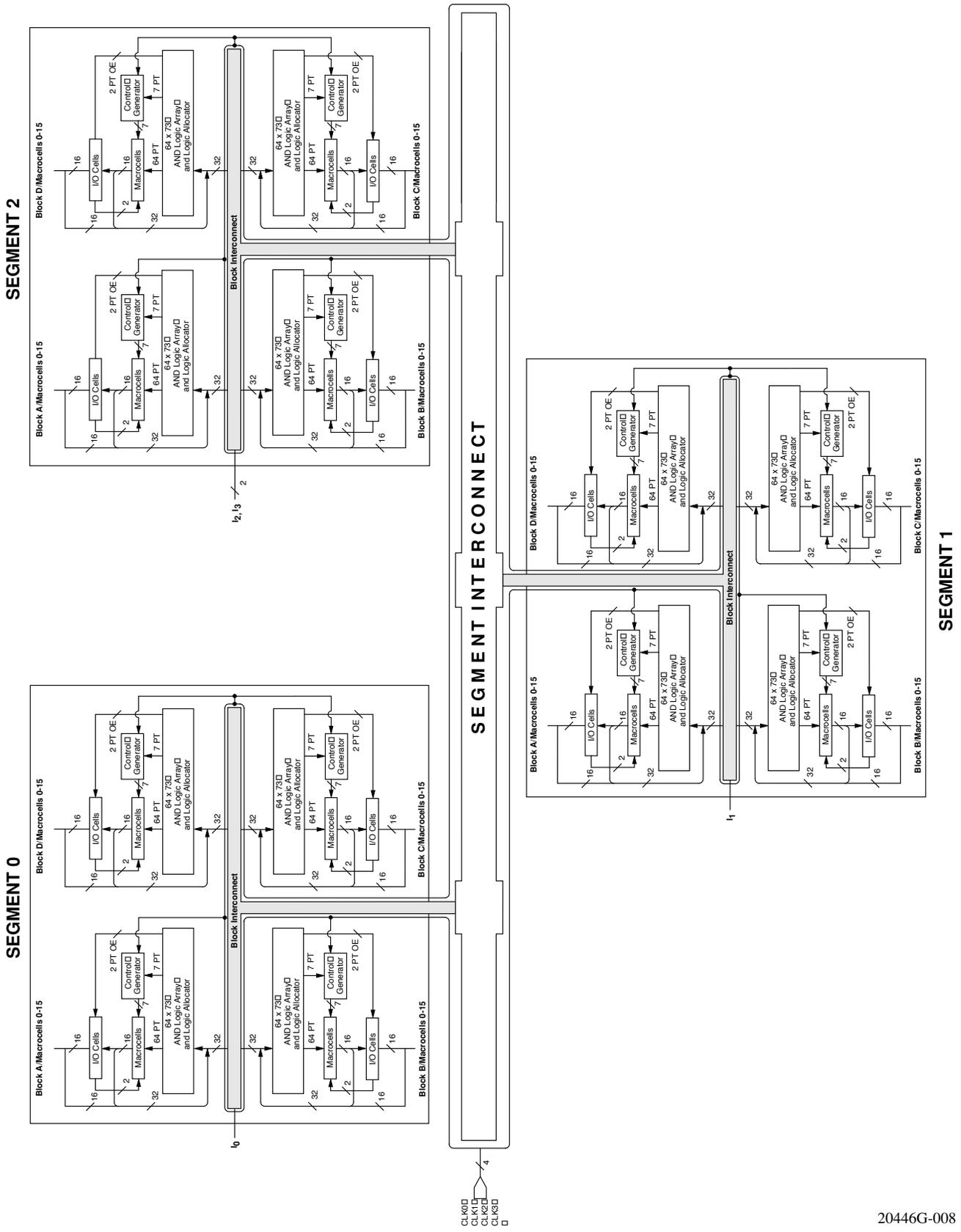
# MACH 5 PAL BLOCK



Select devices have been discontinued.  
See Ordering Information section for product status.

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# BLOCK DIAGRAM — M5-192/XXX

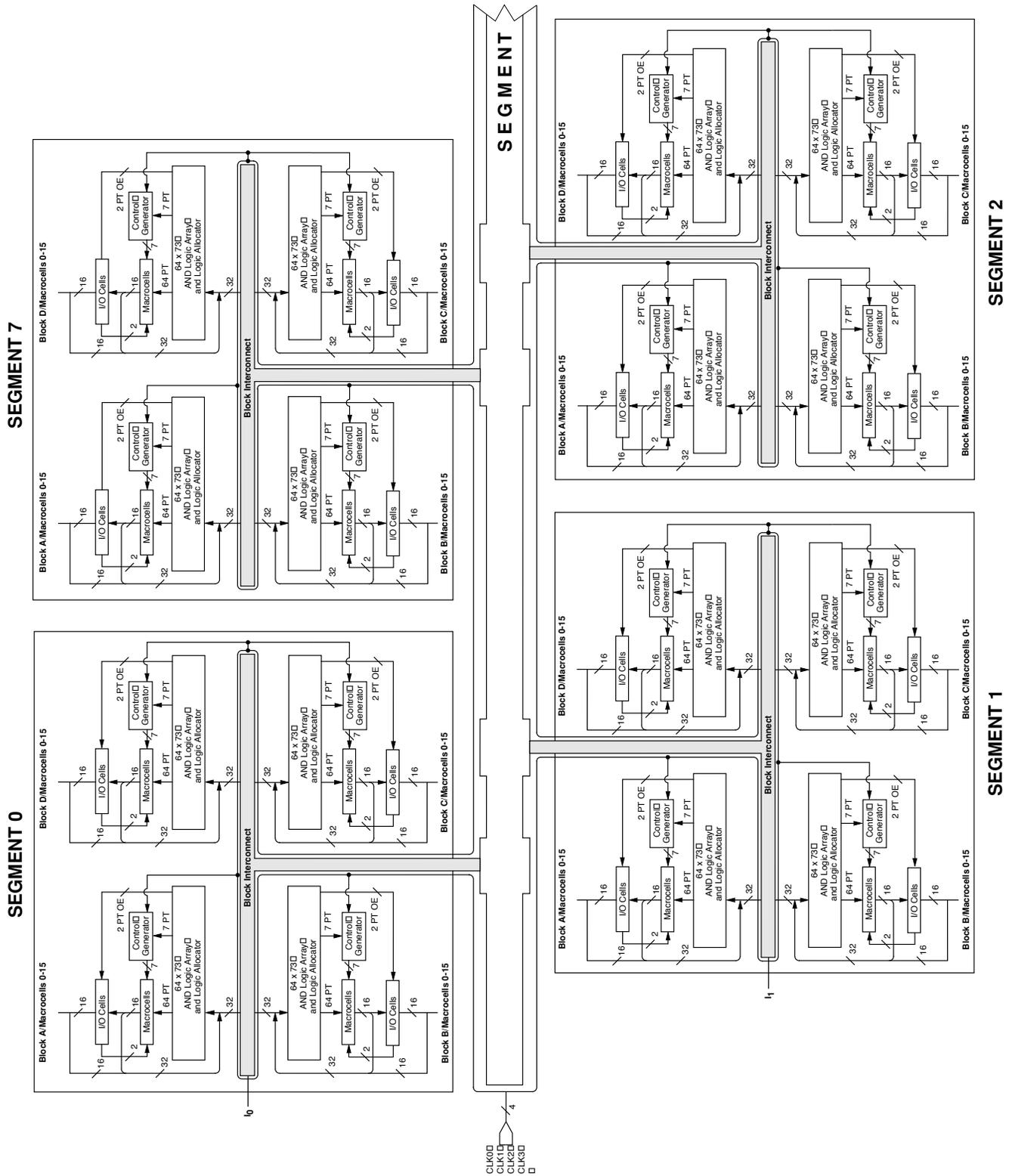


Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-008

# BLOCK DIAGRAM — M5(LV)-512/XXX

Continued



Select devices have been discontinued.  
See Ordering Information section for product status.

## ABSOLUTE MAXIMUM RATINGS

### M5LV

Storage Temperature	-65°C to +150°C
Device Junction Temperature	+130°C
Supply Voltage with Respect to Ground	-0.5 V to +4.5 V
DC Input Voltage	-0.5 V to 5.5 V
Static Discharge Voltage	2000 V
Latchup Current (-40°C to +85°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air	-40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued. See Ordering Information section for product status.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$	V
			$I_{OH} = 3.2 \text{ mA}$	2.4	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 100 \mu\text{A}$	0.2	V
			$I_{OL} = 16 \text{ mA (Note 1)}$	0.5	V
$V_{IH}$	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$	2.0	5.5	V
$V_{IL}$	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$	-0.3	0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$		10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$		-10	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$		10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$		-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$	-15	-160	mA

### Notes:

- Total  $I_{OL}$  between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
- Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup> (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Power Delays:</b>																
t <sub>PL1</sub>	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t <sub>PL2</sub>	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t <sub>PL3</sub>	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
<b>Additional Cluster Delay:</b>																
t <sub>PT</sub>	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
<b>Interconnect Delays:</b>																
t <sub>BLK</sub>	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t <sub>SEG</sub>	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
<b>Reset and Preset Delays:</b>																
t <sub>SRi</sub>	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t <sub>SR</sub>	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t <sub>SRR</sub>	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t <sub>SRW</sub>	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
<b>Clock Enable Delays:</b>																
t <sub>CES</sub>	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t <sub>CEH</sub>	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
<b>Width:</b>																
t <sub>WLS</sub>	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t <sub>WHS</sub>	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t <sub>WLA</sub>	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t <sub>WHA</sub>	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t <sub>GWA</sub>	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t <sub>WIR</sub>	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

Select devices have been discontinued. See Ordering Information section for product status.

## CAPACITANCE<sup>1</sup>

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
$C_{IN}$	I/CLK pin	$V_{IN} = 2.0\text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{VO}$	I/O pin	$V_{OUT} = 2.0\text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

## $I_{CC}$ vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

## $I_{CC}$ CURVES AT HIGH /LOW POWER MODES

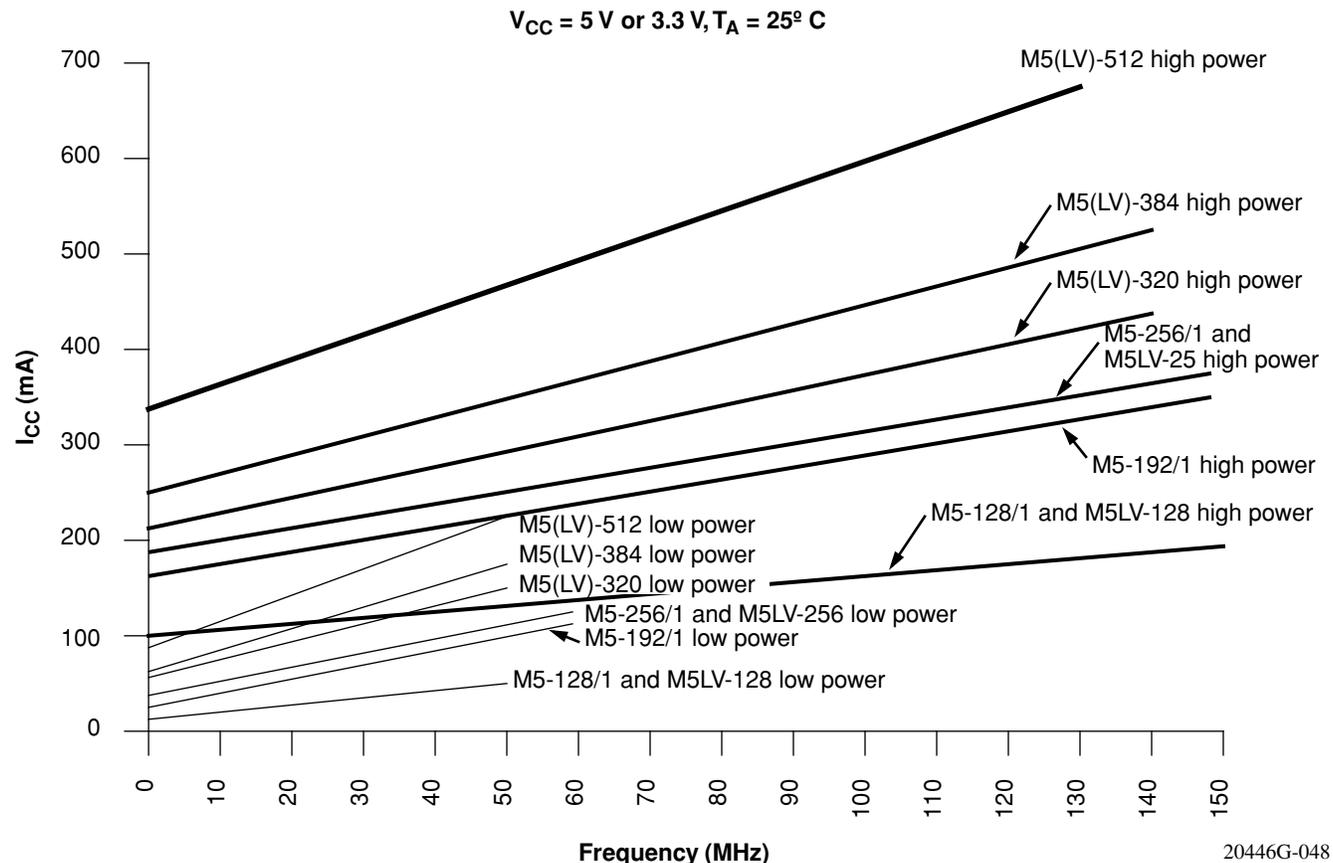


Figure 8.  $I_{CC}$  Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

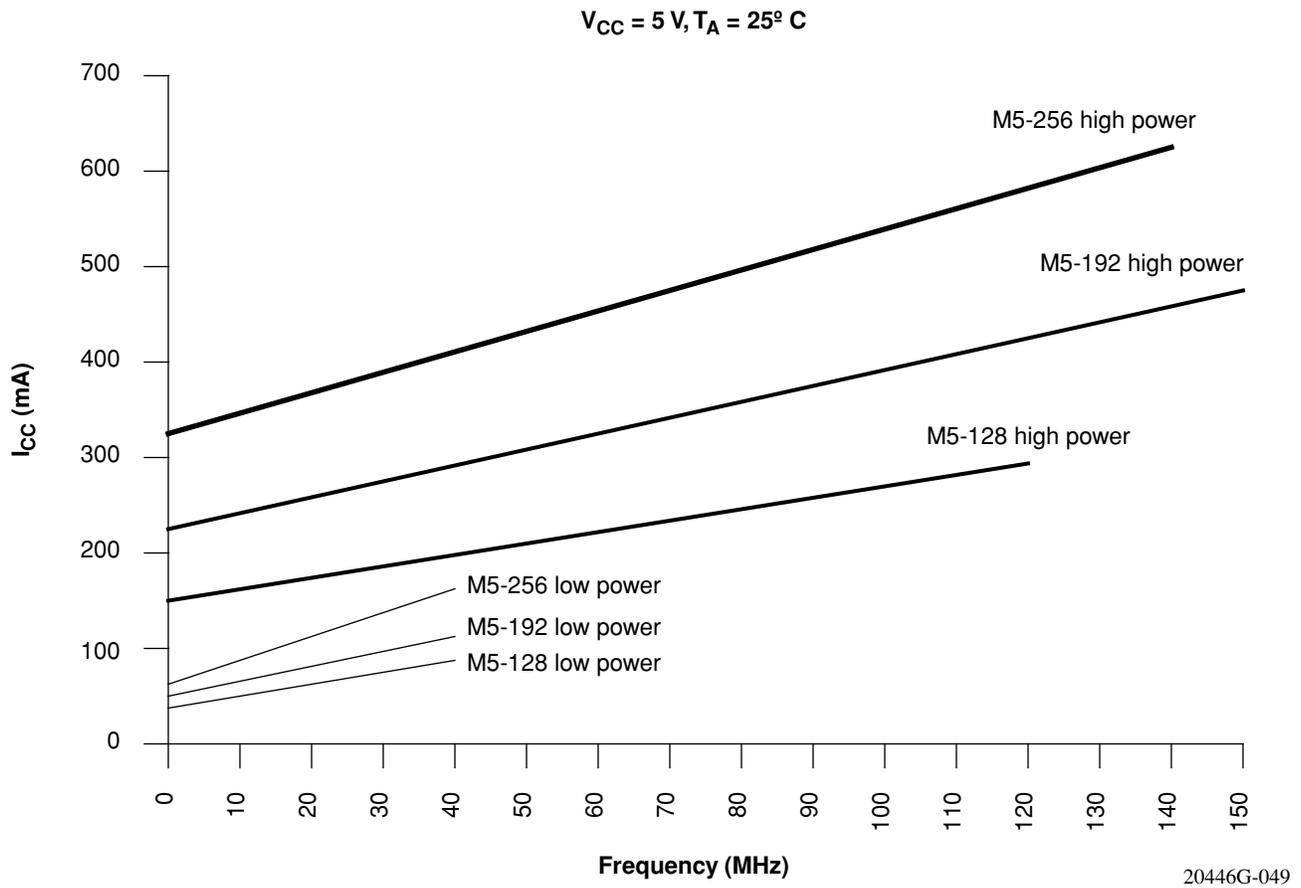


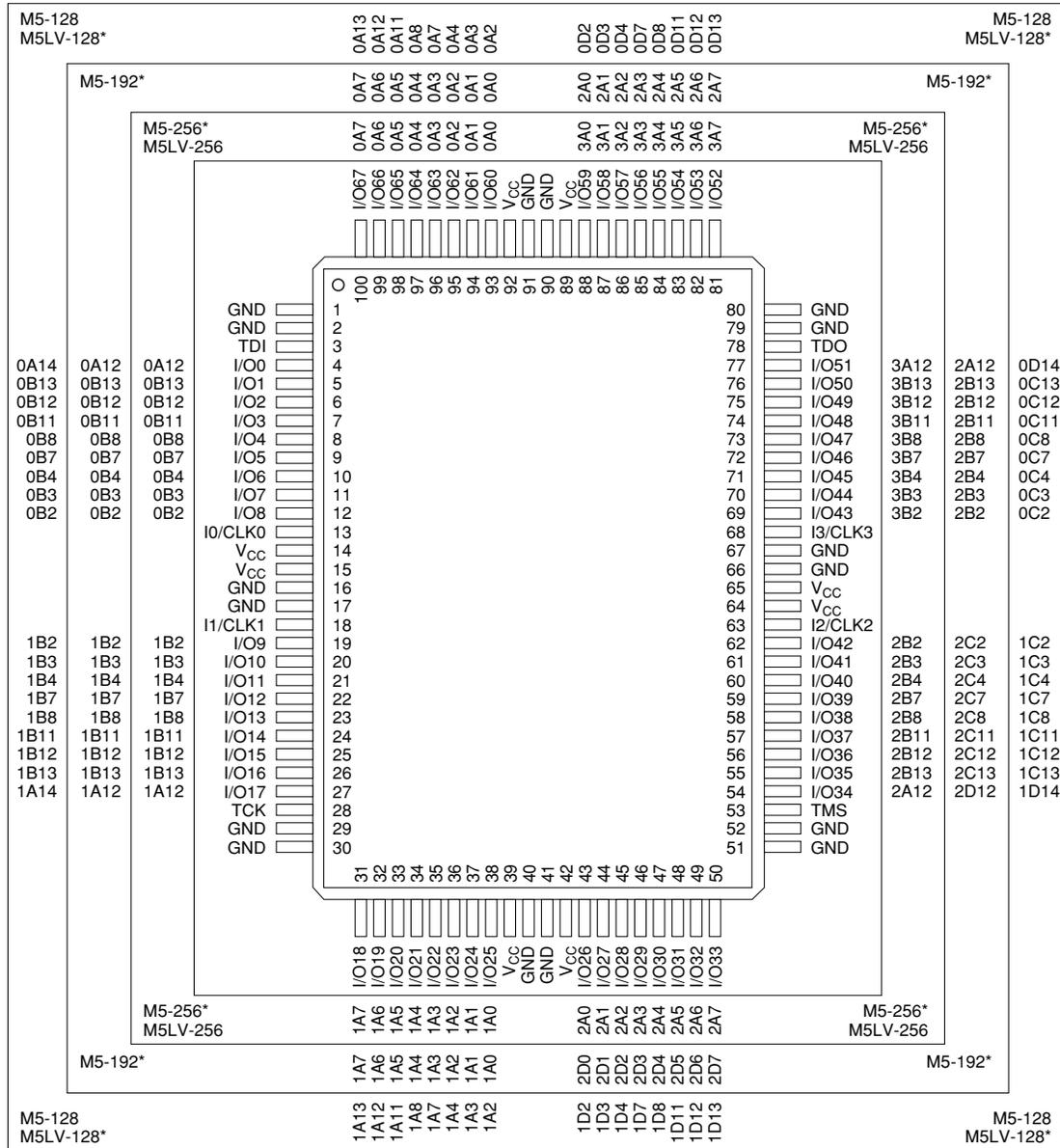
Figure 9.  $I_{CC}$  Curves at High/Low Power Modes

**Select devices have been discontinued. See Ordering Information section for product status.**

# 100-PIN PQFP CONNECTION DIAGRAM

## Top View

100-Pin PQFP (68 I/O)



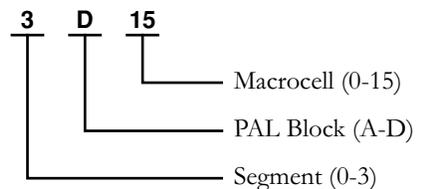
\*Package obsolete, contact factory.

20446G-016

Select devices have been discontinued. See Ordering Information section for product status.

### Pin Designations

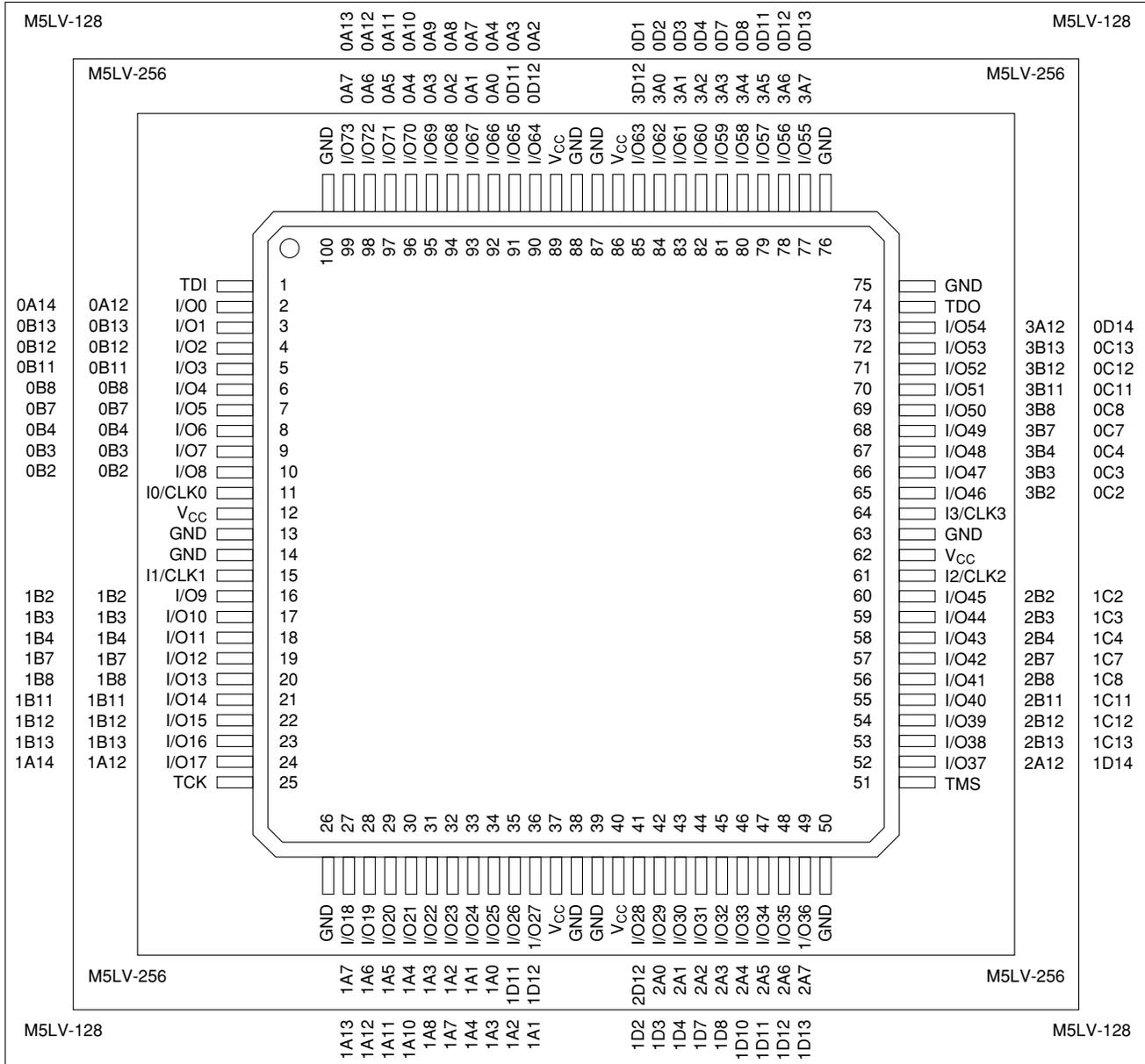
- |                    |                                  |
|--------------------|----------------------------------|
| CLK = Clock        | V <sub>CC</sub> = Supply Voltage |
| GND = Ground       | TDI = Test Data In               |
| I = Input          | TCK = Test Clock                 |
| I/O = Input/Output | TMS = Test Mode Select           |
| NC = No Connect    | TDO = Test Data Out              |



# 100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)

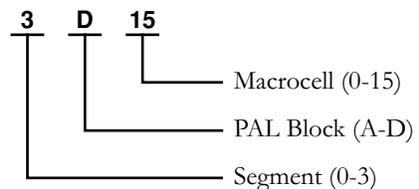


Select devices have been discontinued. See Ordering Information section for product status.

20446G-018

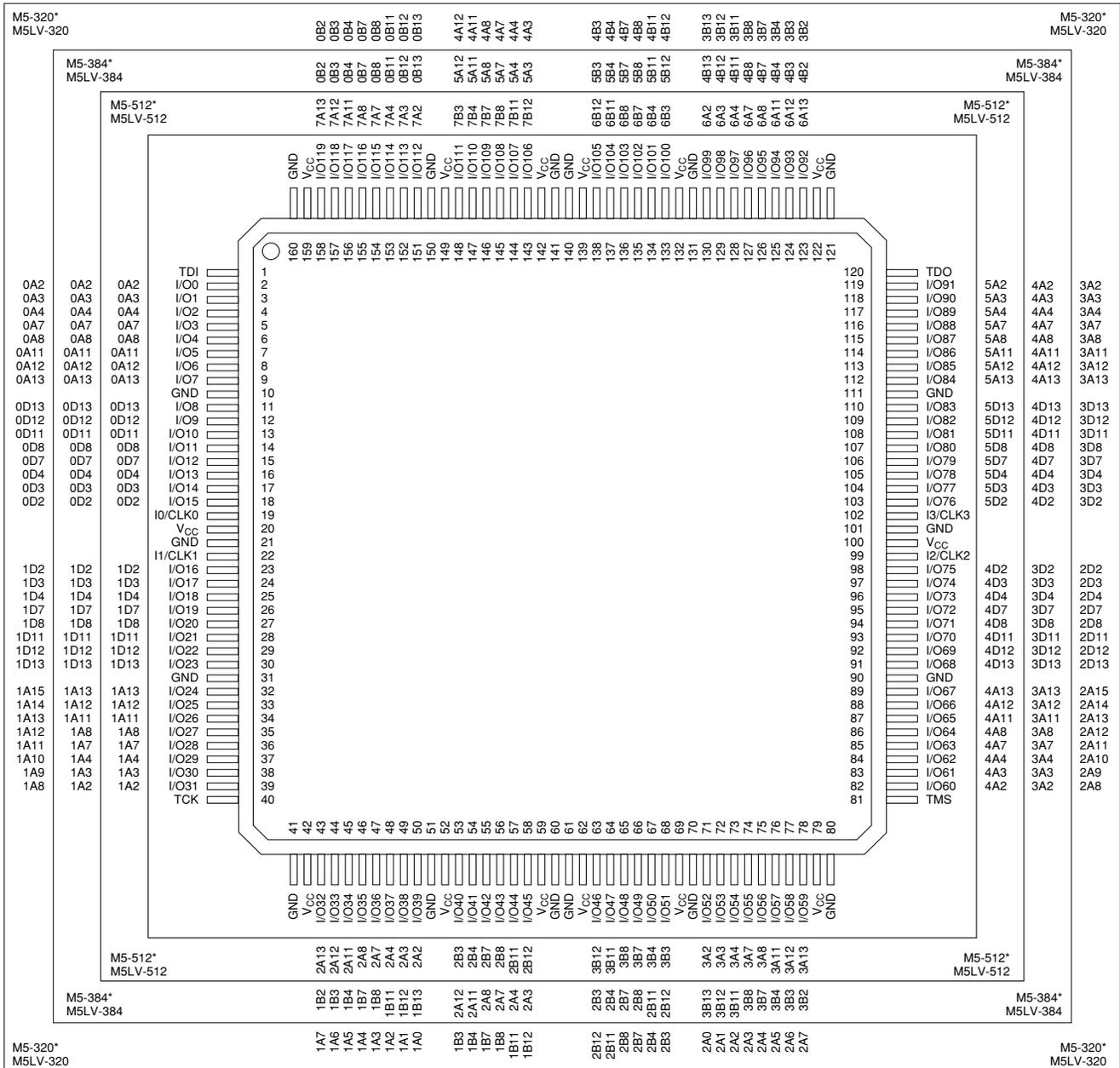
### Pin Designations

- |                    |                                  |
|--------------------|----------------------------------|
| CLK = Clock        | V <sub>CC</sub> = Supply Voltage |
| GND = Ground       | TDI = Test Data In               |
| I = Input          | TCK = Test Clock                 |
| I/O = Input/Output | TMS = Test Mode Select           |
| NC = No Connect    | TDO = Test Data Out              |



# 160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

160-Pin PQFP (320, 384, 512 Macrocells)



Select devices have been discontinued. See Ordering Information section for product status.

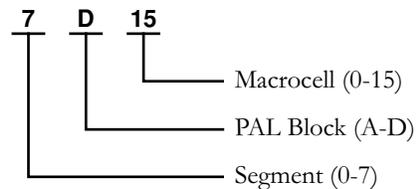
\*Package obsolete, contact factory.

20446G-022

## Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect

- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



# 352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

## Bottom View (I/O Pin-outs)

### 352-Ball BGA

	352-Ball BGA																									
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I <sub>3</sub> /CLK <sub>3</sub>	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O224	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	NC
3	GND	GND	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I/O211	I/O212	I/O213	I/O214	I <sub>2</sub> /CLK <sub>2</sub>	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	TMS	NC	NC
4	NC	I/O188	NC	TDO	I/O189	I/O190	I/O191	V <sub>CC</sub>	I/O192	V <sub>CC</sub>	I/O193	I/O194	I/O195	V <sub>CC</sub>	I/O196	I/O197	I/O198	V <sub>CC</sub>	I/O199	V <sub>CC</sub>	I/O200	I/O201	V <sub>CC</sub>	I/O202	I/O203	I/O204
5	GND	I/O183	I/O184	V <sub>CC</sub>	I/O178	I/O177	I/O176	I/O175	I/O174	I/O173	I/O172	I/O171	I/O170	I/O169	I/O168	I/O167	I/O166	I/O165	I/O164	I/O163	I/O162	I/O161	V <sub>CC</sub>	I/O160	I/O159	I/O158
6	NC	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193	I/O194	I/O195	I/O196	I/O197	I/O198	I/O199	I/O200
7	GND	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193
8	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181
9	GND	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174
10	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167
11	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159
12	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153
13	GND	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146
14	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139
15	NC	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131
16	I/O101	I/O102	I/O103	I/O104	I/O105	I/O106	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126
17	GND	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105	I/O106	I/O107	I/O108	I/O109	I/O110	I/O111
18	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105
19	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98
20	GND	I/O68	I/O69	I/O70	I/O71	I/O72	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92
21	I/O51	I/O52	I/O53	V <sub>CC</sub>	I/O54	I/O55	V <sub>CC</sub>	I/O56	V <sub>CC</sub>	I/O57	I/O58	I/O59	V <sub>CC</sub>	I/O60	I/O61	I/O62	V <sub>CC</sub>	I/O63	V <sub>CC</sub>	I/O64	I/O65	I/O66	I/O67	I/O68	I/O69	I/O70
22	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	TCK	NC	NC	I/O67	I/O68
23	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	TCK	NC	NC	I/O67	I/O68
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	NC	GND	NC	NC	NC

### Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

20446G-030

Select devices have been discontinued.  
See Ordering Information section for product status.

# 352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

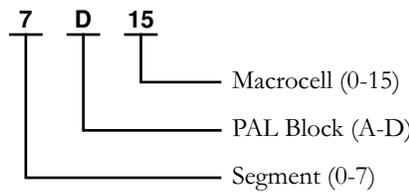
## Bottom View (Macrocell Association)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	I3/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	NC
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	NC
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I2/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	GND
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V <sub>CC</sub>	5A11	V <sub>CC</sub>	5D12	5D7	5D2	V <sub>CC</sub>	4D3	4D8	4D12	V <sub>CC</sub>	4A11	V <sub>CC</sub>	4A4	4A0	V <sub>CC</sub>	3A15	3A13	NC
5	GND	6A12	6A13	V <sub>CC</sub>																			3A14	3A15	3A13	GND
6	NC	6A9	6A10	6A15																			3A10	3A11	3A9	NC
7	GND	6A6	6A8	6A11																			3A6	3A4	3A7	NC
8	6A1	6A4	6A5	6A7																			3A2	3A1	3A0	GND
9	6B1	6A0	6A2	6A3																			V <sub>CC</sub>	3B1	3B2	3A5
10	GND	6B2	6B0	V <sub>CC</sub>																			3B3	3B4	3B3	NC
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	GND
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B10
13	6B14	6B13	6B12	6B11																			V <sub>CC</sub>	2B15	2B15	GND
14	GND	7B15	7B15	V <sub>CC</sub>																			2B11	2B12	2B13	2B14
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6
17	7B7	7B6	7B5	7B4																			V <sub>CC</sub>	2B0	2B2	GND
18	GND	7B3	7B2	V <sub>CC</sub>																			2A3	2A2	2A0	2B1
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC
22	GND	7A9	7A11	7A15																			V <sub>CC</sub>	2A13	2A12	GND
23	7A10	7A13	7A14	V <sub>CC</sub>																			TCK	NC	2A14	NC
24	NC	NC	TDI	0A2	0A5	0A7	0A10	0A11	0D14	0D12	0D8	0D3	V <sub>CC</sub>	1D2	1D7	1D12	V <sub>CC</sub>	1A11	1A6	1A8	1A3	1A1	NC	NC	GND	
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D13	0D10	0D6	0D2	0D0	I1/CLK1	1D1	1D5	1D10	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	NC
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	I1/CLK1	1D3	1D6	GND	1D15	GND	1A12	NC	NC	1A1	NC	NC	NC

**Pin Designations**

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

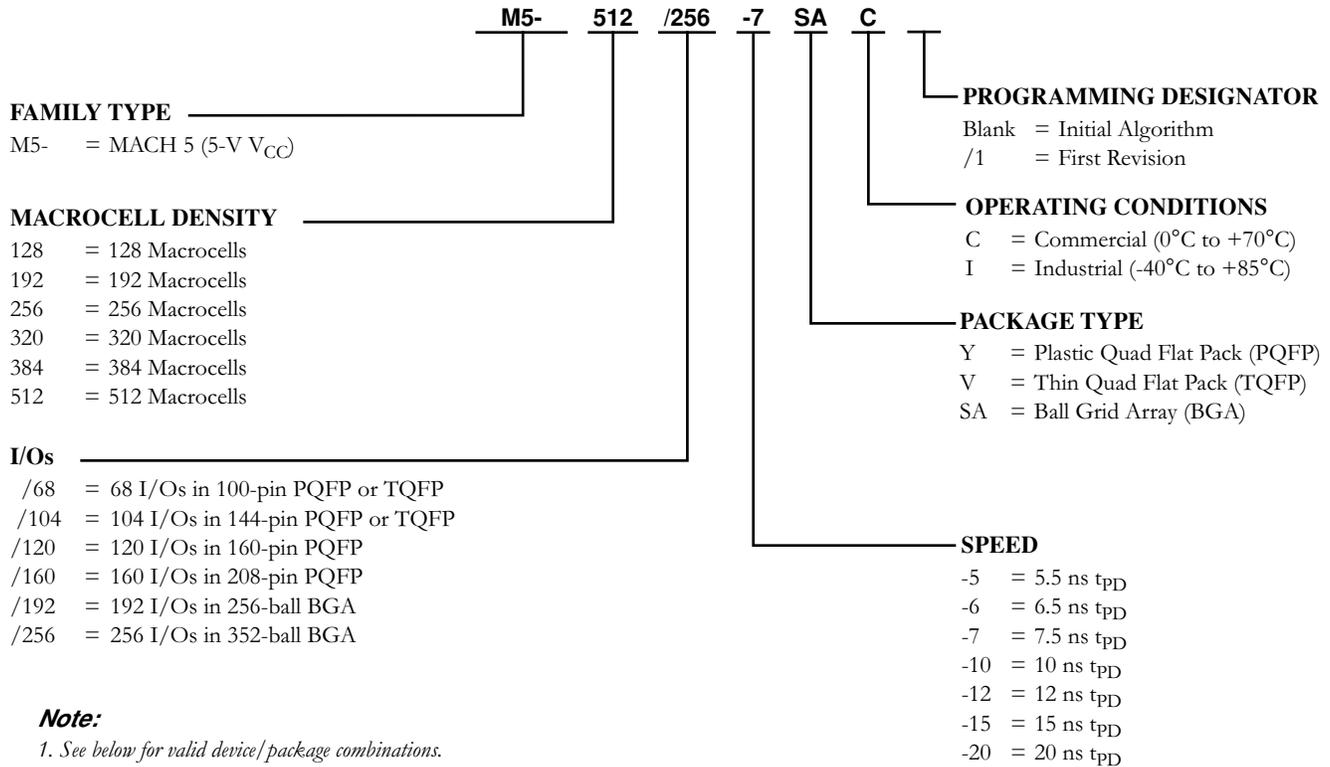


20446G-031

Select devices have been discontinued.  
See Ordering Information section for product status.

# 5V M5 ORDERING INFORMATION<sup>1,2</sup>

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



**Note:**

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15  Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC <sup>1</sup> , YI <sup>1</sup>
M5-128/120		YC, YI
M5-192/68		VC, VI
M5-192/120		YC, YI
M5-256/68		VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

**Device Marking**

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial: -6, -7, -10, -12, -15  Industrial: -7, -10, -12, -15, -20	YC, YI
M5-320/192		SAC, SAI
M5-384/160		YC, YI
M5-512/160		YC, YI
M5-512/256		SAC, SAI

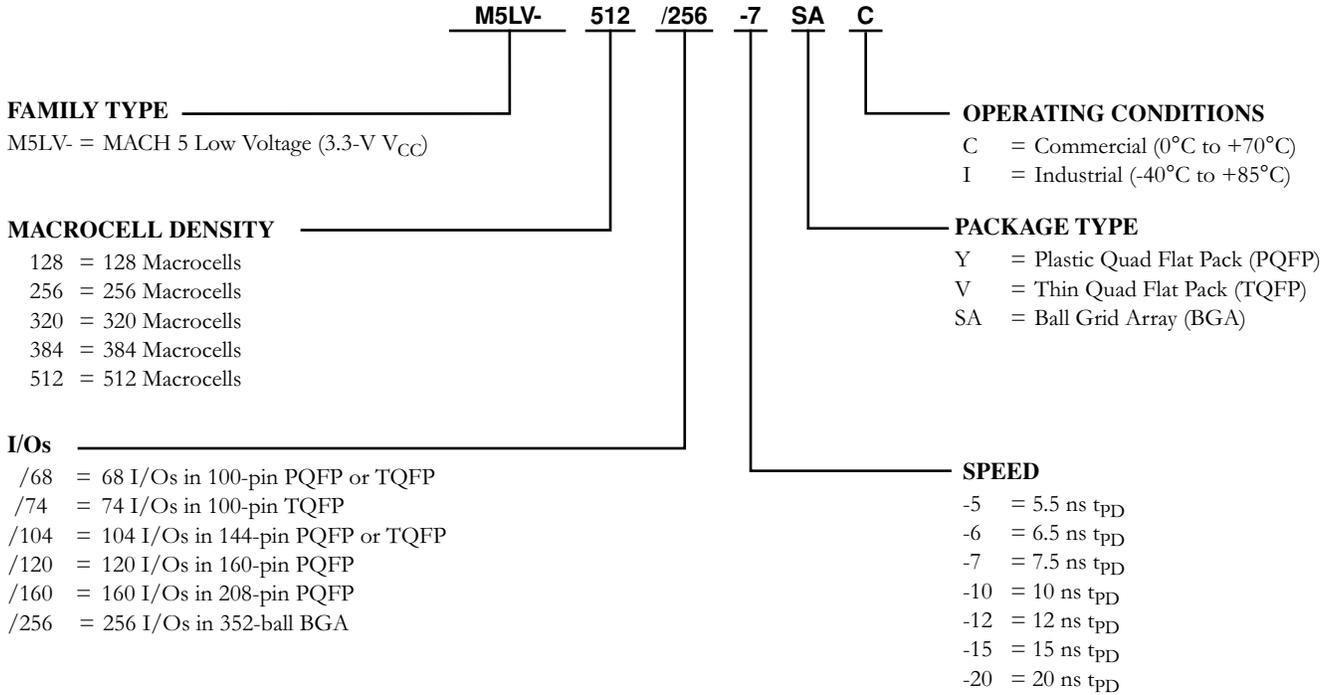
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued. See Ordering Information section for product status.

## 3.3V M5LV ORDERING INFORMATION<sup>1</sup>

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



**Note:**

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68		YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI
		Industrial: -7, -10, -12, -15

**Device Marking**

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations			
M5LV-320/120	Commercial: -6, -7, -10, -12, -15	YC, YI	
M5LV-320/160		YC, YI	
M5LV-384/120		YC, YI	
M5LV-384/160		YC, YI	
M5LV-512/120		YC, YI	
M5LV-512/160		YC, YI	
M5LV-512/256		Industrial: -10, -12, -15, -20	YC, YI
			SAC, SAI

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued. See Ordering Information section for product status.