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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

|                                 |                                                                                                                                                                       |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                              |
| Programmable Type               | In System Programmable                                                                                                                                                |
| Delay Time tpd(1) Max           | 10 ns                                                                                                                                                                 |
| Voltage Supply - Internal       | 4.5V ~ 5.5V                                                                                                                                                           |
| Number of Logic Elements/Blocks | -                                                                                                                                                                     |
| Number of Macrocells            | 128                                                                                                                                                                   |
| Number of Gates                 | -                                                                                                                                                                     |
| Number of I/O                   | 68                                                                                                                                                                    |
| Operating Temperature           | -40°C ~ 85°C (TA)                                                                                                                                                     |
| Mounting Type                   | Surface Mount                                                                                                                                                         |
| Package / Case                  | 100-LQFP                                                                                                                                                              |
| Supplier Device Package         | 100-TQFP (14x14)                                                                                                                                                      |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-128-68-10vi-1">https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-128-68-10vi-1</a> |



Table 1. MACH 5 Device Features <sup>1</sup>

| Feature                             | M5-128/1<br>M5LV-128 |     | M5-192/1 | M5-256/1<br>M5LV-256 |     | M5-320<br>M5LV-320 |     | M5-384<br>M5LV-384 |     | M5-512<br>M5LV-512 |     |
|-------------------------------------|----------------------|-----|----------|----------------------|-----|--------------------|-----|--------------------|-----|--------------------|-----|
| Supply Voltage (V)                  | 5                    | 3.3 | 5        | 5                    | 3.3 | 5                  | 3.3 | 5                  | 3.3 | 5                  | 3.3 |
| Macrocells                          | 128                  | 128 | 192      | 256                  | 256 | 320                | 320 | 384                | 384 | 512                | 512 |
| Maximum User I/O Pins               | 120                  | 120 | 120      | 160                  | 160 | 192                | 160 | 160                | 160 | 256                | 256 |
| t <sub>PD</sub> (ns)                | 5.5                  | 5.5 | 5.5      | 5.5                  | 5.5 | 6.5                | 6.5 | 6.5                | 6.5 | 6.5                | 6.5 |
| t <sub>SS</sub> (ns)                | 3.0                  | 3.0 | 3.0      | 3.0                  | 3.0 | 3.0                | 3.0 | 3.0                | 3.0 | 3.0                | 3.0 |
| t <sub>COS</sub> (ns)               | 4.5                  | 4.5 | 4.5      | 4.5                  | 4.5 | 5.0                | 5.0 | 5.0                | 5.0 | 5.0                | 5.0 |
| f <sub>CNT</sub> (MHz)              | 182                  | 182 | 182      | 182                  | 182 | 167                | 167 | 167                | 167 | 167                | 167 |
| Typical Static Power (mA)           | 35                   | 35  | 45       | 55                   | 55  | 70                 | 70  | 75                 | 75  | 100                | 100 |
| IEEE 1149.1 Boundary Scan Compliant | Yes                  | Yes | Yes      | Yes                  | Yes | Yes                | Yes | Yes                | Yes | Yes                | Yes |
| PCI-Compliant                       | Yes                  | Yes | Yes      | Yes                  | Yes | Yes                | Yes | Yes                | Yes | Yes                | Yes |

**Note:**

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

## GENERAL DESCRIPTION

The MACH<sup>®</sup> 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E<sup>2</sup>CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.  
See Ordering Information section for product status.

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



Figure 1. MACH 5 Block Diagram

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The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

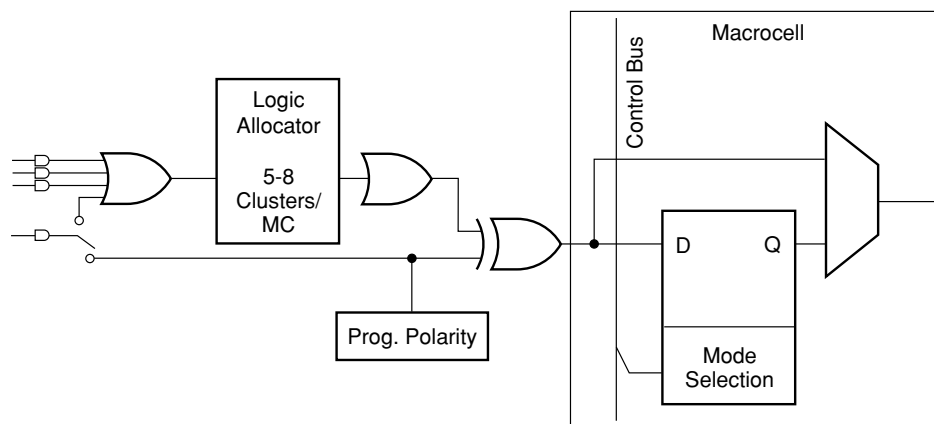
Select devices have been discontinued.  
See Ordering Information section for product status.

## Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



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Figure 3. Macrocell Diagram

## Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

### Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ( $A*B*C$ )
- ◆ Sum-term clock ( $A+B+C$ )

### Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

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- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

#### Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

#### Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

**Figure 4. Clock Generator**



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**Figure 5. Set/Reset Generator**

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.  
See Ordering Information section for product status.**

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS <sup>1</sup>

Both the 3.3-V and 5-V  $V_{CC}$  MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

### Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

## BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

|                                     |            |
|-------------------------------------|------------|
| High Speed/High Power               | 100% Power |
| Medium High Speed/Medium High Power | 67% Power  |
| Medium Low Speed/Medium Low Power   | 40% Power  |
| Low Speed/Low Power                 | 20% Power  |

## PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

Select devices have been discontinued. See Ordering Information section for product status.



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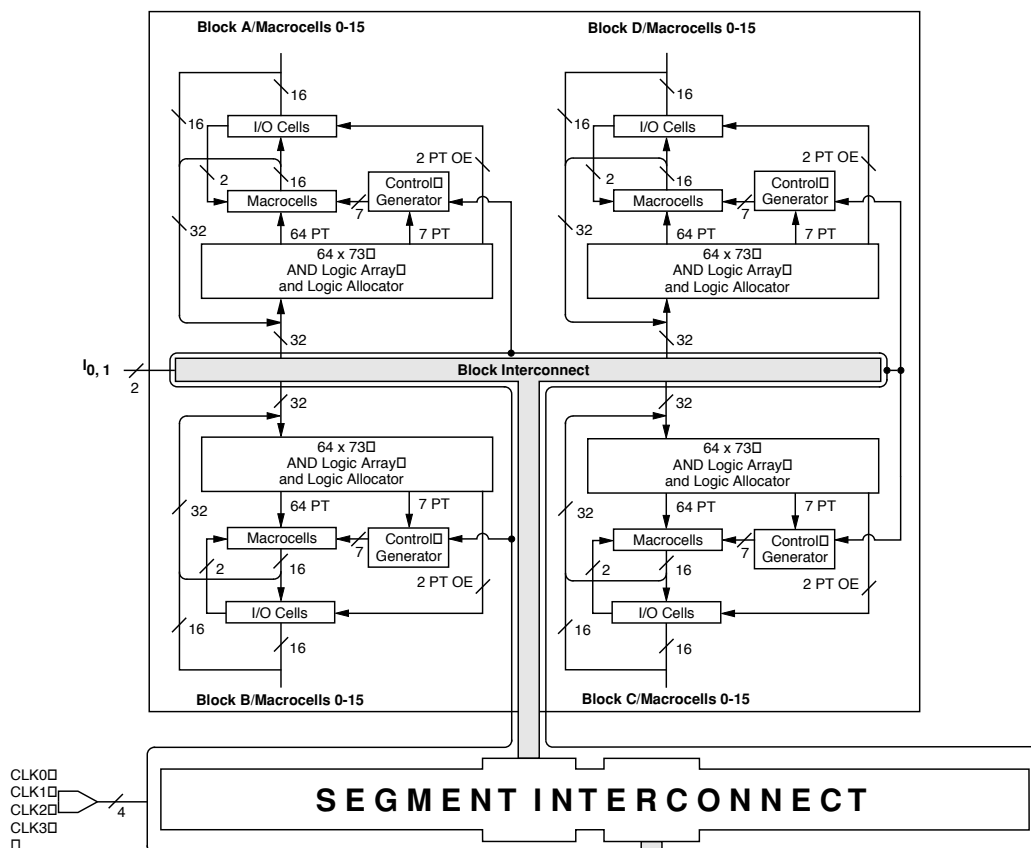
## SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

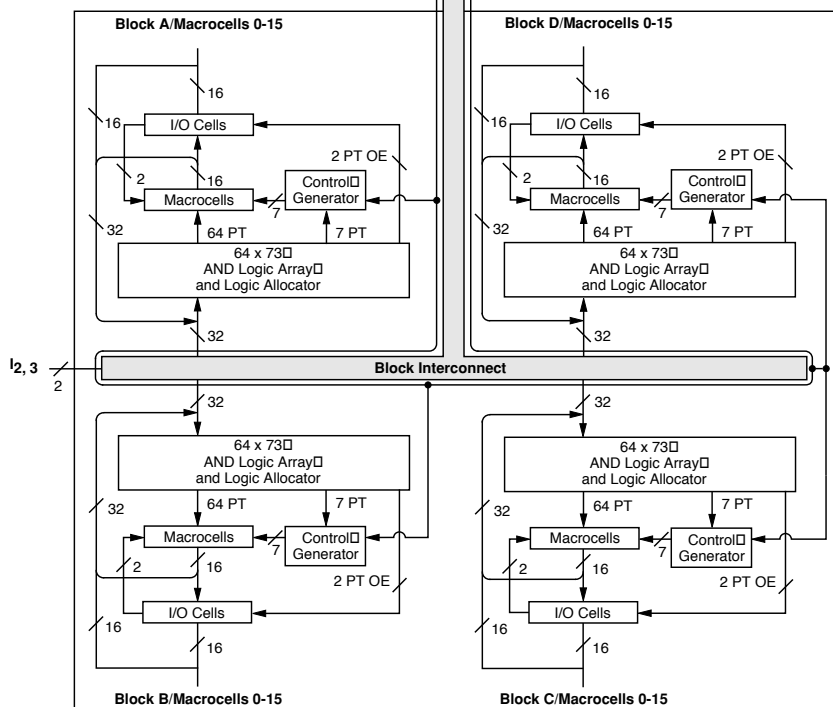
**Select devices have been discontinued.  
See Ordering Information section for product status.**

# BLOCK DIAGRAM — M5(LV)-128/XXX

## SEGMENT 0



## SEGMENT 1



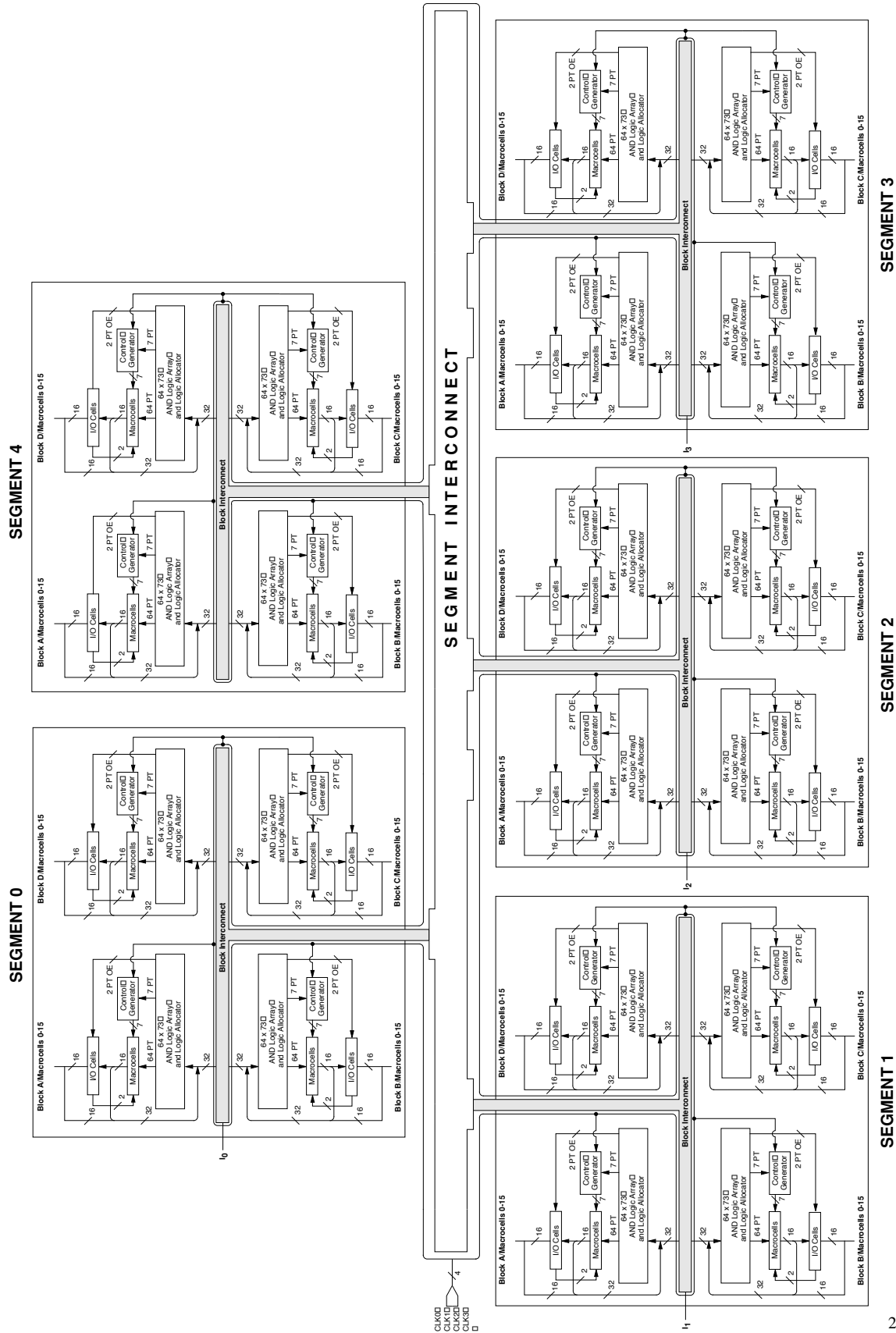
Select devices have been discontinued.  
See Ordering Information section for product status.

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# BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.  
See Ordering Information section for product status.

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## ABSOLUTE MAXIMUM RATINGS

### M5

Storage Temperature. . . . . -65°C to +150°C  
 Device Junction  
 Temperature (Note 1) . . . . . +130°C or +150°C  
 Supply Voltage  
 with Respect to Ground . . . . . -0.5 V to +7.0 V  
 DC Input Voltage . . . . . -0.5 V to 5.5 V  
 Static Discharge Voltage . . . . . 2000 V  
 Latchup Current (-40°C to +85°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . 0°C to +70°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . -40°C to +85°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

Select devices have been discontinued.  
See Ordering Information section for product status.

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                                                                     | Test Description                                                                              | Min | Typ | Max  | Unit          |
|------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage<br>(For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices) | $I_{OH} = -3.2 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$     | 2.4 |     |      | V             |
|                  |                                                                                           | $I_{OH} = -100 \mu\text{A}$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$    |     | 3.3 | 3.6  | V             |
|                  | Output HIGH Voltage<br>(For M5-128, M5-192, M5-256 Devices)                               | $I_{OH} = -3.2 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$     | 2.4 |     |      | V             |
|                  |                                                                                           | $I_{OH} = -2.5 \text{ mA}$ , $V_{CC} = 5.25 \text{ V}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ |     |     | 3.6  | V             |
| $V_{OL}$         | Output LOW Voltage (Note 2)                                                               | $I_{OL} = +16 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$      |     |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                                                                        | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)                                 | 2.0 |     |      | V             |
| $V_{IL}$         | Input LOW Voltage                                                                         | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)                                  |     |     | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current                                                                | $V_{IN} = 5.25$ , $V_{CC} = \text{Max}$ (Note 4)                                              |     |     | 10   | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current                                                                 | $V_{IN} = 0$ , $V_{CC} = \text{Max}$ (Note 4)                                                 |     |     | -10  | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH                                                     | $V_{OUT} = 5.25$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)      |     |     | 10   | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW                                                      | $V_{OUT} = 0$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)         |     |     | -10  | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current                                                              | $V_{OUT} = 0.5 V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 5)           | -30 |     | -180 | mA            |

### Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.
- Total  $I_{OL}$  between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

## ABSOLUTE MAXIMUM RATINGS

### M5LV

Storage Temperature. . . . . -65°C to +150°C  
 Device Junction Temperature. . . . . +130°C  
 Supply Voltage  
 with Respect to Ground. . . . . -0.5 V to +4.5 V  
 DC Input Voltage. . . . . -0.5 V to 5.5 V  
 Static Discharge Voltage. . . . . 2000 V  
 Latchup Current (-40°C to +85°C). . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . 0°C to +70°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . -40°C to +85°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +3.0 V to +3.6 V  
*Operating ranges define those limits between which the functionality of the device is guaranteed.*

Select devices have been discontinued.  
See Ordering Information section for product status.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Description                                                                          |                                   | Min            | Max  | Unit    |
|------------------|---------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------|----------------|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $V_{CC} = \text{Min}$                                                                     | $I_{OH} = -100 \mu A$             | $V_{CC} - 0.2$ |      | V       |
|                  |                                       | $V_{IN} = V_{IH} \text{ or } V_{IL}$                                                      | $I_{OH} = 3.2 \text{ mA}$         | 2.4            |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $V_{CC} = \text{Min}$                                                                     | $I_{OL} = 100 \mu A$              |                | 0.2  | V       |
|                  |                                       | $V_{IN} = V_{IH} \text{ or } V_{IL}$                                                      | $I_{OL} = 16 \text{ mA (Note 1)}$ |                | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | $V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$            |                                   | 2.0            | 5.5  | V       |
| $V_{IL}$         | Input LOW Voltage                     | $V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$            |                                   | -0.3           | 0.8  | V       |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$                                              |                                   |                | 10   | $\mu A$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$                                                |                                   |                | -10  | $\mu A$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$ |                                   |                | 10   | $\mu A$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$   |                                   |                | -10  | $\mu A$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$  |                                   | -15            | -160 | mA      |

### Notes:

1. Total  $I_{OL}$  between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                        |                                                       | -5  |     | -6  |      | -7  |      | -10 |      | -12 |      | -15 |      | -20  |      | Unit |
|------------------------|-------------------------------------------------------|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|------|------|------|
|                        |                                                       | Min | Max | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min  | Max  |      |
| Combinatorial Delay:   |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>PDi</sub>       | Internal combinatorial propagation delay              |     | 3.5 |     | 4.5  |     | 5.5  |     | 8.0  |     | 10.0 |     | 13.0 |      | 18.0 | ns   |
| t <sub>PD</sub>        | Combinatorial propagation delay                       |     | 5.5 |     | 6.5  |     | 7.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |
| Registered Delays:     |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SS</sub>        | Synchronous clock setup time                          | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 8.0 |      | 10.0 |      | ns   |
| t <sub>SA</sub>        | Asynchronous clock setup time                         | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>HS</sub>        | Synchronous clock hold time                           | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HA</sub>        | Asynchronous clock hold time                          | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>COSi</sub>      | Synchronous clock to internal output                  |     | 2.5 |     | 3.0  |     | 4.0  |     | 5.0  |     | 6.0  |     | 8.0  |      | 10.0 | ns   |
| t <sub>COS</sub>       | Synchronous clock to output                           |     | 4.5 |     | 5.0  |     | 6.0  |     | 7.0  |     | 8.0  |     | 10.0 |      | 12.0 | ns   |
| t <sub>COAi</sub>      | Asynchronous clock to internal output                 |     | 6.0 |     | 6.0  |     | 8.0  |     | 10.0 |     | 13.0 |     | 15.0 |      | 18.0 | ns   |
| t <sub>COA</sub>       | Asynchronous clock to output                          |     | 8.0 |     | 8.0  |     | 10.0 |     | 12.0 |     | 15.0 |     | 17.0 |      | 20.0 | ns   |
| Latched Delays:        |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SAL</sub>       | Latch setup time                                      | 3.0 |     | 4.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>HAL</sub>       | Latch hold time                                       | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>PDLi</sub>      | Transparent latch internal                            |     | 6.0 |     | 7.0  |     | 7.0  |     | 8.0  |     | 9.0  |     | 10.0 |      | 10.0 | ns   |
| t <sub>PDL</sub>       | Propagation delay through transparent latch           |     | 8.0 |     | 9.0  |     | 9.0  |     | 10.0 |     | 11.0 |     | 12.0 |      | 12.0 | ns   |
| t <sub>GOAi</sub>      | Gate to internal output                               |     | 7.0 |     | 8.0  |     | 8.0  |     | 9.0  |     | 10.0 |     | 11.0 |      | 12.0 | ns   |
| t <sub>GOA</sub>       | Gate to output                                        |     | 9.0 |     | 10.0 |     | 10.0 |     | 11.0 |     | 12.0 |     | 13.0 |      | 14.0 | ns   |
| Input Register Delays: |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SIRS</sub>      | Input register setup time using a synchronous clock   | 2.0 |     | 2.0 |      | 2.0 |      | 3.0 |      | 3.0 |      | 3.0 |      | 3.0  |      | ns   |
| t <sub>SIRA</sub>      | Input register setup time using an asynchronous clock | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HIRS</sub>      | Input register hold time using a synchronous clock    | 3.0 |     | 3.0 |      | 3.0 |      | 4.0 |      | 4.0 |      | 4.0 |      | 4.0  |      | ns   |
| t <sub>HIRA</sub>      | Input register hold time using an asynchronous clock  | 6.0 |     | 6.0 |      | 6.0 |      | 7.0 |      | 7.0 |      | 7.0 |      | 7.0  |      | ns   |
| Input Latch Delays:    |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SIL</sub>       | Input latch setup time                                | 2.0 |     | 2.0 |      | 2.0 |      | 3.0 |      | 3.0 |      | 3.0 |      | 3.0  |      | ns   |
| t <sub>HIL</sub>       | Input latch hold time                                 | 6.0 |     | 6.0 |      | 6.0 |      | 7.0 |      | 7.0 |      | 7.0 |      | 7.0  |      | ns   |
| t <sub>PDILi</sub>     | Transparent input latch                               |     | 5.0 |     | 5.0  |     | 5.5  |     | 6.0  |     | 6.0  |     | 6.0  |      | 6.0  | ns   |
| Output Delays:         |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>BUF</sub>       | Output buffer delay                                   |     | 2.0 |     | 2.0  |     | 2.0  |     | 2.0  |     | 2.0  |     | 2.0  |      | 2.0  | ns   |
| t <sub>SLW</sub>       | Slow slew rate delay                                  |     | 2.5 |     | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |      | 2.5  | ns   |
| t <sub>EA</sub>        | Output enable time                                    |     | 7.5 |     | 7.5  |     | 9.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |
| t <sub>ER</sub>        | Output disable time                                   |     | 7.5 |     | 7.5  |     | 9.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |

Select devices have been discontinued.  
See Ordering Information section for product status.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup> (CONTINUED)

|                   |                                                                                                                                 | -5  |     | -6  |     | -7   |     | -10  |     | -12  |     | -15  |     | -20  |     | Unit |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|
|                   |                                                                                                                                 | Min | Max | Min | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |
| Frequency:        |                                                                                                                                 |     |     |     |     |      |     |      |     |      |     |      |     |      |     |      |
| f <sub>MAX</sub>  | External feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COS</sub> )  | 133 |     | 125 |     | 100  |     | 83.3 |     | 71.4 |     | 55.6 |     | 45.5 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COSi</sub> ) | 182 |     | 167 |     | 125  |     | 100  |     | 83.3 |     | 62.5 |     | 50.0 |     | MHz  |
|                   | No feedback PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>HS</sub> )          | 200 |     | 167 |     | 167  |     | 125  |     | 100  |     | 83.3 |     | 83.3 |     | MHz  |
| f <sub>MAXA</sub> | External feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COA</sub> )  | 91  |     | 91  |     | 71.4 |     | 58.8 |     | 47.6 |     | 41.7 |     | 35.7 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COAi</sub> ) | 111 |     | 111 |     | 83.3 |     | 66.7 |     | 52.6 |     | 45.5 |     | 38.5 |     | MHz  |
|                   | No feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>HA</sub> )         | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |
| f <sub>MAXI</sub> | Maximum input register frequency 1/(t <sub>SIRS</sub> +t <sub>HIRS</sub> ) or 1/(2 x t <sub>WICW</sub> )                        | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |

### Notes:

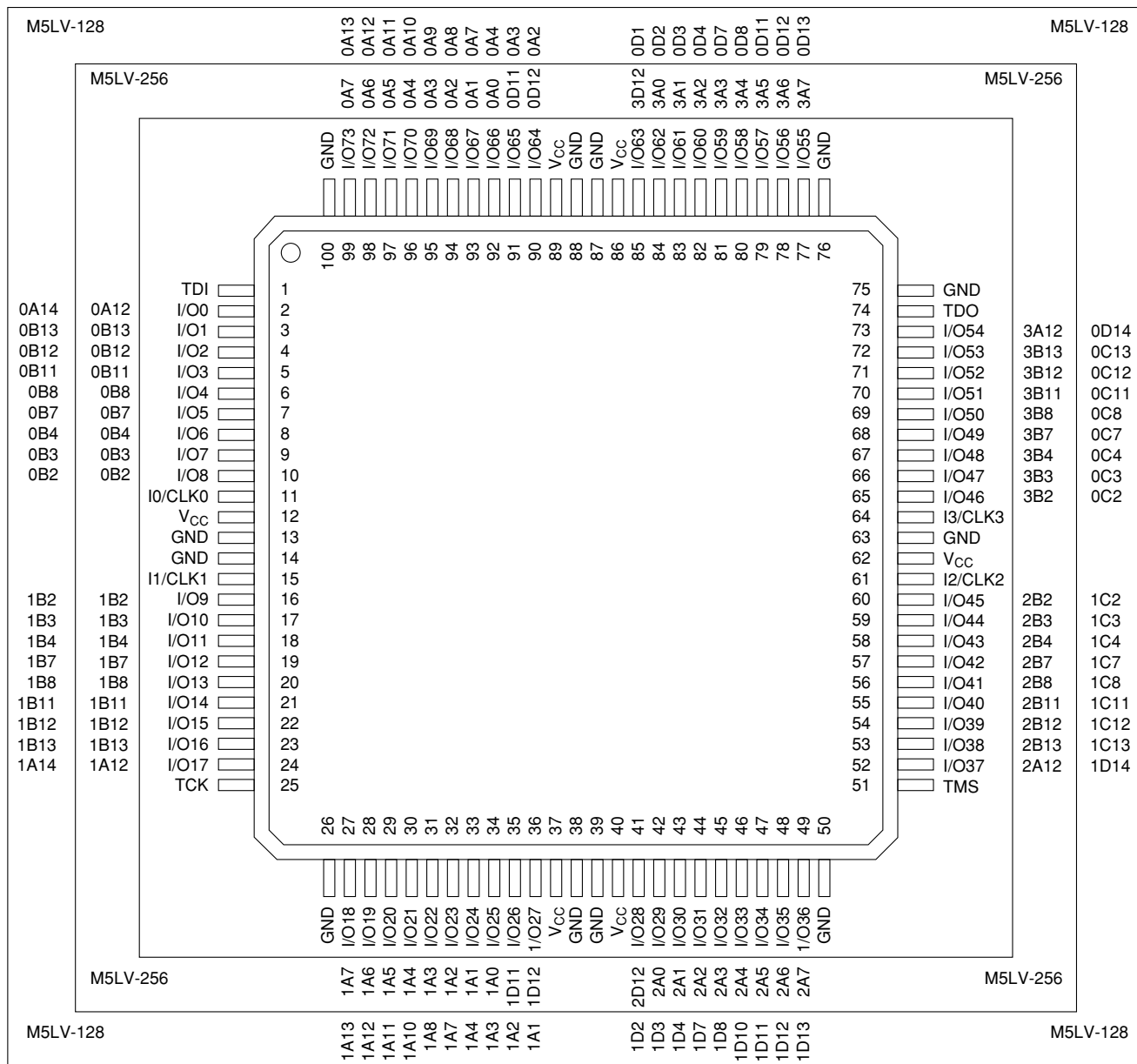
- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ( $f_{MAX}/2$ ).

Select devices have been discontinued.  
See Ordering Information section for product status.

# 100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

## Top View

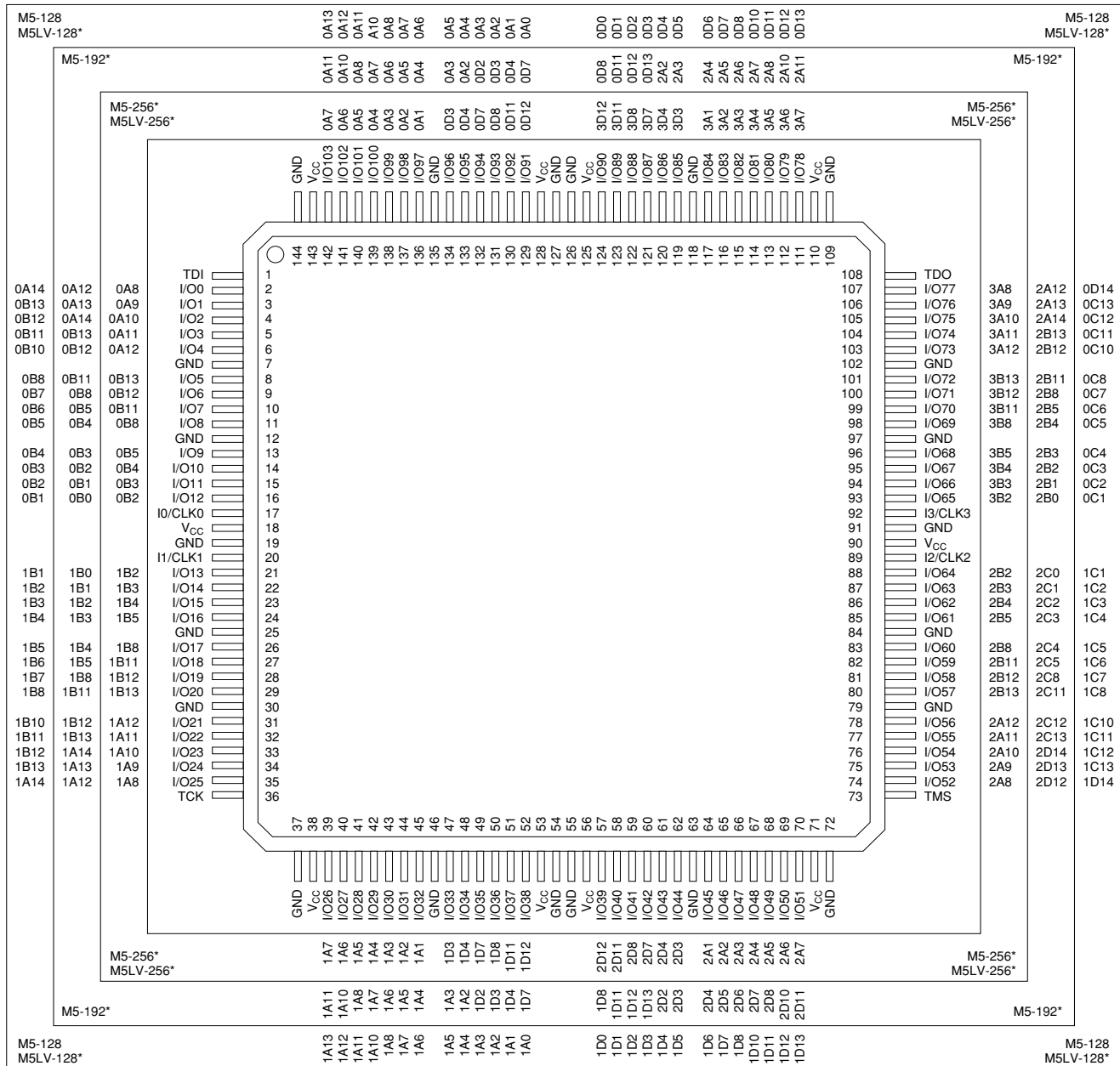
100-Pin TQFP (74 I/O)



# 144-PIN PQFP CONNECTION DIAGRAM

## Top View

144-Pin PQFP



Select devices have been discontinued.  
See Ordering Information section for product status.

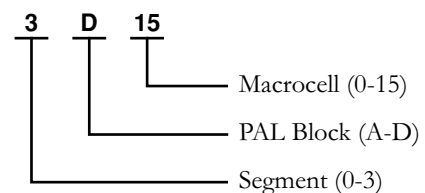
\*Package obsolete, contact factory.

20446G-019

### Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

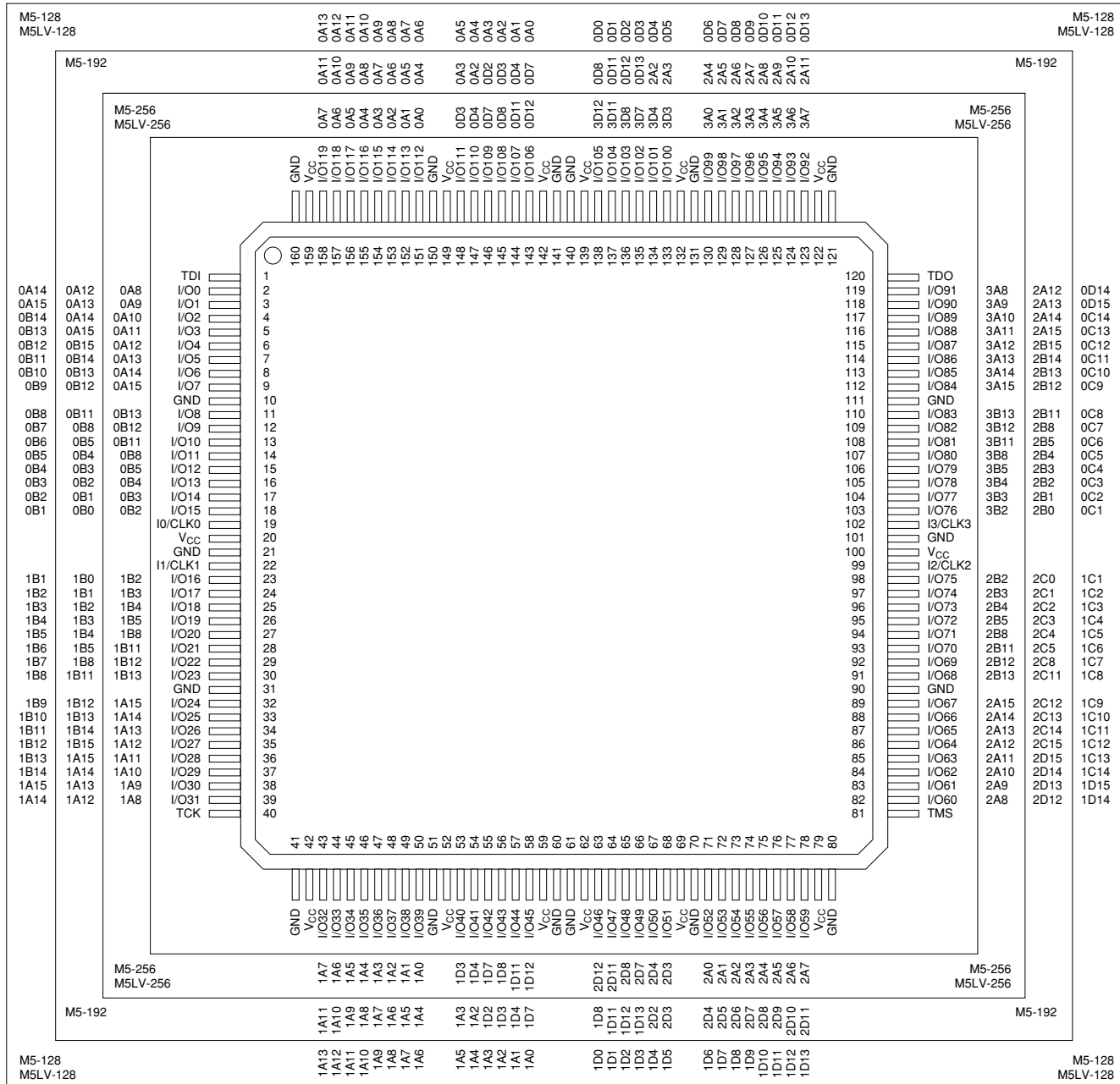
V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



# 160-PIN PQFP CONNECTION DIAGRAM

## Top View

### 160-Pin PQFP (128, 192, 256 Macrocells)



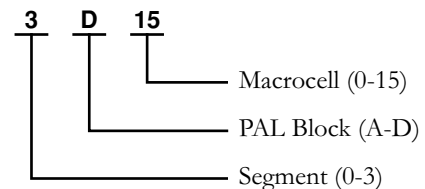
Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-021

### Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



# 208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

208-Pin PQFP (320, 384, 512 Macrocells)



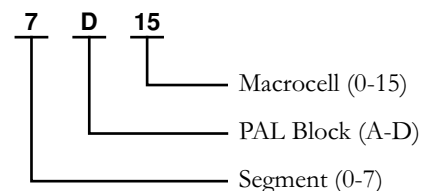
Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-024

## Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

VCC = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



## 256-BALL BGA CONNECTION DIAGRAM — M5-320

### Bottom View (I/O Pin-outs)

256-Ball BGA

|   | 20    | 19    | 18              | 17              | 16              | 15    | 14              | 13    | 12    | 11    | 10    | 9      | 8      | 7               | 6      | 5               | 4               | 3               | 2      | 1      |   |
|---|-------|-------|-----------------|-----------------|-----------------|-------|-----------------|-------|-------|-------|-------|--------|--------|-----------------|--------|-----------------|-----------------|-----------------|--------|--------|---|
| A | GND   | I/O11 | GND             | I/O44           | I/O58           | GND   | I/O70           | I/O76 | GND   | GND   | GND   | GND    | I/O108 | I/O116          | GND    | I/O128          | I/O134          | GND             | GND    | GND    | A |
| B | GND   | I/O12 | I/O28           | I/O45           | I/O59           | I/O64 | I/O71           | I/O77 | I/O84 | I/O90 | I/O96 | I/O102 | I/O109 | I/O117          | I/O122 | I/O129          | I/O135          | I/O148          | I/O164 | GND    | B |
| C | I/O0  | I/O13 | V <sub>CC</sub> | I/O46           | I/O60           | I/O65 | I/O72           | I/O78 | I/O85 | I/O91 | I/O97 | I/O103 | I/O110 | I/O118          | I/O123 | I/O130          | I/O136          | V <sub>CC</sub> | I/O165 | I/O181 | C |
| D | I/O1  | I/O14 | I/O29           | V <sub>CC</sub> | V <sub>CC</sub> | I/O66 | V <sub>CC</sub> | I/O79 | I/O86 | I/O92 | I/O98 | I/O104 | I/O111 | V <sub>CC</sub> | I/O124 | V <sub>CC</sub> | V <sub>CC</sub> | I/O149          | I/O166 | I/O182 | D |
| E | I/O2  | I/O15 | I/O30           | TDI             |                 |       |                 |       |       |       |       |        |        |                 |        |                 | TDO             | I/O150          | I/O167 | I/O183 | E |
| F | GND   | I/O16 | I/O31           | I/O47           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O137          | I/O151          | I/O168 | GND    | F |
| G | I/O3  | I/O17 | I/O32           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O152          | I/O169 | I/O184 | G |
| H | GND   | I/O18 | I/O33           | I/O48           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O138          | I/O153          | I/O170 | GND    | H |
| J | I/O4  | I/O19 | I/O34           | I/O49           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O139          | I/O154          | I/O171 | I/O185 | J |
| K | GND   | I/O20 | I/O35           | I/O50           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O140          | I/O155          | I/O172 | I/O186 | K |
| L | I/O5  | I/O21 | I/O36           | I/O51           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O141          | I/O156          | I/O173 | GND    | L |
| M | I/O6  | I/O22 | I/O37           | I/O52           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O142          | I/O157          | I/O174 | I/O187 | M |
| N | GND   | I/O23 | I/O38           | I/O53           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O143          | I/O158          | I/O175 | GND    | N |
| P | I/O7  | I/O24 | I/O39           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O159          | I/O176 | I/O188 | P |
| R | GND   | I/O25 | I/O40           | I/O54           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O144          | I/O160          | I/O177 | GND    | R |
| T | I/O8  | I/O26 | I/O41           | TCK             |                 |       |                 |       |       |       |       |        |        |                 |        |                 | TMS             | I/O161          | I/O178 | I/O189 | T |
| U | I/O9  | I/O27 | I/O42           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O162          | I/O179 | I/O190 | U |
| V | I/O10 | I/O28 | V <sub>CC</sub> | I/O55           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O145          | V <sub>CC</sub> | I/O180 | I/O191 | V |
| W | GND   | I/O29 | I/O43           | I/O56           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O146          | I/O163          | I/O181 | GND    | W |
| Y | GND   | I/O30 | GND             | I/O57           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O147          | GND             | I/O182 | I/O192 | Y |

#### Pin Designations

|                 |   |                  |
|-----------------|---|------------------|
| CLK             | = | Clock            |
| GND             | = | Ground           |
| I               | = | Input            |
| I/O             | = | Input/Output     |
| NC              | = | No Connect       |
| V <sub>CC</sub> | = | Supply Voltage   |
| TDI             | = | Test Data In     |
| TCK             | = | Test Clock       |
| TMS             | = | Test Mode Select |
| TDO             | = | Test Data Out    |

Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-026



## 5V M5 ORDERING INFORMATION<sup>1,2</sup>

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



### Note:

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

| Valid Combinations |                                                                               |                                   |
|--------------------|-------------------------------------------------------------------------------|-----------------------------------|
| M5-128/68          | Commercial:<br>-5, -7, -10, -12, -15<br>Industrial:<br>-7, -10, -12, -15, -20 | YC, VC, YI, VI                    |
| M5-128/104         |                                                                               | YC <sup>1</sup> , YI <sup>1</sup> |
| M5-128/120         |                                                                               | YC, YI                            |
| M5-192/68          |                                                                               | VC, VI                            |
| M5-192/120         |                                                                               | YC, YI                            |
| M5-256/68          |                                                                               | VC, VI                            |
| M5-256/120         |                                                                               | YC, YI                            |
| M5-256/160         |                                                                               | YC, YI                            |

### Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

| Valid Combinations |                                       |          |
|--------------------|---------------------------------------|----------|
| M5-320/160         | Commercial:<br>-6, -7, -10, -12, -15  | YC, YI   |
| M5-320/192         |                                       | SAC, SAI |
| M5-384/160         |                                       | YC, YI   |
| M5-512/160         | Industrial:<br>-7, -10, -12, -15, -20 | YC, YI   |
| M5-512/256         |                                       | SAC, SAI |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.  
See Ordering Information section for product status.