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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-256-68-7vc-1



Table 1. MACH 5 Device Features ¹

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	160	160	160	256	256
t _{PD} (ns)	5.5	5.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	6.5	6.5
t _{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t _{COS} (ns)	4.5	4.5	4.5	4.5	4.5	5.0	5.0	5.0	5.0	5.0	5.0
f _{CNT} (MHz)	182	182	182	182	182	167	167	167	167	167	167
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

GENERAL DESCRIPTION

The MACH[®] 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E²CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.
See Ordering Information section for product status.



20446G-002

Figure 2. PAL Block Structure

Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 or 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 4. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂ , C ₃ , C ₄	M ₈	C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₁	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅	M ₉	C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₂	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆	M ₁₀	C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₃	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₁	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₄	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₂	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₅	C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈	M ₁₃	C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉	M ₁₄	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀	M ₁₅	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅

Select devices have been discontinued.
See Ordering Information section for product status.

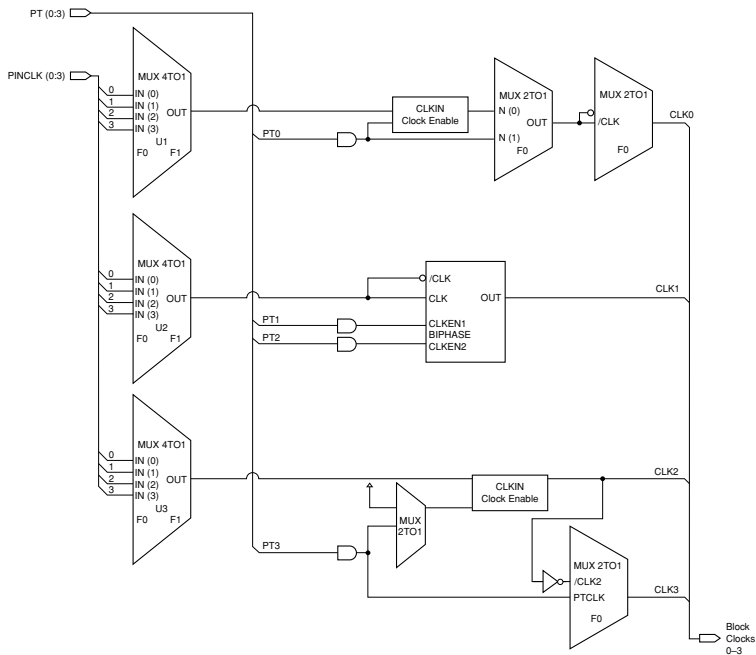
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

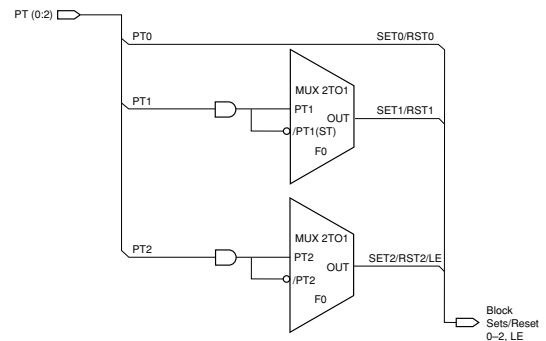
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator



20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.
See Ordering Information section for product status.**

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

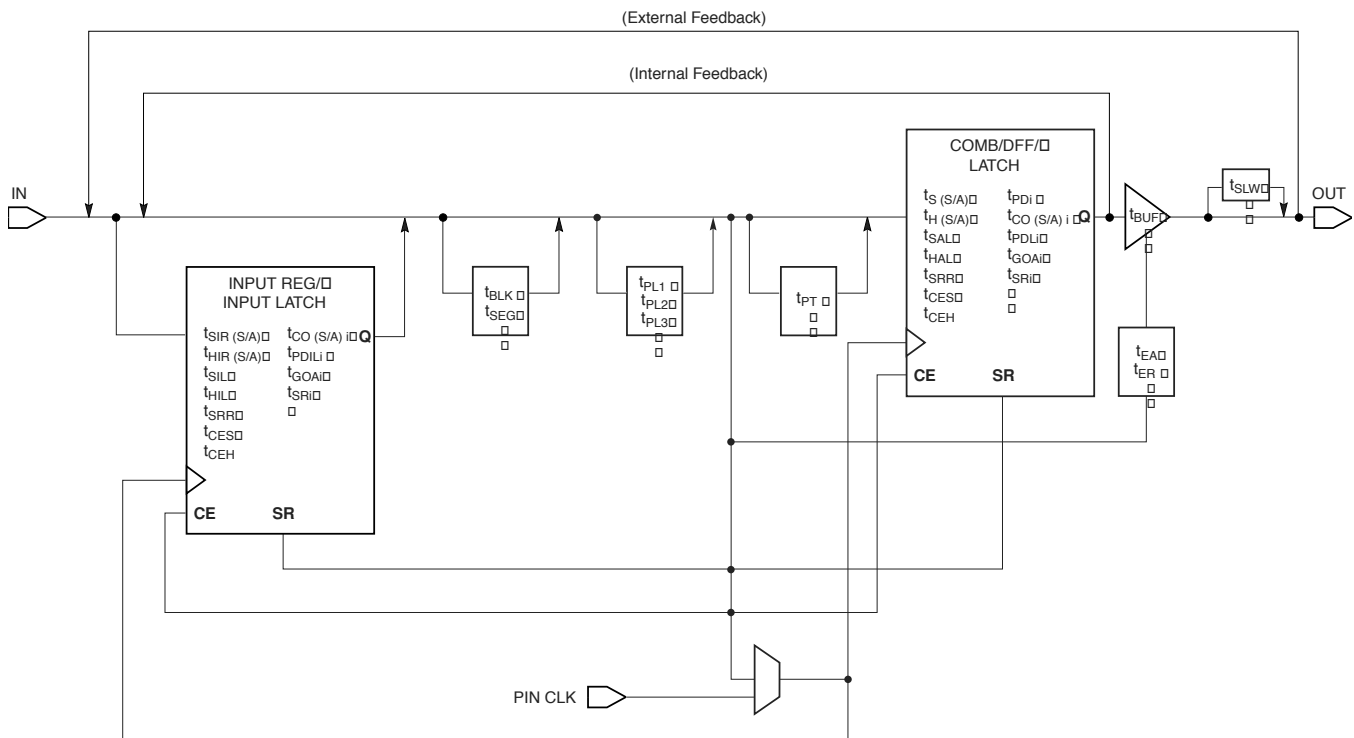


Figure 7. MACH 5 Timing Model

20446G-014

Select devices have been discontinued.
See Ordering Information section for product status.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

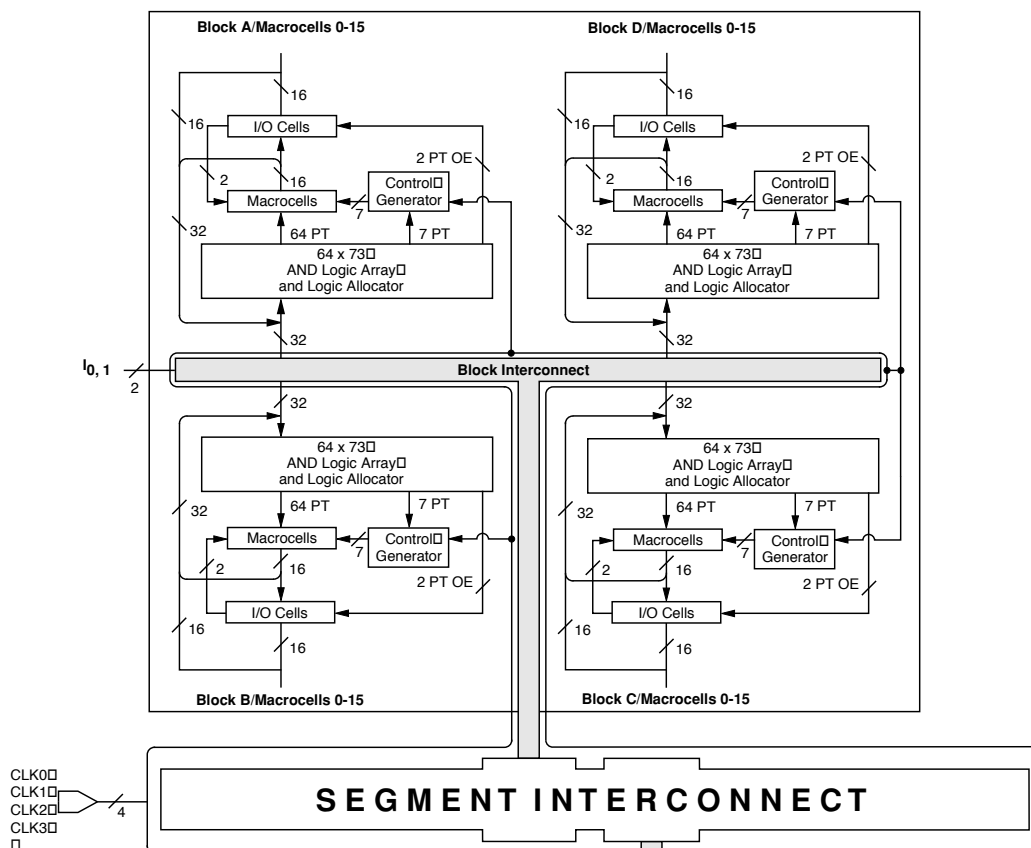
POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

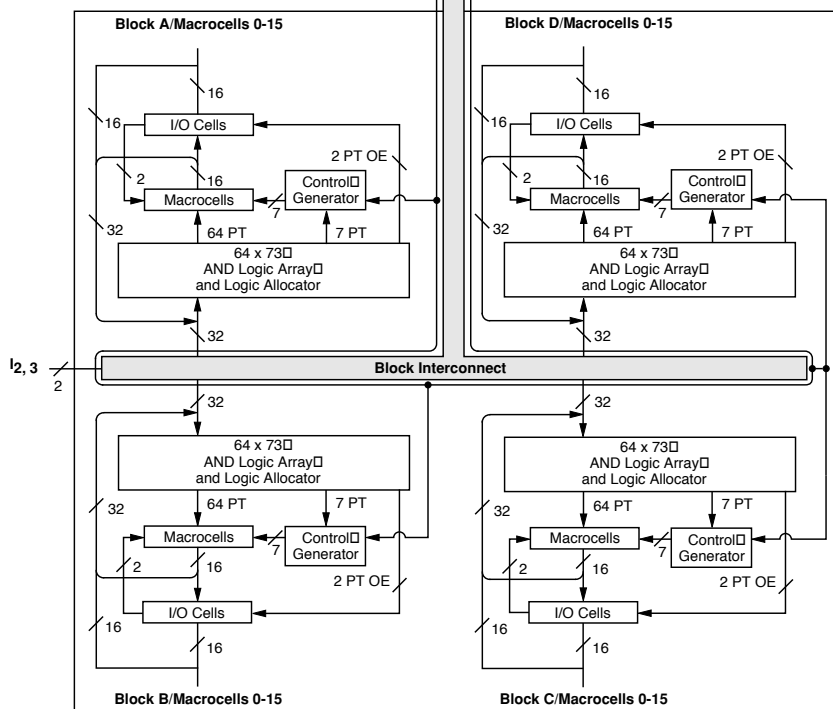
Select devices have been discontinued. See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0



SEGMENT 1

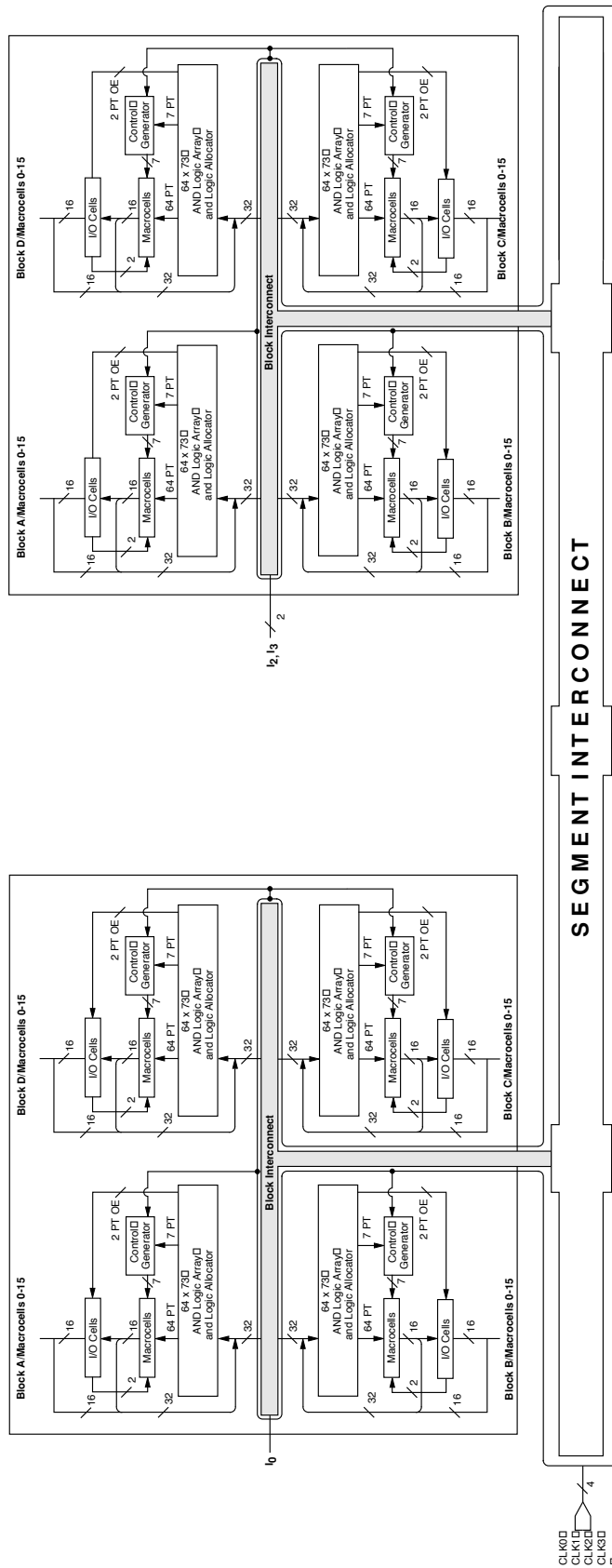


Select devices have been discontinued.
See Ordering Information section for product status.

20446G-007

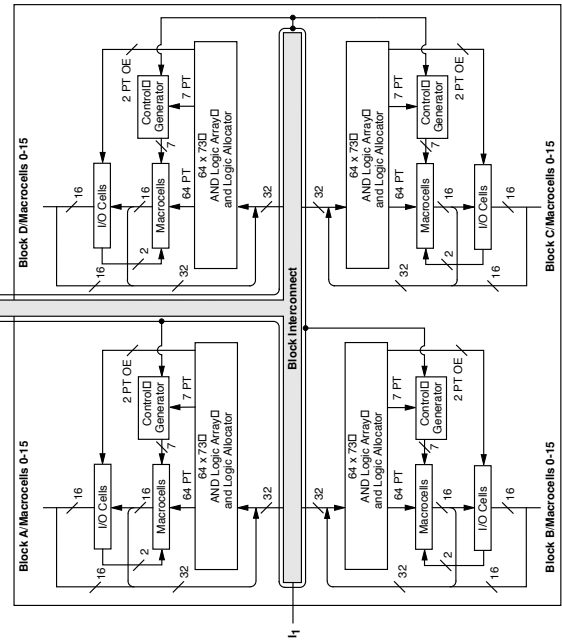
BLOCK DIAGRAM — M5-192/XXX

SEGMENT 2



SEGMENT INTERCONNECT

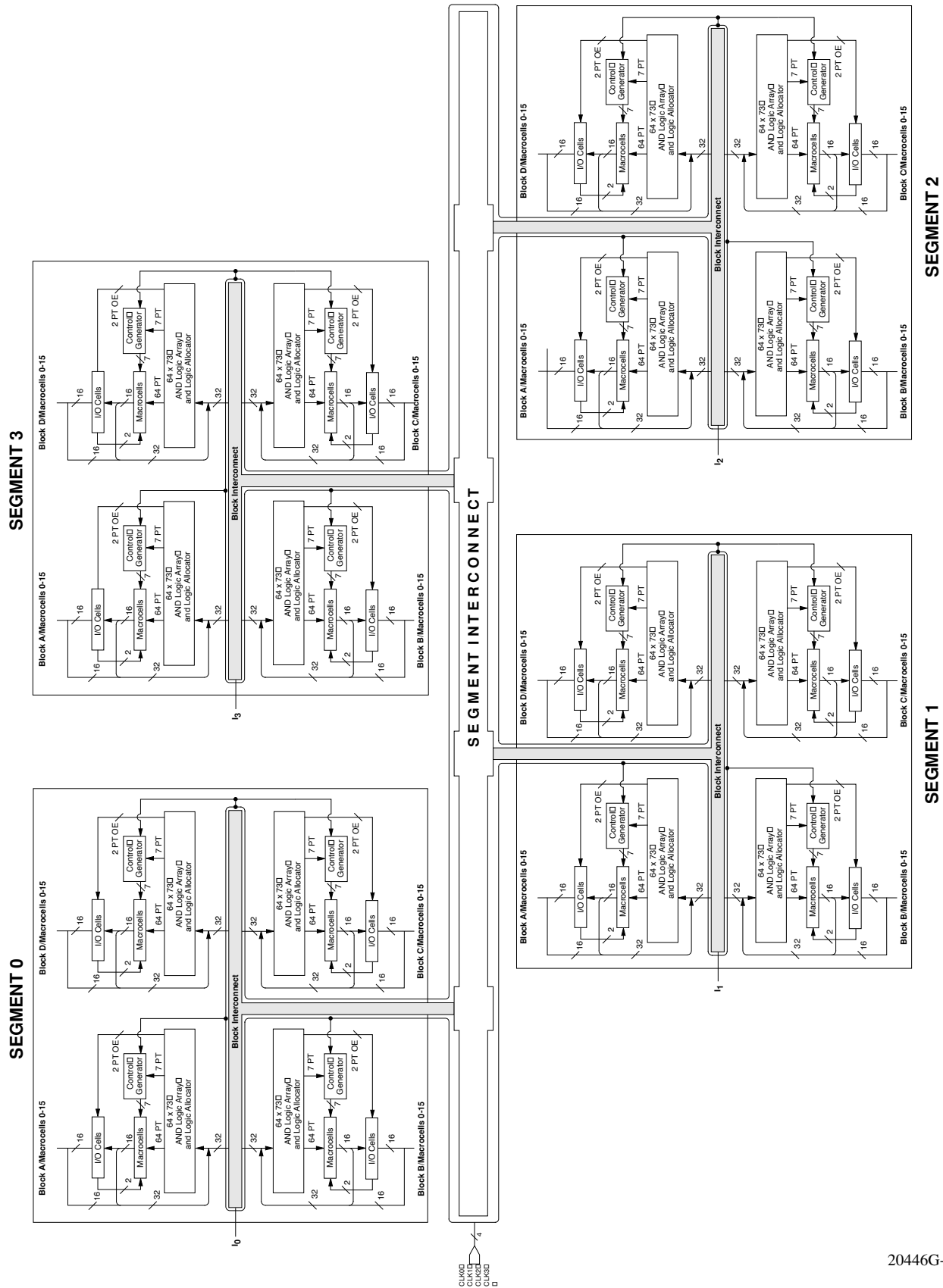
SEGMENT 1



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-008

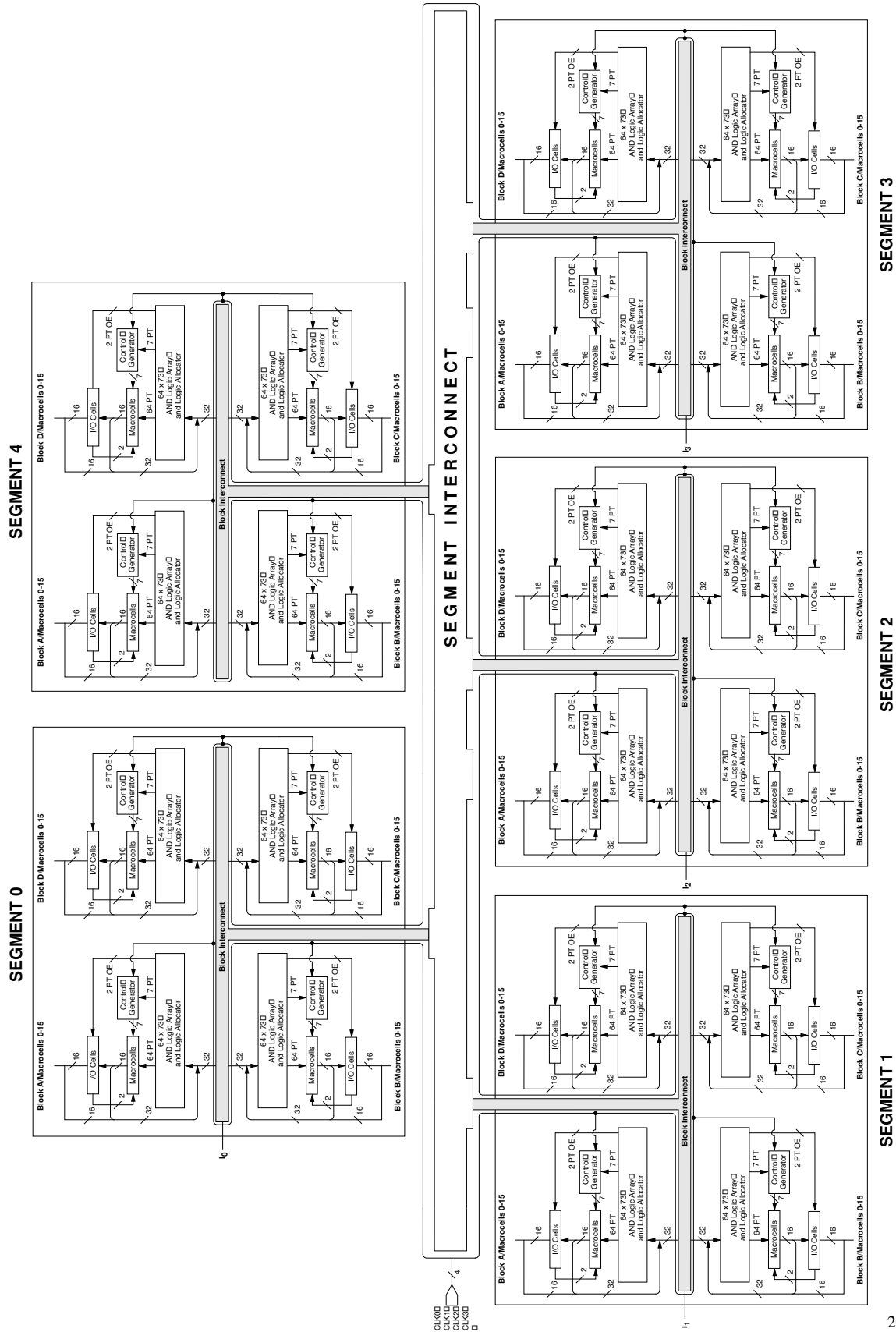
BLOCK DIAGRAM — M5(LV)-256/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-009

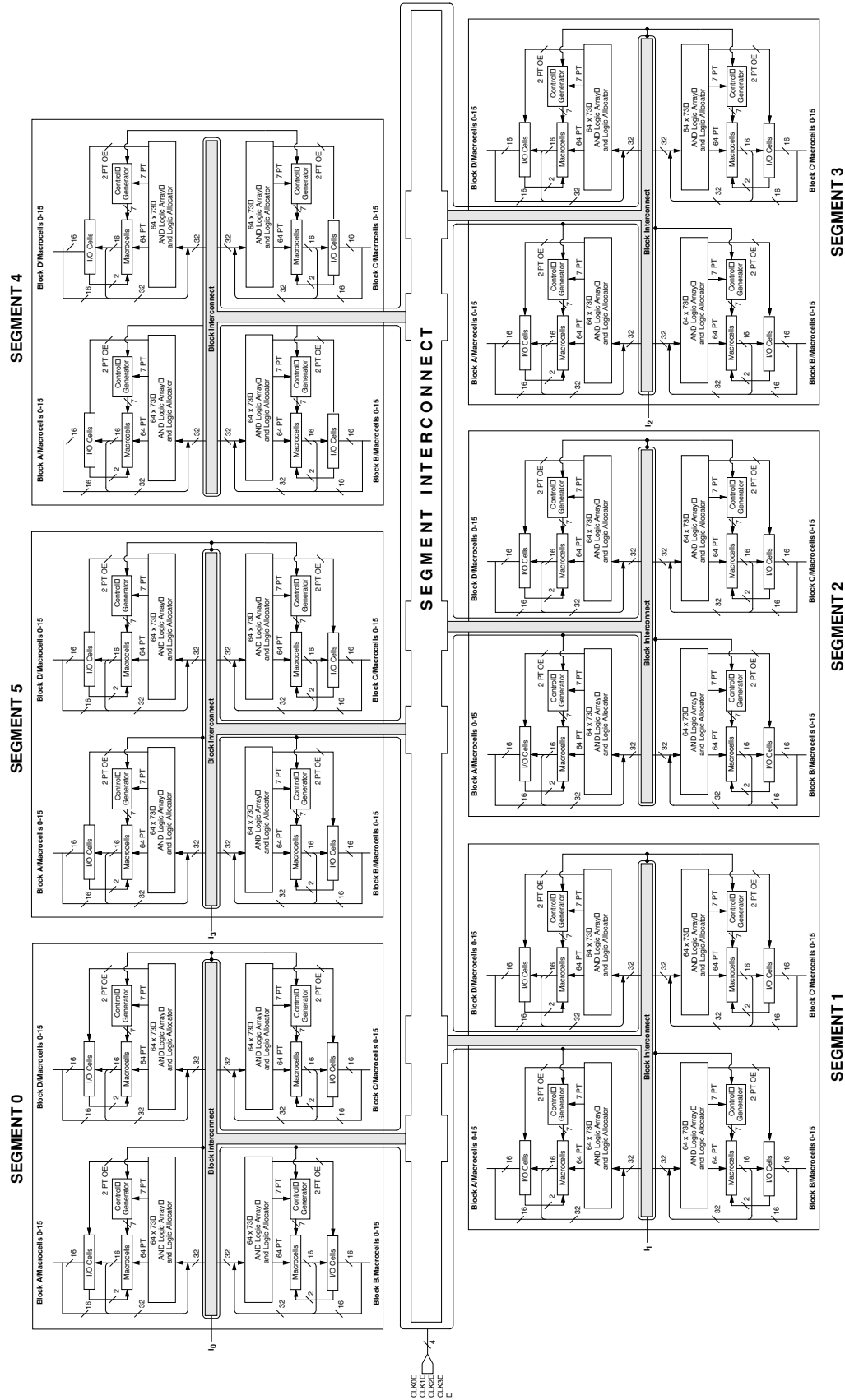
BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-010

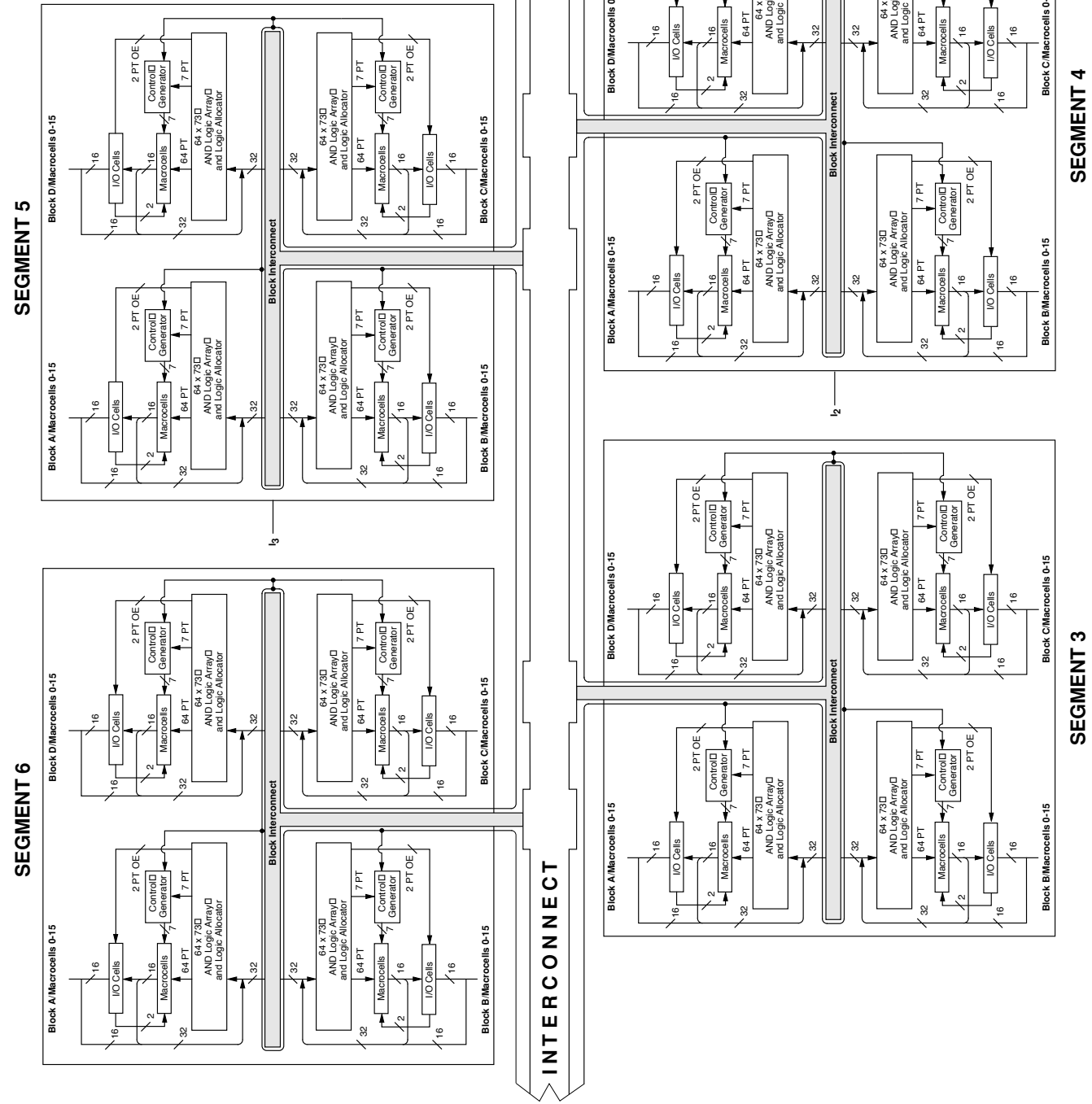
BLOCK DIAGRAM — M5(LV)-384/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-011

BLOCK DIAGRAM — M5(LV)-512/XXX



Continued

Select devices have been discontinued.
See Ordering Information section for product status.

ABSOLUTE MAXIMUM RATINGS

M5LV

Storage Temperature. -65°C to +150°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +4.5 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued.
See Ordering Information section for product status.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 3.2 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 100 \mu A$		0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16 \text{ mA (Note 1)}$		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-15	-160	mA

Notes:

1. Total I_{OL} between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																
f _{MAX}	External feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{HS})	200		167		167		125		100		83.3		83.3		MHz
f _{MAXA}	External feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{HA})	167		125		125		100		83.3		71.4		62.5		MHz
f _{MAXI}	Maximum input register frequency 1/(t _{SIRS} +t _{HIRS}) or 1/(2 x t _{WICW})	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).

Select devices have been discontinued.
See Ordering Information section for product status.

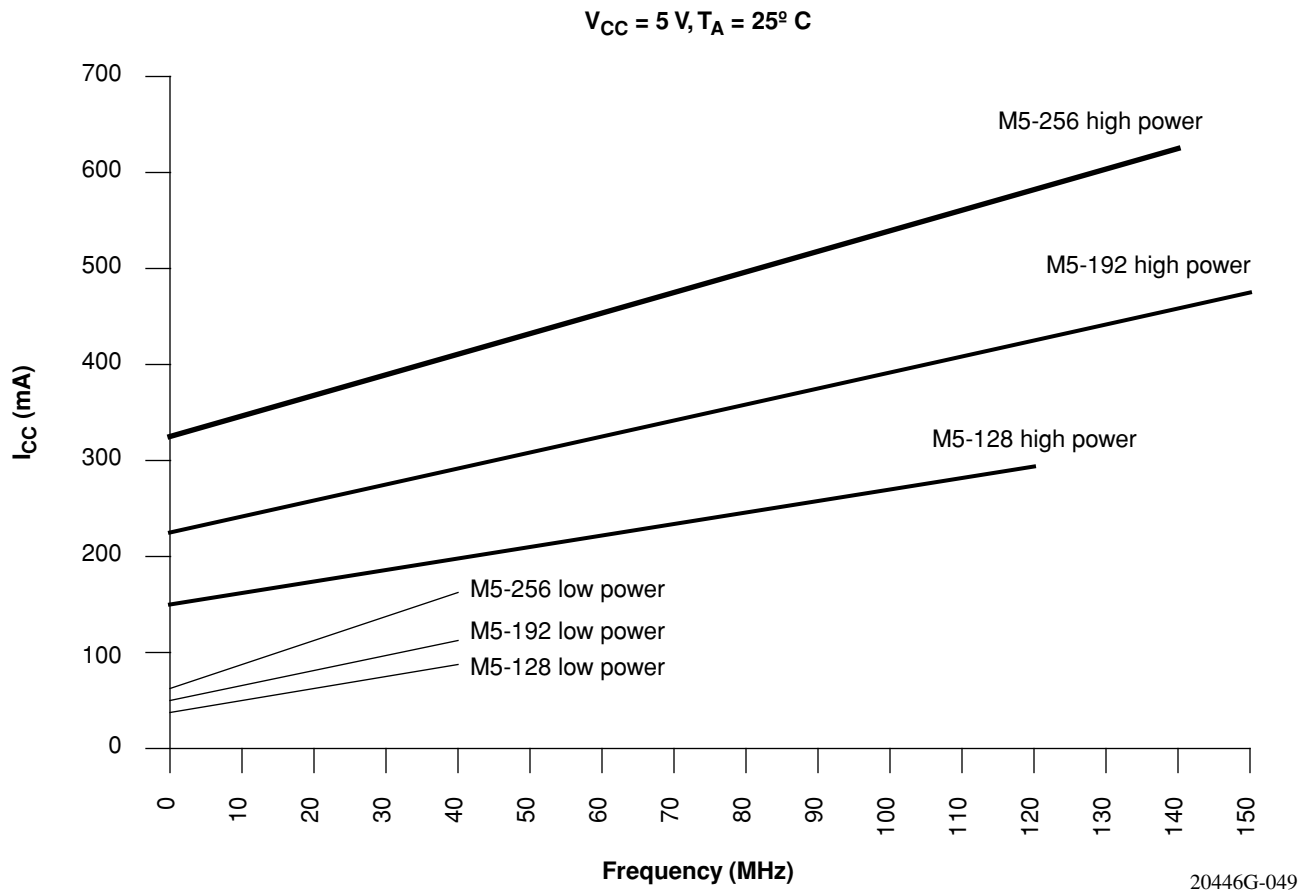


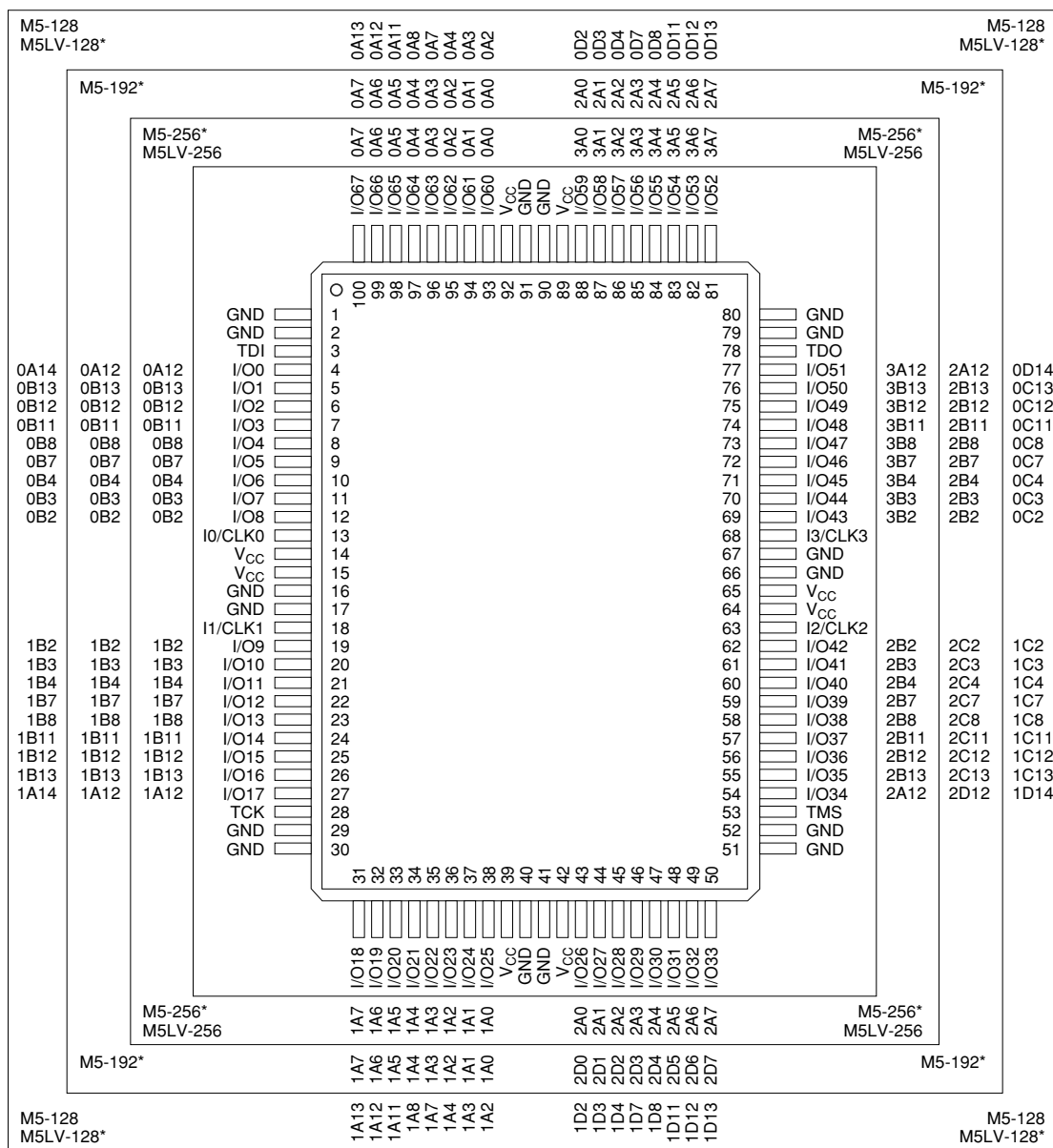
Figure 9. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued.
See Ordering Information section for product status.

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)



*Package obsolete, contact factory.

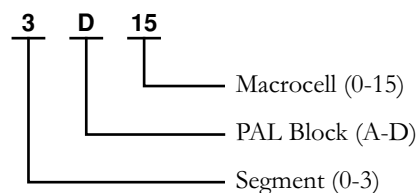
20446G-016

Select devices have been discontinued.
See Ordering Information section for product status.

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

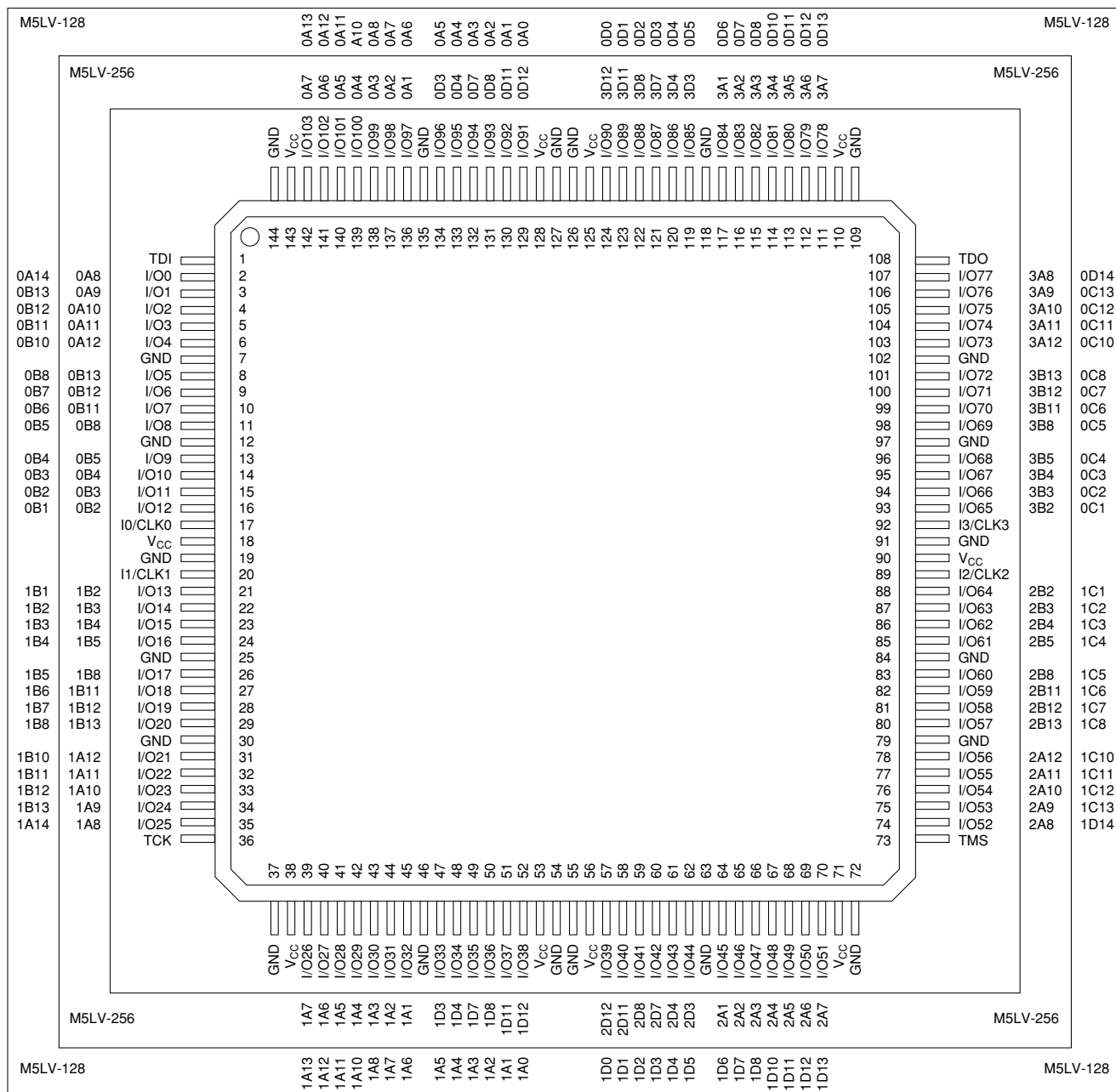
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



144-PIN TQFP CONNECTION DIAGRAM

Top View

144-Pin TQFP



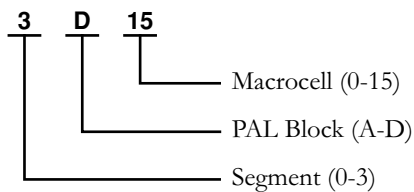
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-020

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

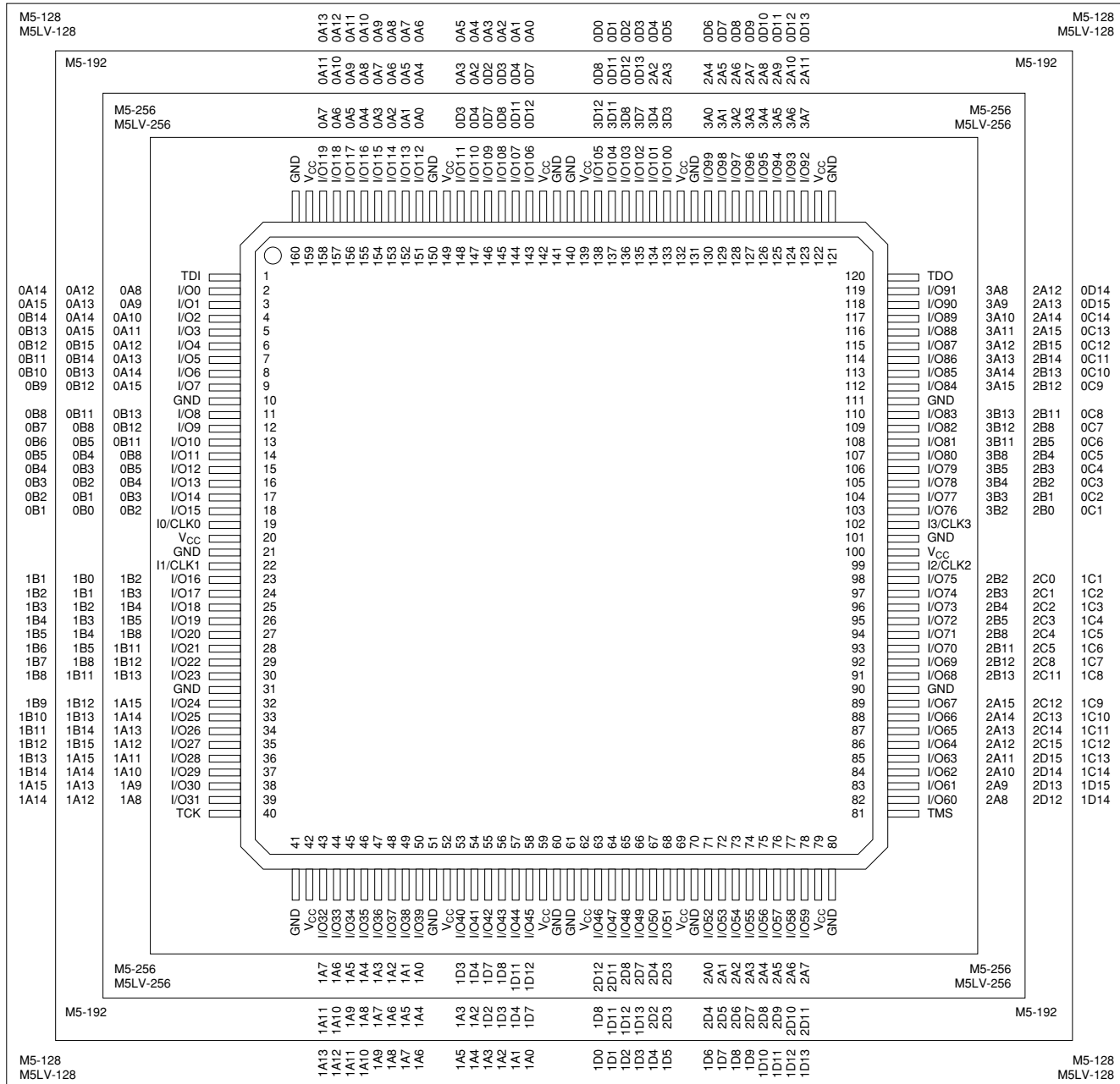


160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

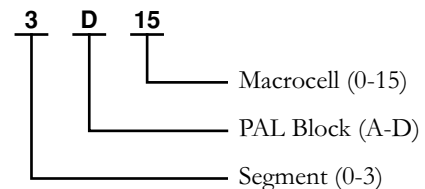
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See Ordering Information section for product status.



Pin Designations

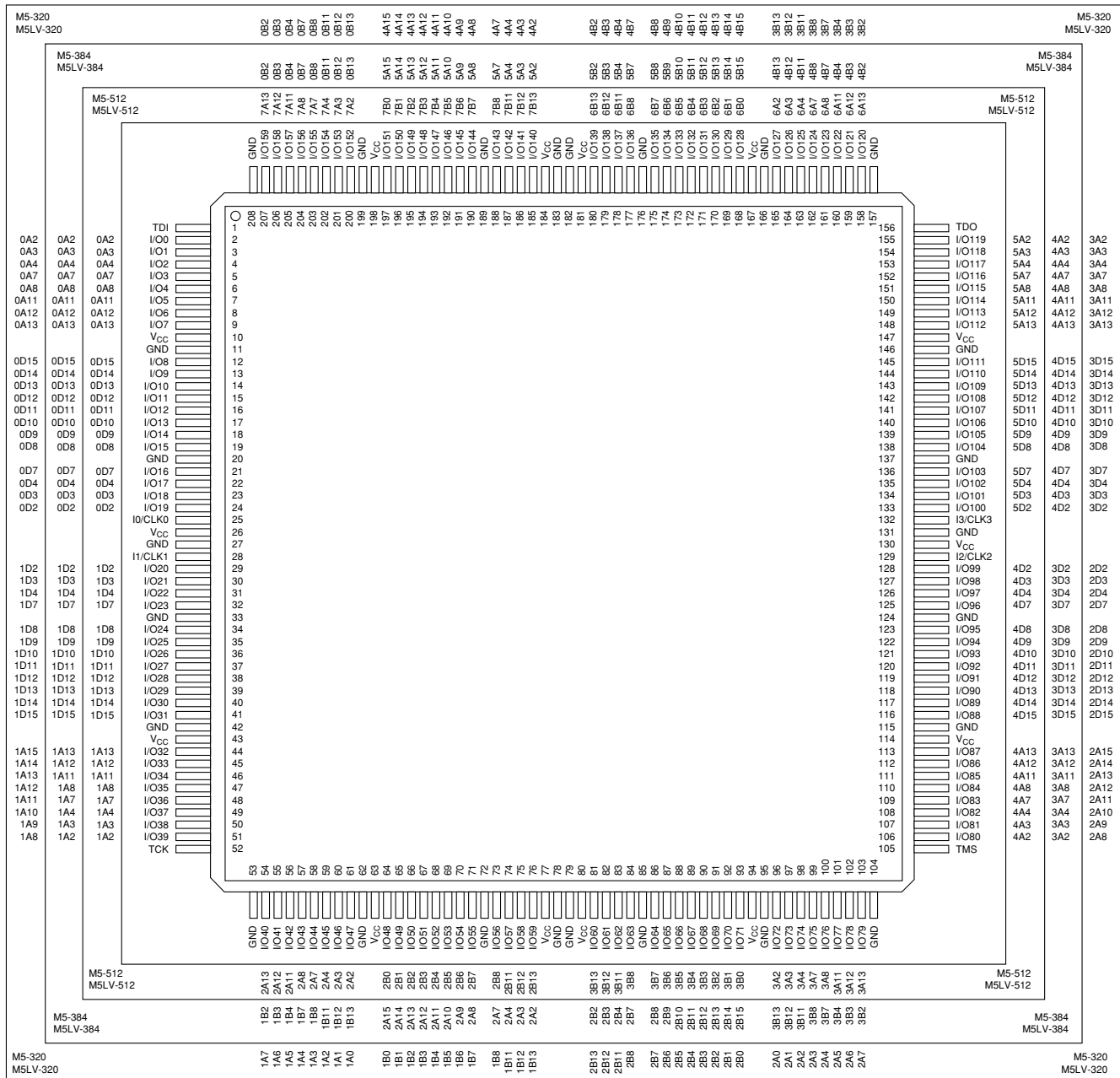
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

208-Pin PQFP (320, 384, 512 Macrocells)



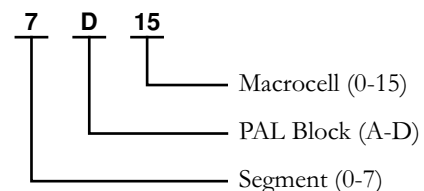
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-024

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (Macrocell Association)

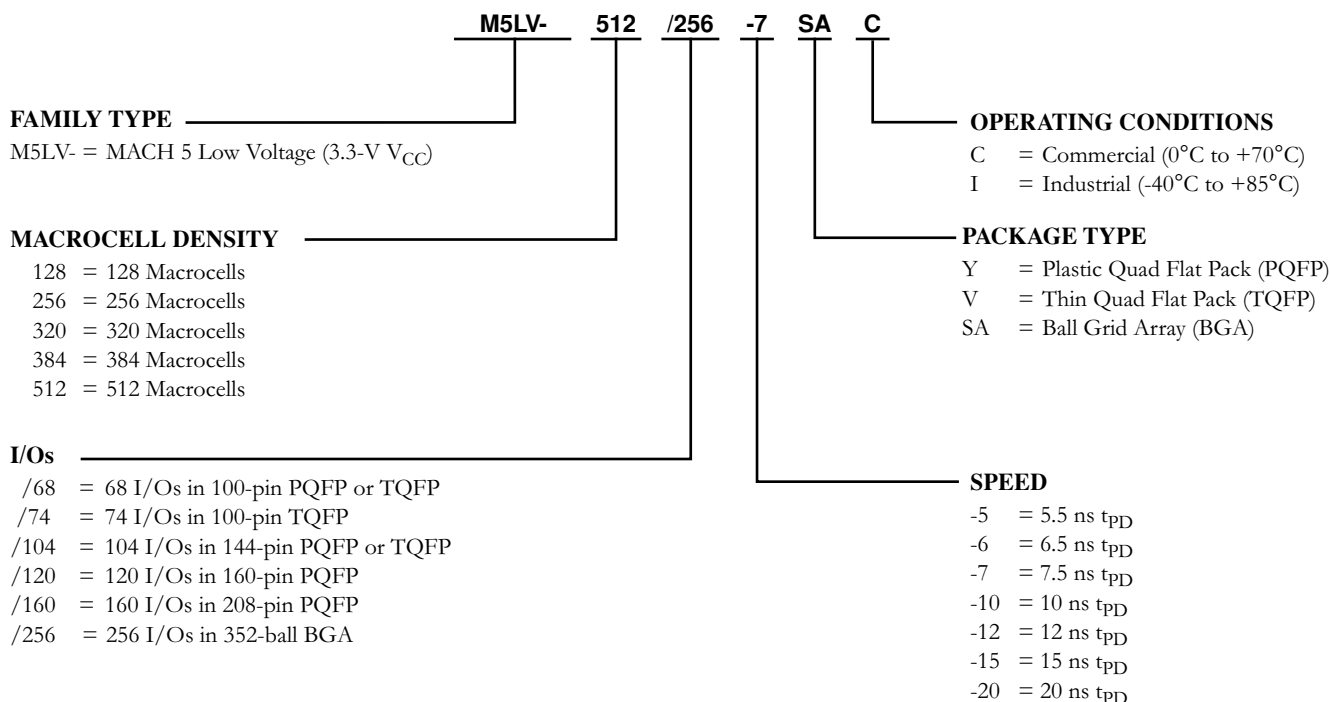
256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2D10	2D13	2D15	GND	GND	1
2	GND	3B2	3A3	3A8	3A13	3D13	3D9	3D8	3D4	13/CLK3	12/CLK2	2D3	2D4	2D8	2A14	2A15	2A13	2A12	2A9	2A7	2
3	GND	3B8	V _{CC}	3A2	3A4	3A12	3D14	3D10	3D5	3D0	2D0	2D5	2D9	2D14	2A11	2A10	2A8	V _{CC}	2A3	GND	3
4	3B13	3B11	3B3	V _{CC}	TDO	3A7	V _{CC}	3D11	3D6	3D1	2D1	2D6	2D11	V _{CC}	2A11	TMS	V _{CC}	2A6	2A2	2A0	4
5	4B14	4B15	3B4	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 4 D 15 Macrocell (0-15) PAL Block (A-D) Segment (0-4) <td>V_{CC}</td> <td>2A4</td> <td>2A1</td> <td>2B4</td> <td>GND</td> <td>2B1</td> <td>5</td>	V _{CC}	2A4	2A1	2B4	GND	2B1	5									
6	GND	4B11	3B12	3B7		V _{CC}	2B3	2B6	2B9	2B11	GND	2B8	2B10	2B12	GND	2B7	6				
7	4B8	4B10	4B13	V _{CC}		2B8	2B13	2B14	2B15	GND	1B13	1B8	1B10	1B12	GND	1B7	7				
8	4B4	4B6	4B9	4B12		2B13	1B3	1B6	1B9	1B11	1B14	1B3	1B10	1B12	1B11	1B7	8				
9	GND	4B3	4B5	4B7		2B8	V _{CC}	1B2	1B5	GND	1A4	1A1	1B2	1B5	GND	1A8	9				
10	GND	4B0	4B1	4B2		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	10				
11	GND	4A0	4A1	4A2		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	11				
12	GND	4A3	4A5	4A7		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	12				
13	4A4	4A6	4A9	4A12		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	13				
14	4A8	4A10	4A13	V _{CC}		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	14				
15	GND	4A11	0B12	0B7	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	15					
16	4A14	4A15	0B4	V _{CC}	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	16					
17	0B13	0B11	0B3	V _{CC}	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	17					
18	GND	0B8	V _{CC}	0A2	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	18					
19	0B2	0A3	0A8	0A11	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	19					
20	GND	GND	0D15	0D13	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	20					
A	0D10	0A13	0A4	0A7	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	A					
B	GND	0D12	0D14	0D11	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	B					
C	0D7	0D8	0D4	0D5	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	C					
D	GND	0D2	0D3	0D0	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	D					
E	GND	10/CLK0	1D2	1D0	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	E					
F	1D3	1D4	1D8	1D10	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	F					
G	GND	1D7	1D9	1D14	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	G					
H	GND	1D12	1A13	1A10	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	H					
J	1D13	1A14	1A11	TCK	2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	J					
K	1D15	1A16	1A0		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	K					
L	GND	1A17	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	L					
M	GND	1A19	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	M					
N	GND	1A20	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	N					
P	GND	1A21	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	P					
R	GND	1A22	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	R					
T	GND	1A23	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	T					
U	GND	1A24	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	U					
V	GND	1A25	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	V					
W	GND	1A26	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	W					
Y	GND	1A27	GND		2B13	1B3	1B6	1B9	1B11	1A4	1A1	1B2	1B5	GND	1A8	Y					

Select devices have been discontinued.
See Ordering Information section for product status.

3.3V M5LV ORDERING INFORMATION¹

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68	Industrial: -7, -10, -12, -15	YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15	YC, YI
M5LV-320/160		YC, YI
M5LV-384/120		YC, YI
M5LV-384/160		YC, YI
M5LV-512/120	Industrial: -10, -12, -15, -20	YC, YI
M5LV-512/160		YC, YI
M5LV-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.