Lattice Semiconductor Corporation - M5-320/192-7SAC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	320
Number of Gates	-
Number of I/O	192
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-SBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5-320-192-7sac

Table 1. MACH 5 Device Features [1]

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	160	160	160	256	256
t_{PD} (ns)	5.5	5.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	6.5	6.5
t_{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t_{COS} (ns)	4.5	4.5	4.5	4.5	4.5	5.0	5.0	5.0	5.0	5.0	5.0
f_{CNT} (MHz)	182	182	182	182	182	167	167	167	167	167	167
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

GENERAL DESCRIPTION

The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E^2CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Table 2. MACH 5 Speed Grades

Device	Speed Grade[1]						
	-5	-6	-7	-10	-12	-15	-20
M5-128[2]			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C,I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256[2]			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	C, I	I

Note:

1. *C = Commercial grade, I = Industrial grade*
2. */1 version recommended for new designs*

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL® block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options [1]

	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage	**5**	**3.3**	**5**	**5**	**3.3**	**5**	**3.3**	**5**	**3.3**	**5**	**3.3**
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

Note:

1. *The I/O options indicated with a "*" are obsolete, please contact factory for more information.*

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.

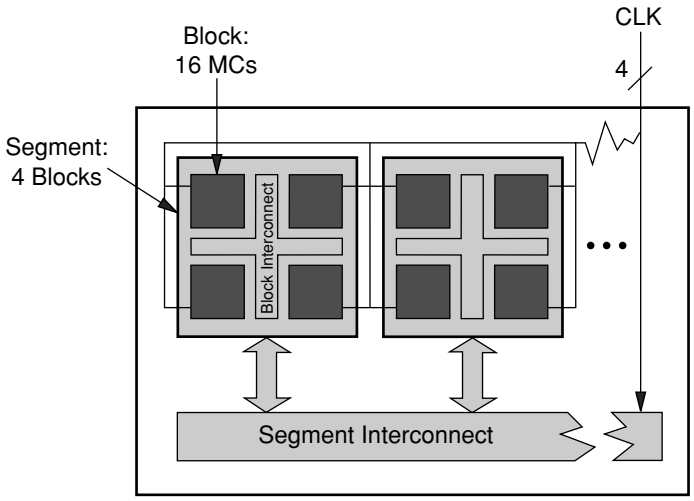

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Figure 1. MACH 5 Block Diagram

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- I/O cells
- Product-term array and Logic Allocator
- Macrocells
- Register control generator
- Output enable generator

I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The
I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as "buried" macrocells to drive device logic via the matrix.

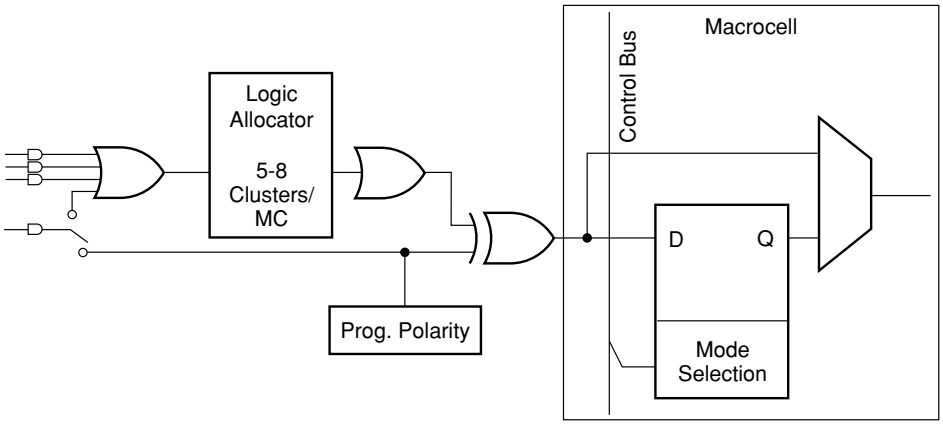

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Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 1 Options

- Global clock (0, 1, 2, or 3) with positive edge clock enable
- Global clock (0, 1, 2, or 3) with negative edge clock enable

- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- Global clock (0, 1, 2, or 3) with clock enable

Clock Line 3 Options

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable

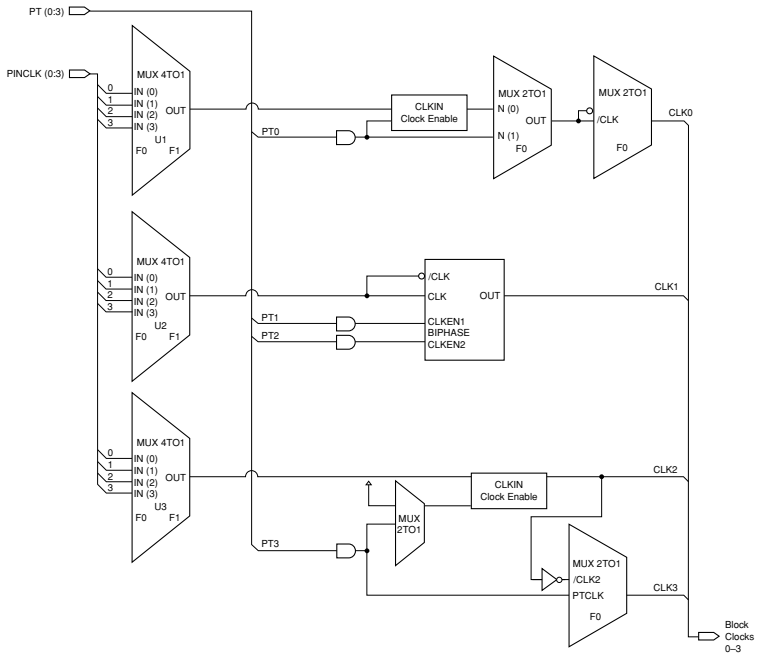

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Figure 4. Clock Generator

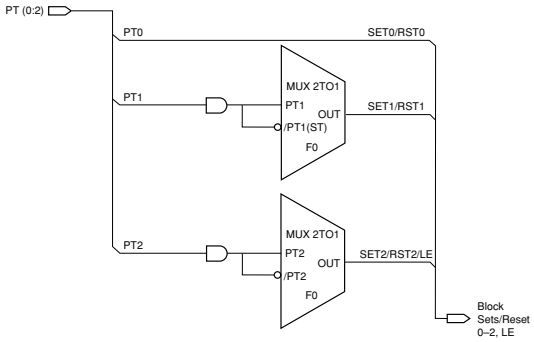

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Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

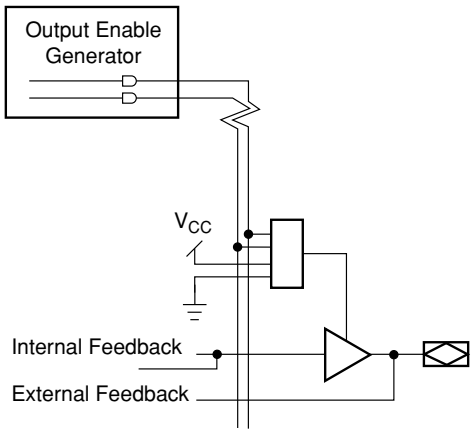

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Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

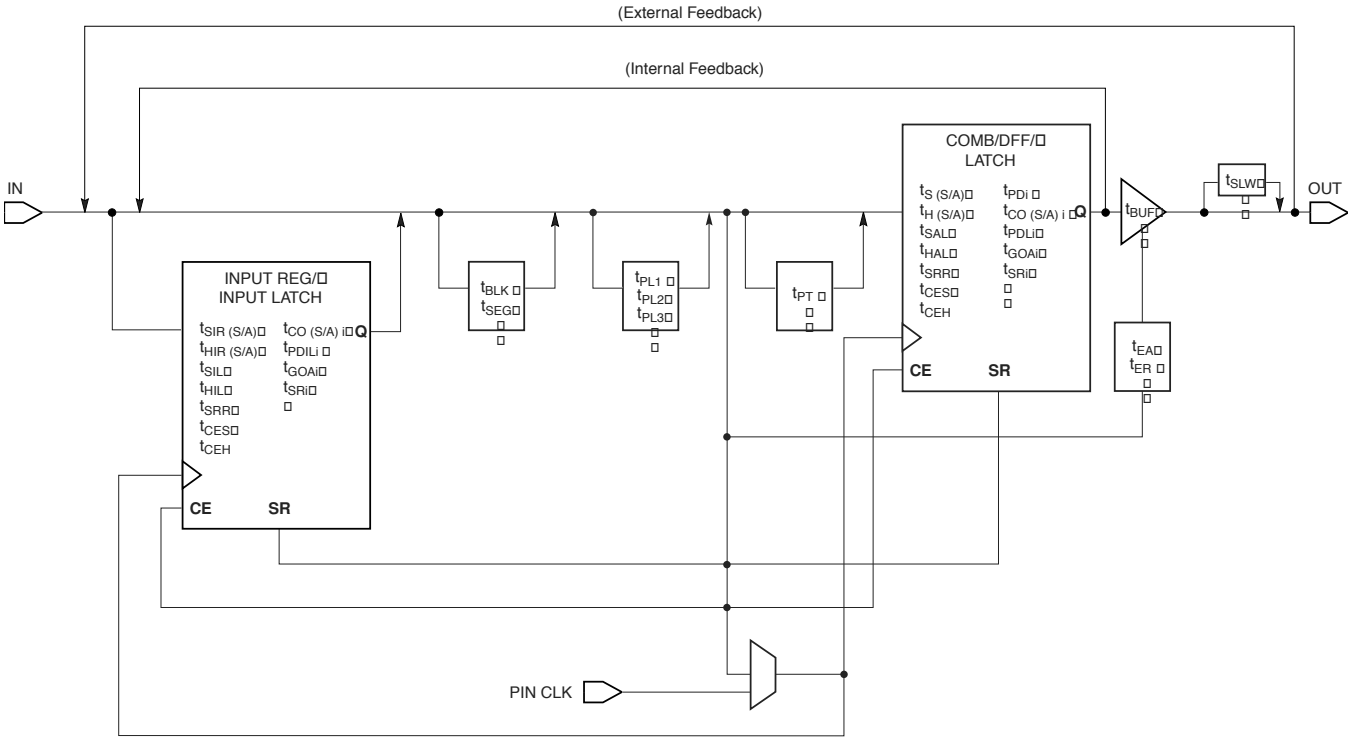

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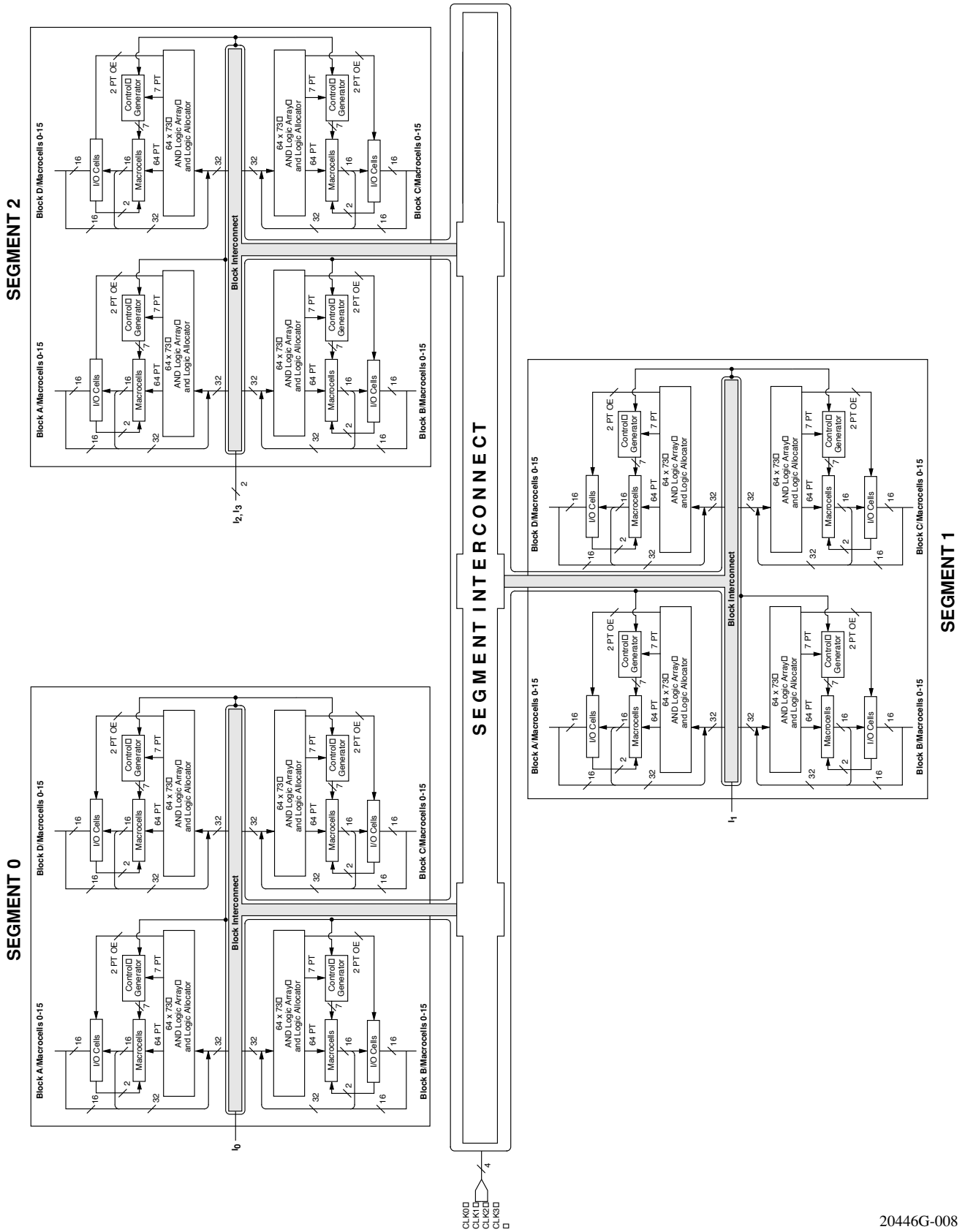
Figure 7. MACH 5 Timing Model

SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

BLOCK DIAGRAM — M5-192/XXX



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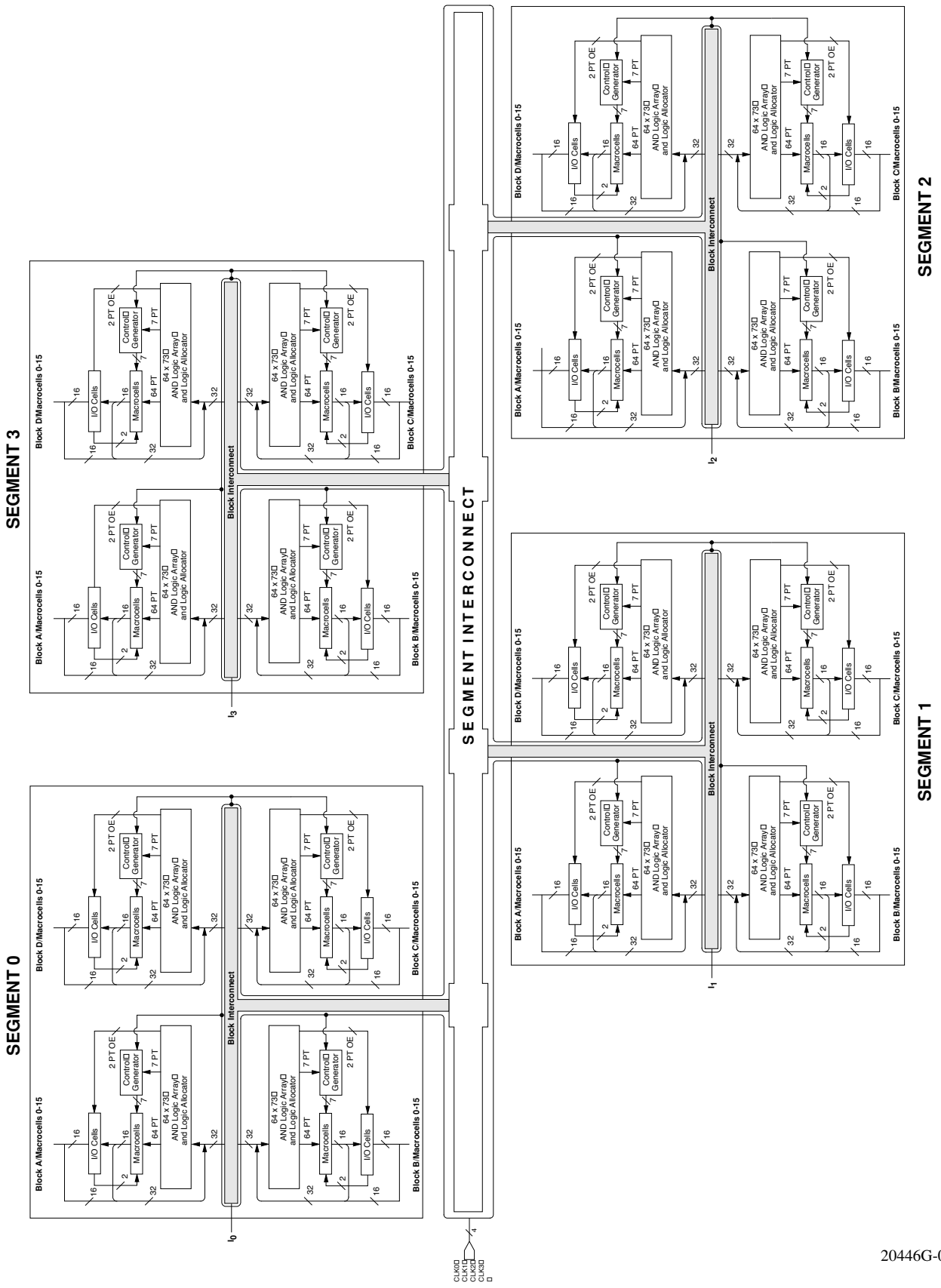
Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-256/XXX



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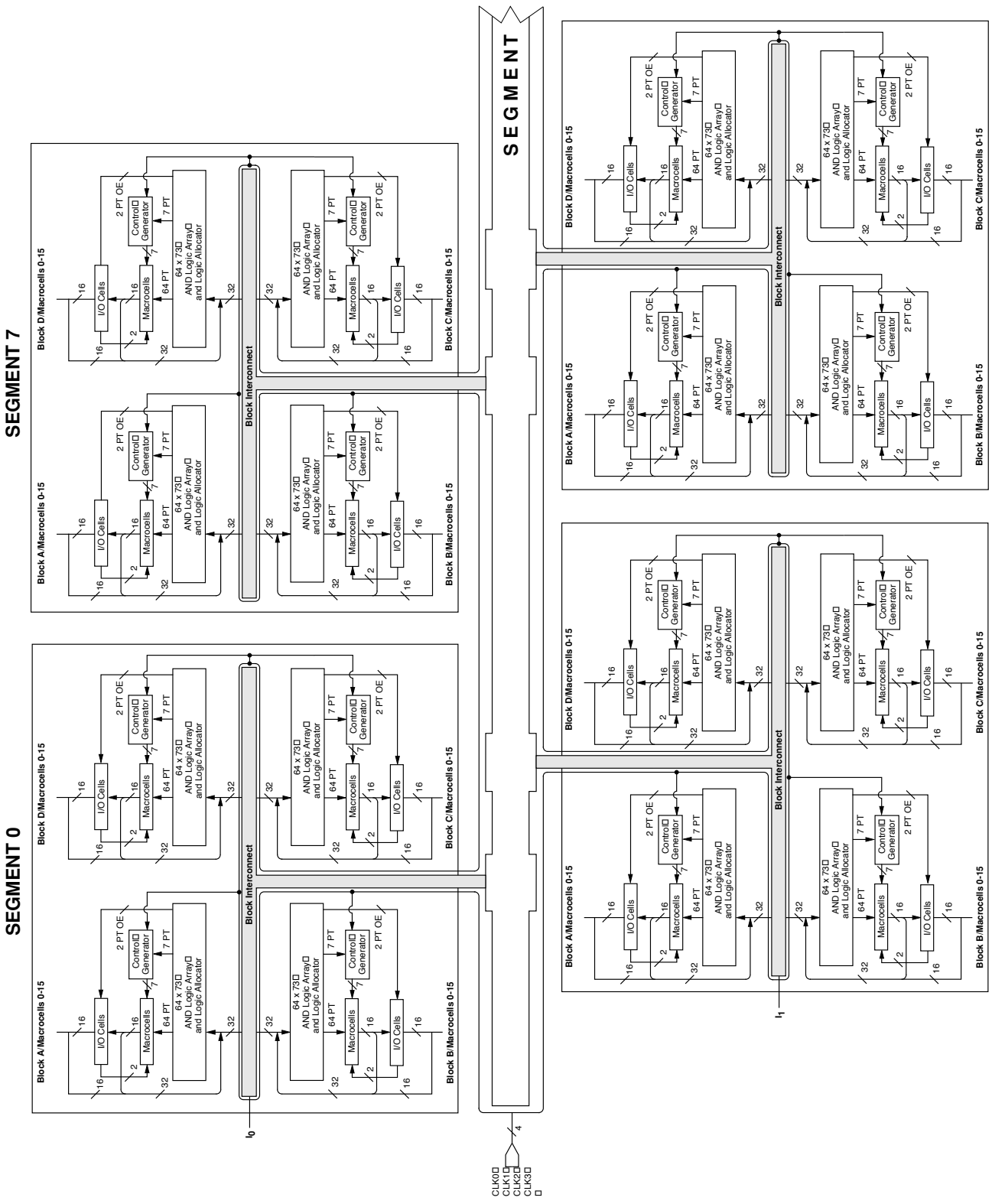
Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-512/XXX

Continued



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-012

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																
f_{MAX}	External feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{HS})$	200		167		167		125		100		83.3		83.3		MHz
f_{MAXA}	External feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{HA})$	167		125		125		100		83.3		71.4		62.5		MHz
f_{MAXI}	Maximum input register frequency $1/(t_{SIRS}+t_{HIRS})$ or $1/(2 \times t_{WICW})$	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

1. *See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.*
2. *Numbers in parentheses are for M5-128, M5-192, M5-256.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} =2.0 V	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} =2.0 V	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

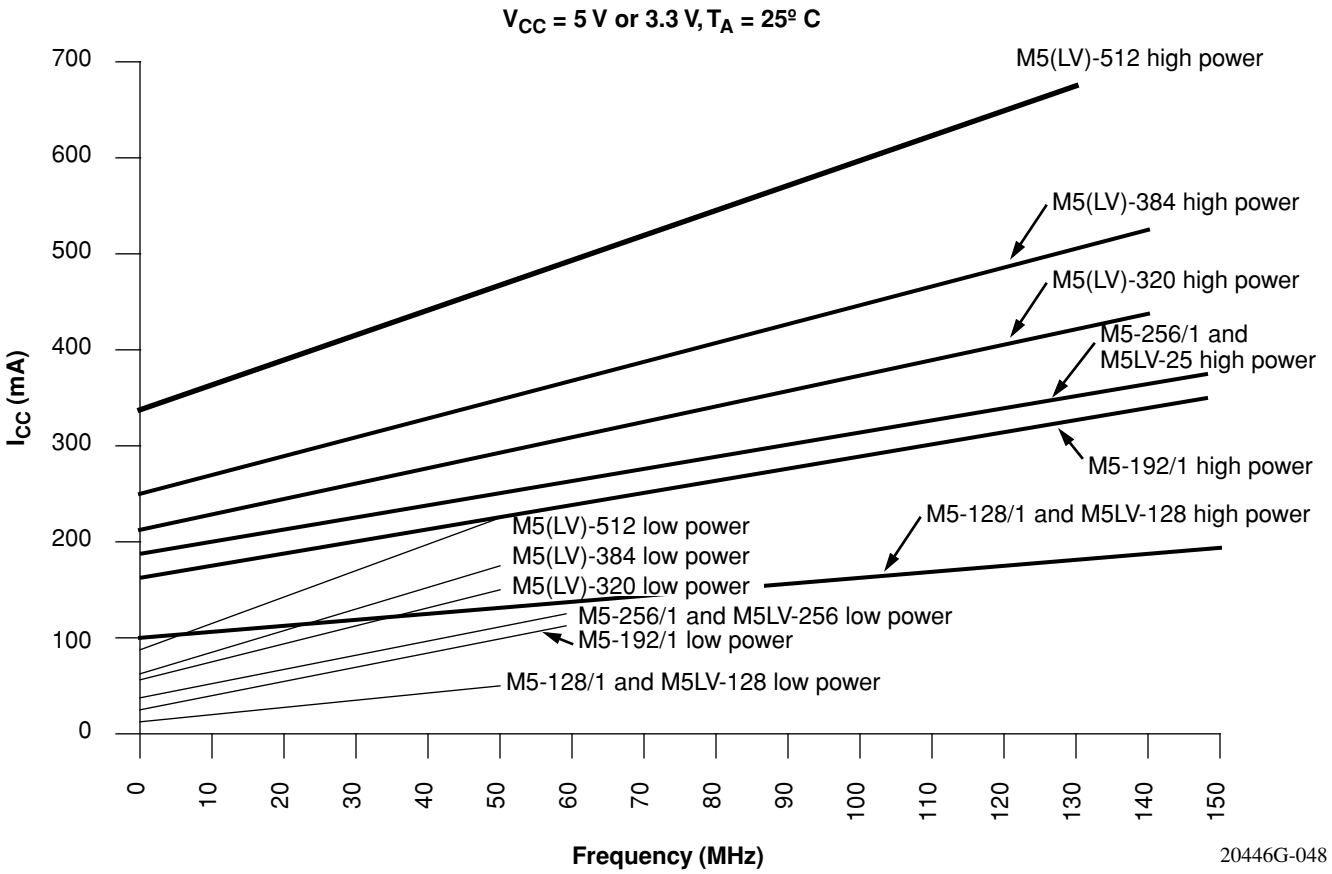


Figure 8. I_{CC} Curves at High/Low Power Modes

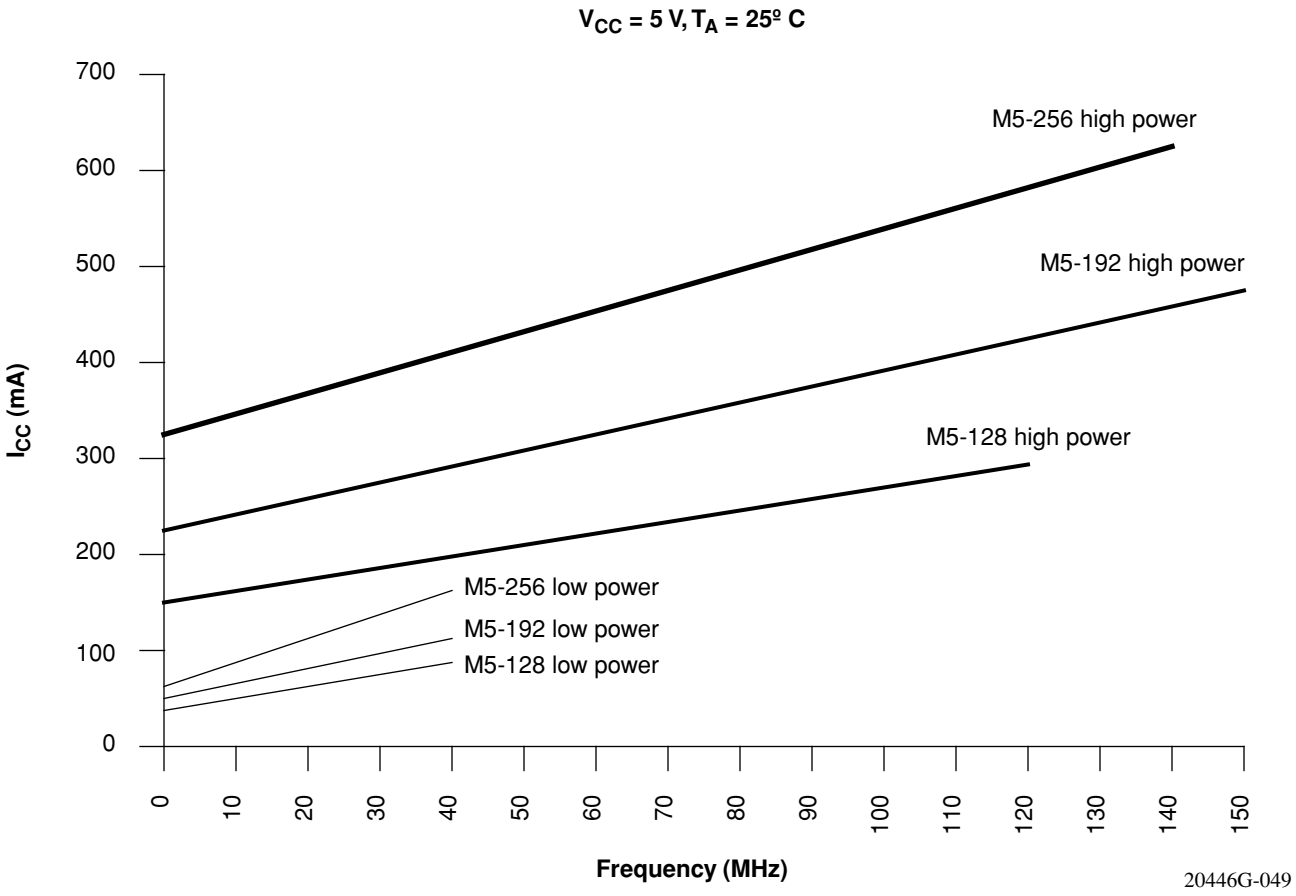
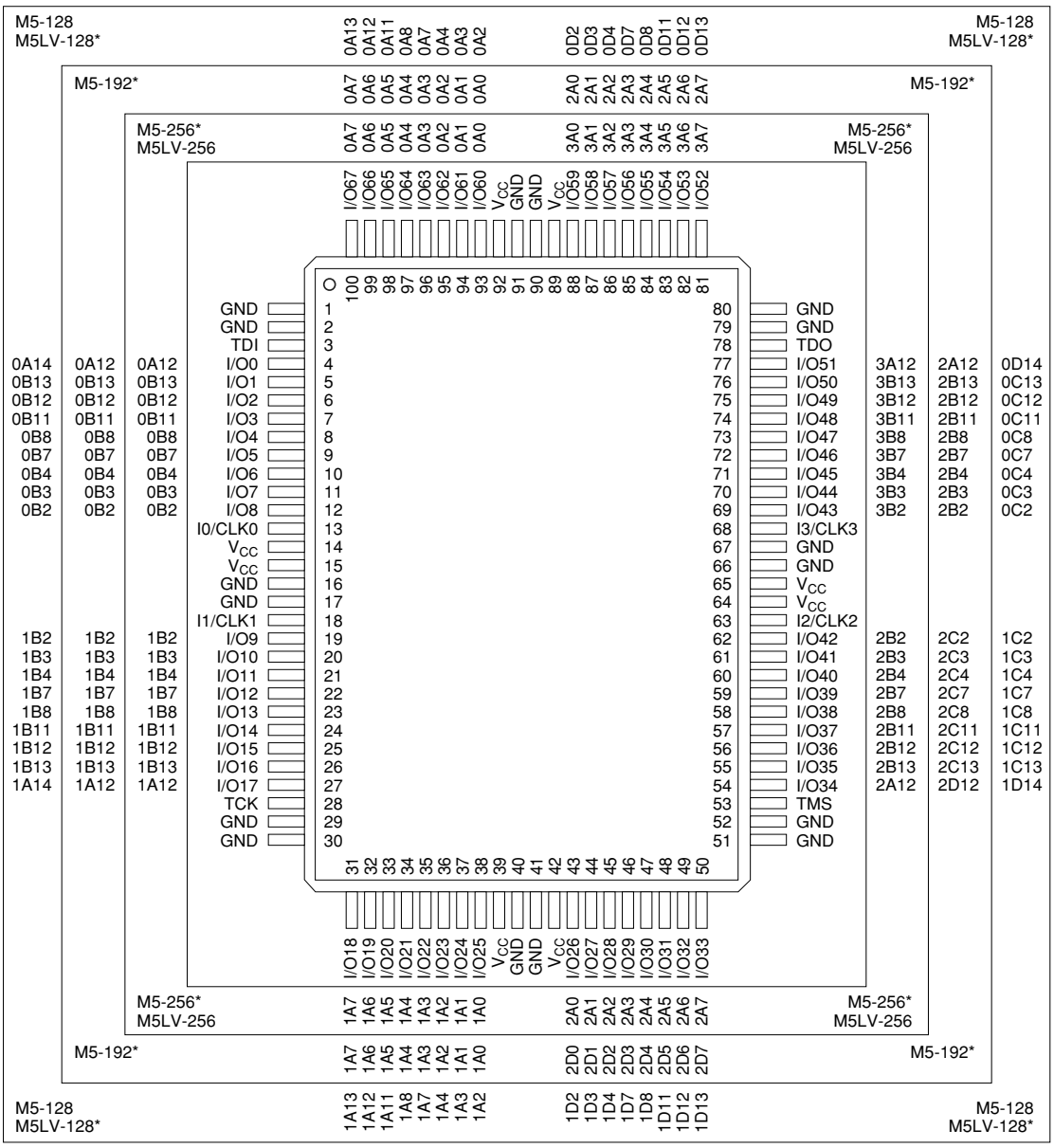


Figure 9. I_{CC} Curves at High/Low Power Modes

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)



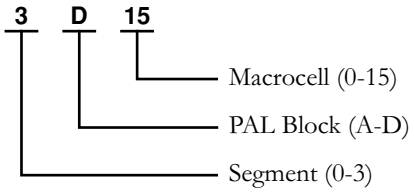
*Package obsolete, contact factory.

20446G-016

Select devices have been discontinued. See Ordering Information section for product status.

Pin Designations

CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (I/O Pin-outs)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	I/O181	I/O182	I/O183	GND	I/O184	GND	I/O185	I/O186	GND	I/O187	GND	I/O188	GND	I/O189	I/O190	I/O191	GND	GND	1
2	GND	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I3/CLK3	I2/CLK2	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	2
3	GND	I/O148	V_{CC}	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	V_{CC}	I/O163	GND	3
4	I/O134	I/O135	I/O136	V_{CC}	TDO	I/O137	V_{CC}	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	V_{CC}	I/O144	TMS	V_{CC}	I/O145	I/O146	I/O147	4
5	I/O128	I/O129	I/O130	V_{CC}													V_{CC}	I/O131	I/O132	I/O133	5
6	GND	I/O122	I/O123	I/O124													I/O125	I/O126	I/O127	GND	6
7	I/O116	I/O117	I/O118	V_{CC}													V_{CC}	I/O119	I/O120	I/O121	7
8	I/O108	I/O109	I/O110	I/O111													I/O112	I/O113	I/O114	I/O115	8
9	GND	I/O102	I/O103	I/O104													I/O105	I/O106	I/O107	GND	9
10	GND	I/O96	I/O97	I/O98													I/O99	I/O100	I/O101	GND	10
11	GND	I/O90	I/O91	I/O92													I/O93	I/O94	I/O95	GND	11
12	GND	I/O84	I/O85	I/O86													I/O87	I/O88	I/O89	GND	12
13	I/O76	I/O77	I/O78	I/O79													I/O80	I/O81	I/O82	I/O83	13
14	I/O70	I/O71	I/O72	V_{CC}													V_{CC}	I/O73	I/O74	I/O75	14
15	GND	I/O64	I/O65	I/O66													I/O67	I/O68	I/O69	GND	15
16	I/O58	I/O59	I/O60	V_{CC}													V_{CC}	I/O61	I/O62	I/O63	16
17	I/O44	I/O45	I/O46	V_{CC}	TDI	I/O47	V_{CC}	I/O48	I/O49	I/O50	I/O51	I/O52	I/O53	V_{CC}	I/O54	TCK	V_{CC}	I/O55	I/O56	I/O57	17
18	GND	I/O28	V_{CC}	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	V_{CC}	I/O43	GND	18
19	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	IO/CLK0	I1/CLK1	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	GND	19
20	GND	GND	I/O0	I/O1	I/O2	GND	I/O3	GND	I/O4	GND	I/O5	I/O6	GND	I/O7	GND	I/O8	I/O9	I/O10	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

20446G-026

Select devices have been discontinued.
See Ordering Information section for product status.

256-BALL BGA CONNECTION DIAGRAM — M5-320

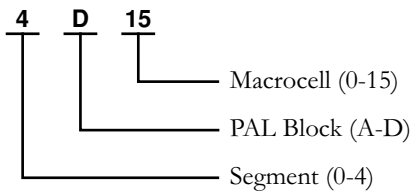
Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2D10	2D13	2D15	GND	GND	1
2	GND	3B2	3A3	3A8	3A13	3D13	3D9	3D8	3D4	I3/CLK3	I2/CLK2	2D3	2D4	2D8	2D12	2A15	2A13	2A12	2A9	2A7	2
3	GND	3B8	V_{CC}	3A2	3A4	3A12	3D14	3D10	3D5	3D0	2D0	2D5	2D9	2D14	2A14	2A10	2A8	V_{CC}	2A3	GND	3
4	3B13	3B11	3B3	V_{CC}	TDO	3A7	V_{CC}	3D11	3D6	3D1	2D1	2D6	2D11	V_{CC}	2A11	TMS	V_{CC}	2A6	2A2	2A0	4
5	4B14	4B15	3B4	V_{CC}													V_{CC}	2A5	2B0	2B1	5
6	GND	4B11	3B12	3B7													2A4	2A1	2B4	GND	6
7	4B8	4B10	4B13	V_{CC}													V_{CC}	2B2	2B5	2B7	7
8	4B4	4B6	4B9	4B12													2B3	2B6	2B9	2B11	8
9	GND	4B3	4B5	4B7													2B8	2B10	2B12	GND	9
10	GND	4B0	4B1	4B2													2B13	2B14	2B15	GND	10
11	GND	4A0	4A1	4A2													1B13	1B14	1B15	GND	11
12	GND	4A3	4A5	4A7													1B8	1B10	1B12	GND	12
13	4A4	4A6	4A9	4A12													1B3	1B6	1B9	1B11	13
14	4A8	4A10	4A13	V_{CC}													V_{CC}	1B2	1B5	1B7	14
15	GND	4A11	0B12	0B7													1A4	1A1	1B4	GND	15
16	4A14	4A15	0B4	V_{CC}													V_{CC}	1A5	1B0	1B1	16
17	0B13	0B11	0B3	V_{CC}	TDI	0A7	V_{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V_{CC}	1A11	TCK	V_{CC}	1A6	1A2	1A0	17
18	GND	0B8	V_{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A14	1A10	1A8	V_{CC}	1A3	GND	18
19	0B2	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	I0/CLK0	I1/CLK1	1D4	1D8	1D9	1D13	1A15	1A12	1A9	1A7	GND	19
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A13	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



20446G-029

Select devices have been discontinued. See Ordering Information section for product status.

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (Macrocell Association)

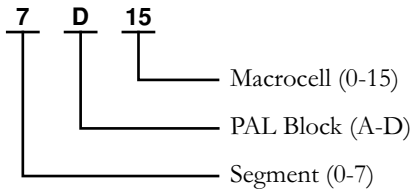
352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	I3/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	NC	1
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	GND	2
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I2/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	3
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V_{CC}	5A11	V_{CC}	5D12	5D7	5D2	V_{CC}	4D3	4D8	4D12	V_{CC}	4A11	V_{CC}	4A4	4A0	V_{CC}	3A15	3A13	3A12	4
5	GND	6A12	6A13	V_{CC}																			3A14	3A11	3A9	GND	5
6	NC	6A9	6A10	6A15																			3A10	3A8	3A7	3A5	6
7	GND	6A6	6A8	6A11																			3A6	3A4	3A3	3A0	7
8	6A1	6A4	6A5	6A7																			3A2	3A1	3B0	NC	8
9	6B1	6A0	6A2	6A3																			V_{CC}	3B1	3B2	GND	9
10	GND	6B2	6B0	V_{CC}																			3B3	3B4	3B5	3B6	10
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	3B10	11
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B14	12
13	6B14	6B13	6B12	6B11																			V_{CC}	2B15	3B15	GND	13
14	GND	7B15	6B15	V_{CC}																			2B11	2B12	2B13	2B14	14
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10	15
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6	16
17	7B7	7B6	7B5	7B4																			V_{CC}	2B0	2B2	GND	17
18	GND	7B3	7B2	V_{CC}																			2A3	2A2	2A0	2B1	18
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1	19
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND	20
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC	21
22	GND	7A9	7A11	7A15																			V_{CC}	2A13	2A12	GND	22
23	7A10	7A13	7A14	V_{CC}	0A0	0A4	V_{CC}	0A11	V_{CC}	0D12	0D8	0D3	V_{CC}	1D2	1D7	1D12	V_{CC}	1A11	V_{CC}	1A6	1A3	1A0	TCK	NC	2A14	NC	23
24	NC	NC	TDI	0A2	0A5	0A7	0A10	0A14	0D14	0D11	0D7	0D4	I0/CLK0	1D1	1D5	1D9	1D14	1A13	1A10	1A8	1A7	1A4	1A1	NC	GND	GND	24
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D13	0D10	0D6	0D2	0D0	1D0	1D4	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	25
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	I1/CLK1	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	26
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

20446G-031

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



Select devices have been discontinued.
See Ordering Information section for product status.

5V M5 ORDERING INFORMATION[1,2]

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

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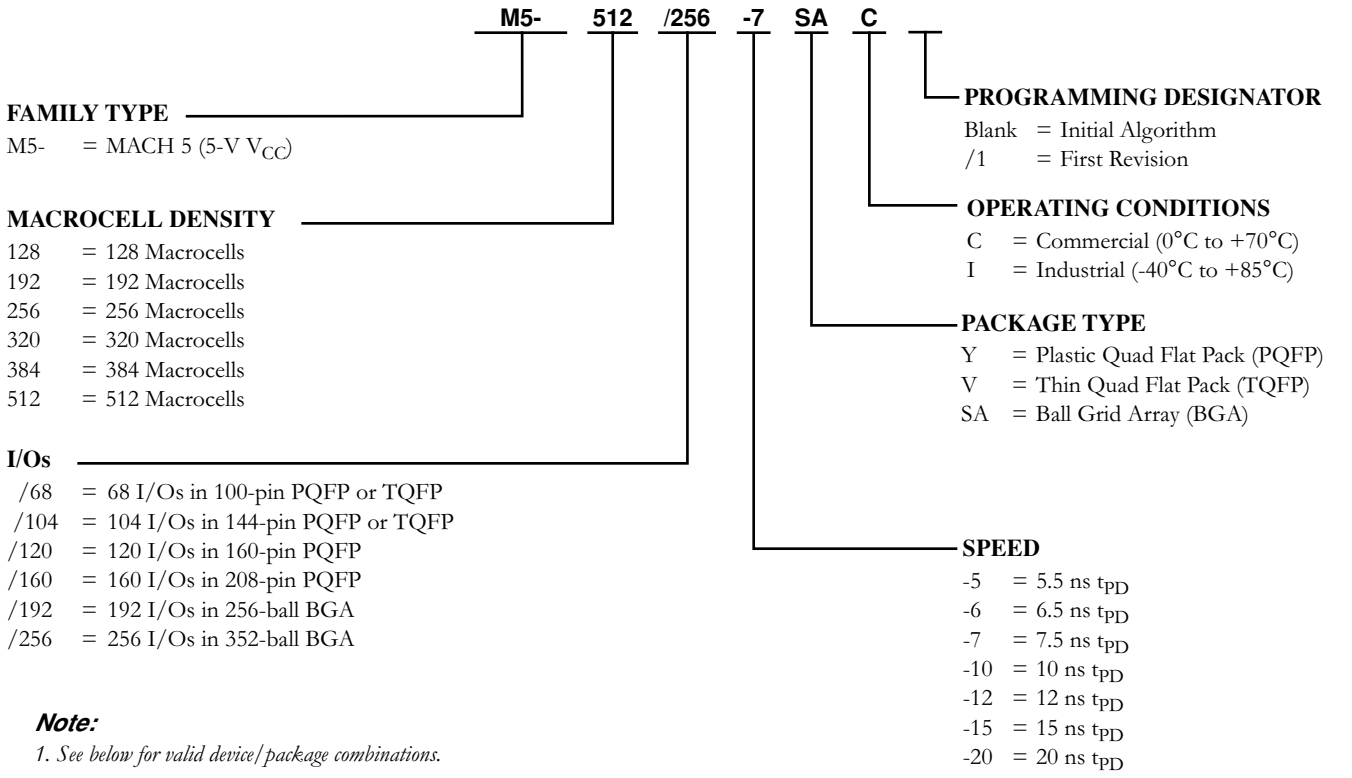


Note:

1. See below for valid device/package combinations.

2. M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC[1], YI[1]
M5-128/120		YC, YI
M5-192/68		VC, VI
M5-192/120		YC, YI
M5-256/68		VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial: -6, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, YI
M5-320/192		SAC, SAI
M5-384/160		YC, YI
M5-512/160		YC, YI
M5-512/256		SAC, SAI

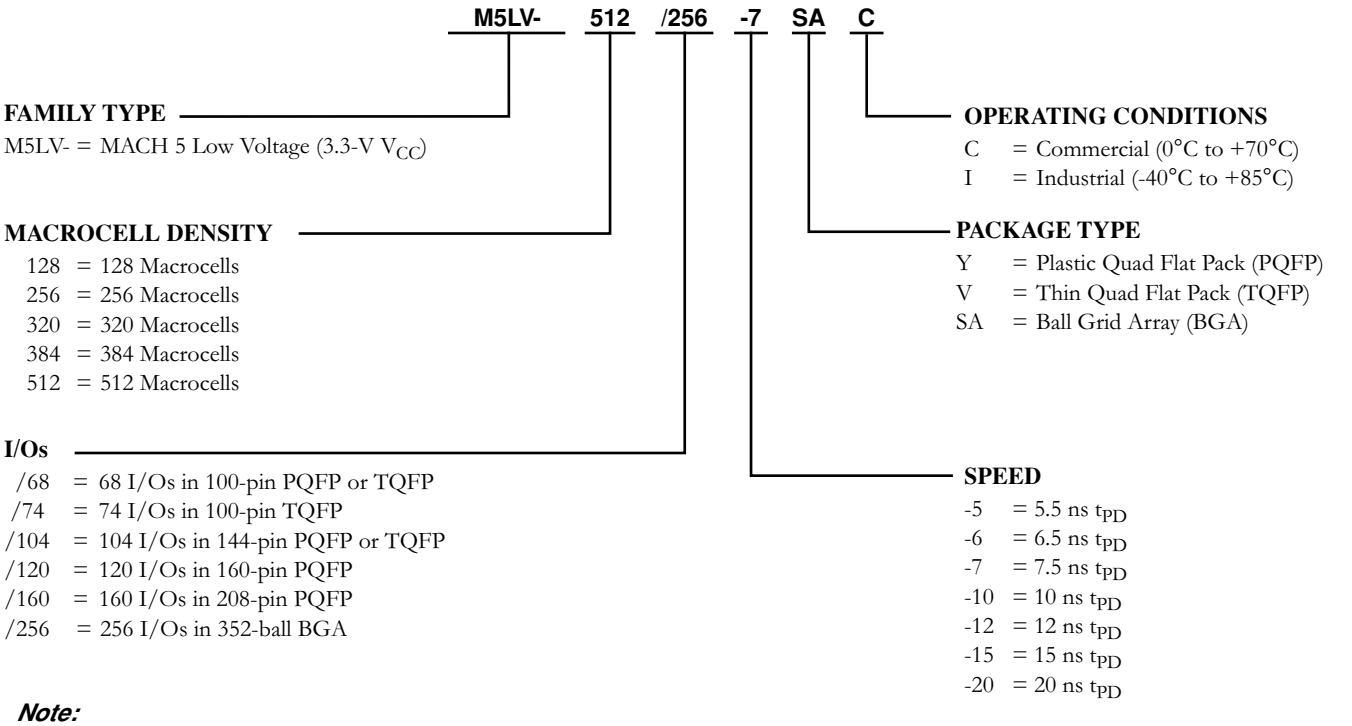
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued. See Ordering Information section for product status.

3.3V M5LV ORDERING INFORMATION[1]

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12 Industrial: -7, -10, -12, -15	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68		YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15 Industrial: -10, -12, -15, -20	YC, YI
M5LV-320/160		YC, YI
M5LV-384/120		YC, YI
M5LV-384/160		YC, YI
M5LV-512/120		YC, YI
M5LV-512/160		YC, YI
M5LV-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued. See Ordering Information section for product status.