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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	104
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-128-104-7vc

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



Figure 1. MACH 5 Block Diagram

20446G-001

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Select devices have been discontinued.
See Ordering Information section for product status.



20446G-002

Figure 2. PAL Block Structure

Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 or 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 4. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂ , C ₃ , C ₄	M ₈	C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₁	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅	M ₉	C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₂	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆	M ₁₀	C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₃	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₁	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₄	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₂	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₅	C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈	M ₁₃	C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉	M ₁₄	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀	M ₁₅	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅

Select devices have been discontinued.
See Ordering Information section for product status.

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ($A*B*C$)
- ◆ Sum-term clock ($A+B+C$)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.
See Ordering Information section for product status.

**Select devices have been discontinued.
See Ordering Information section for product status.**



MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.
See Ordering Information section for product status.

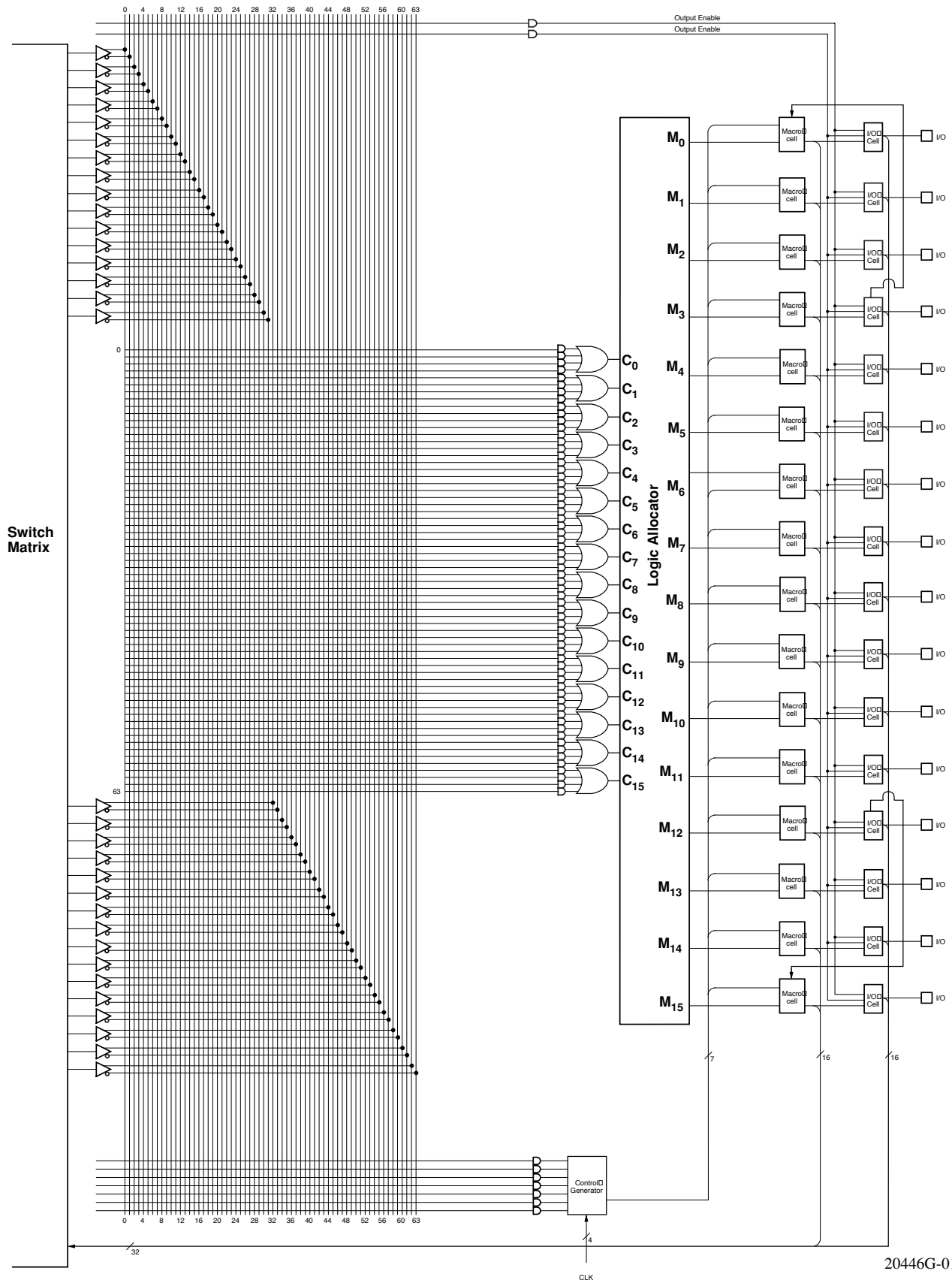


SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

**Select devices have been discontinued.
See Ordering Information section for product status.**

MACH 5 PAL BLOCK

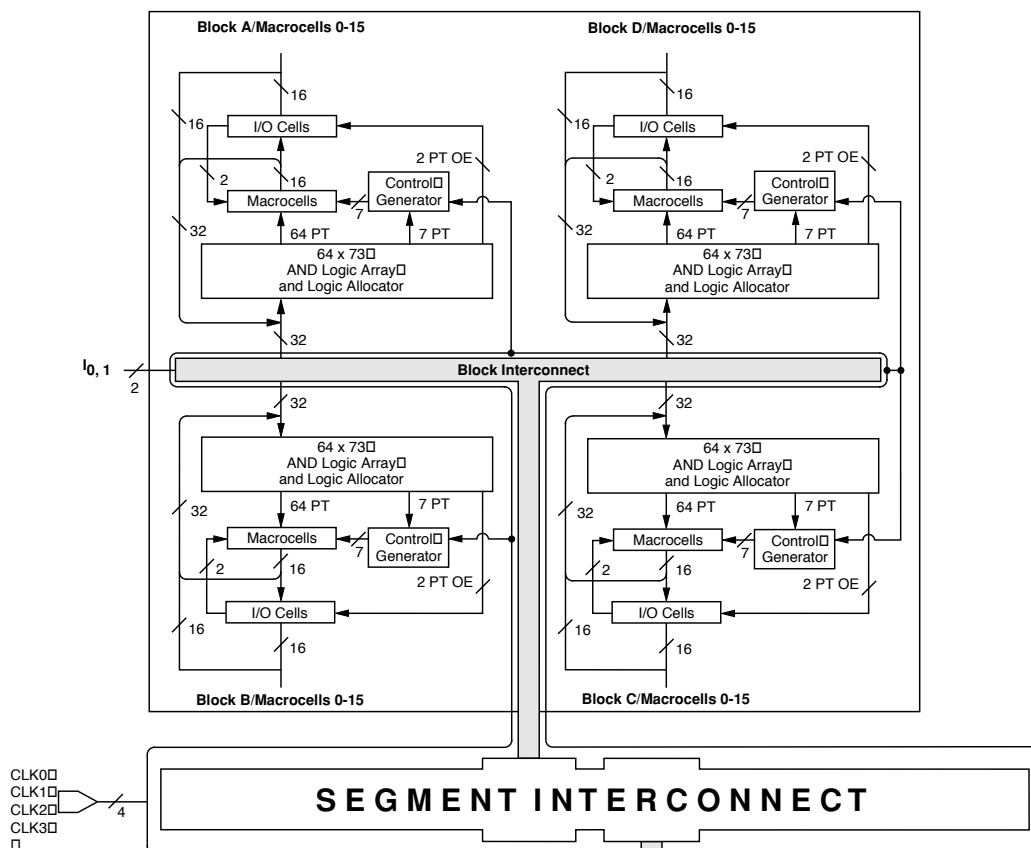


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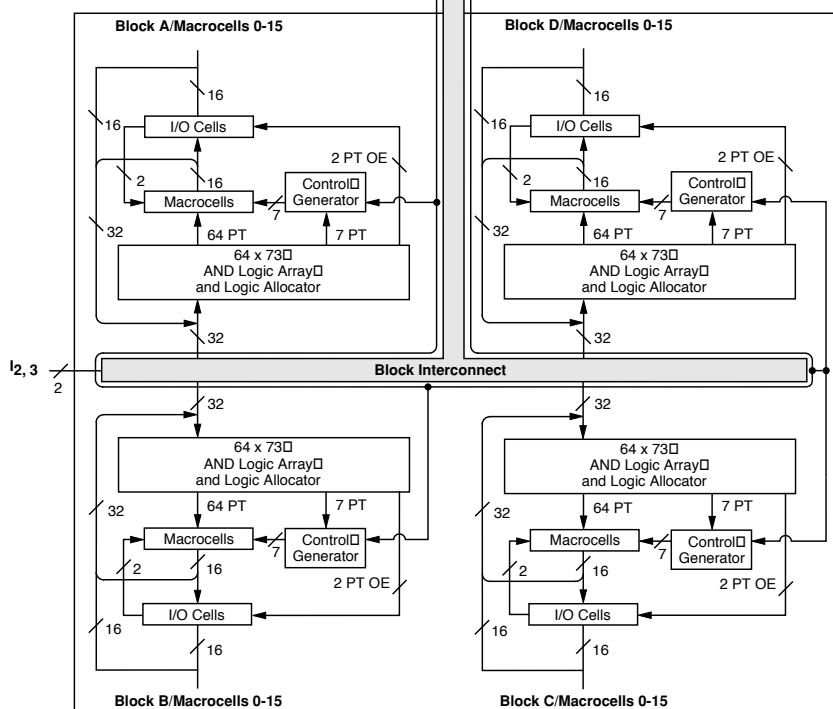
20446G-015

BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0



SEGMENT 1

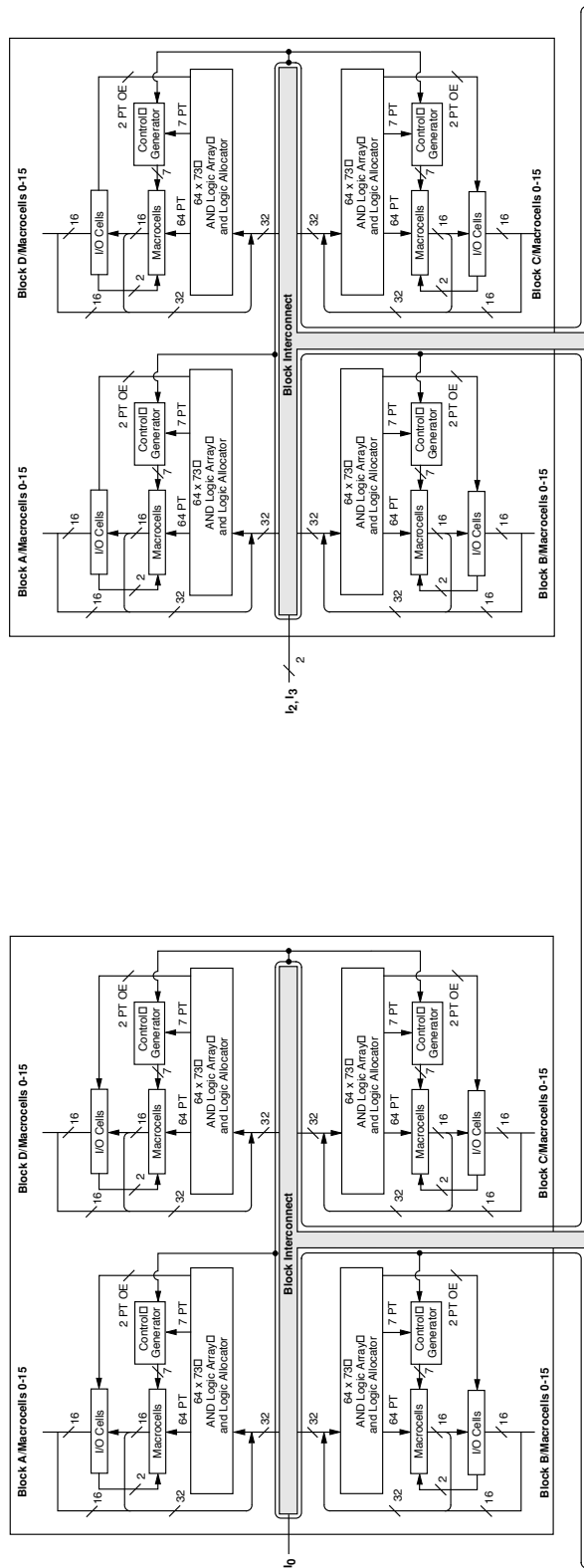


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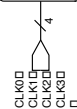
20446G-007

BLOCK DIAGRAM — M5-192/XXX

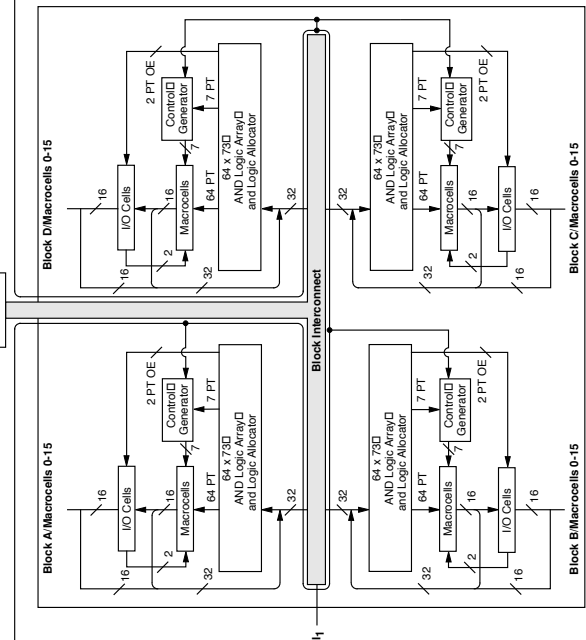
SEGMENT 2



SEGMENT INTERCONNECT



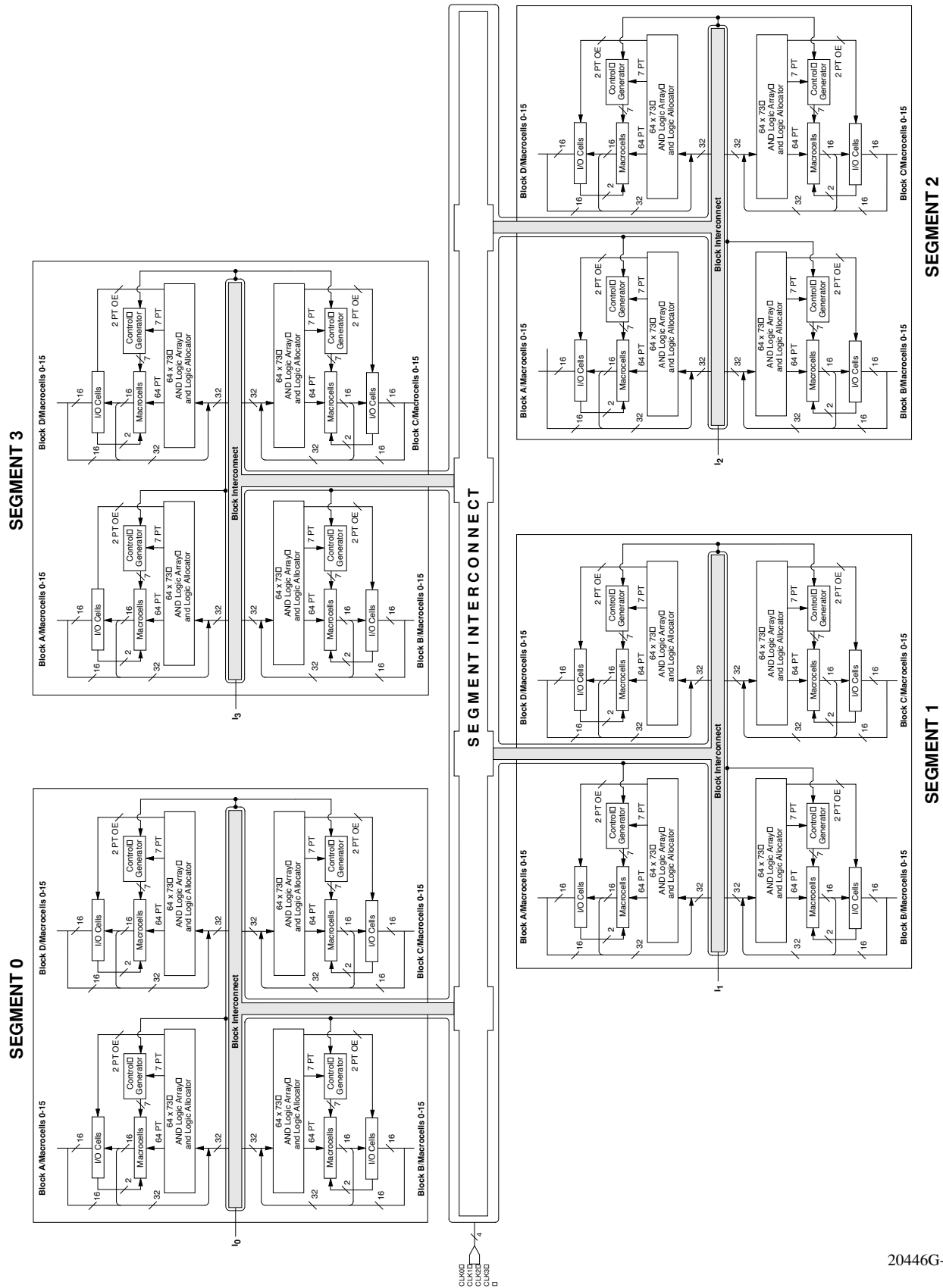
SEGMENT 1



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-008

BLOCK DIAGRAM — M5(LV)-256/XXX

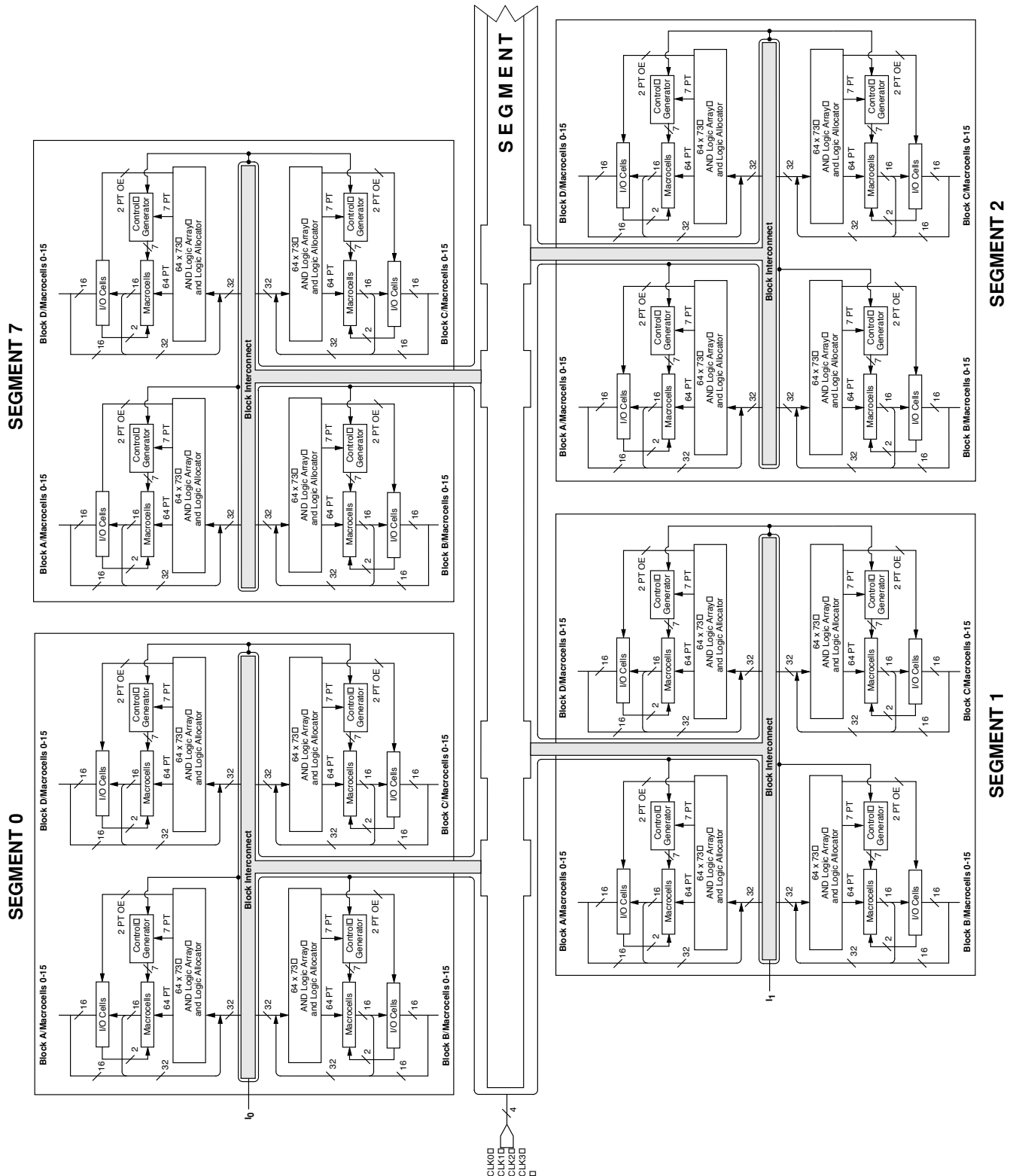


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20446G-009

BLOCK DIAGRAM — M5(LV)-512/XXX

Continued



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-012

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																
t _{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0		18.0	ns
t _{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:																
t _{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		10.0		ns
t _{SA}	Asynchronous clock setup time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{COSi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0		10.0	ns
t _{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0		12.0	ns
t _{COAi}	Asynchronous clock to internal output		6.0		6.0		8.0		10.0		13.0		15.0		18.0	ns
t _{COA}	Asynchronous clock to output		8.0		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:																
t _{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0		10.0	ns
t _{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0		12.0	ns
t _{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0		12.0	ns
t _{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:																
t _{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		4.0		ns
t _{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:																
t _{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
t _{PDILi}	Transparent input latch		5.0		5.0		5.5		6.0		6.0		6.0		6.0	ns
Output Delays:																
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns
t _{ER}	Output disable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns

Select devices have been discontinued.
See Ordering Information section for product status.

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	$V_{IN} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	$V_{OUT} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

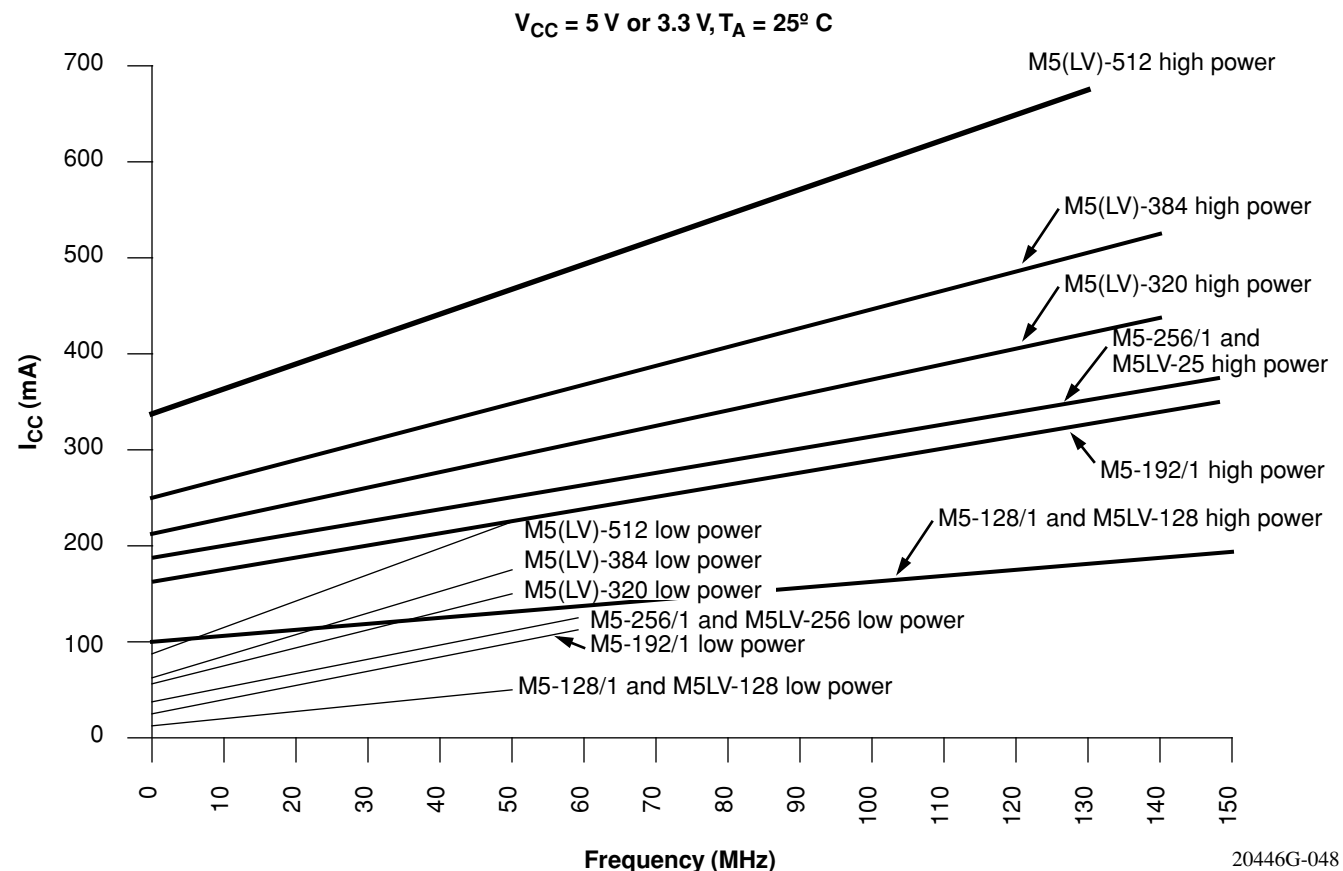


Figure 8. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

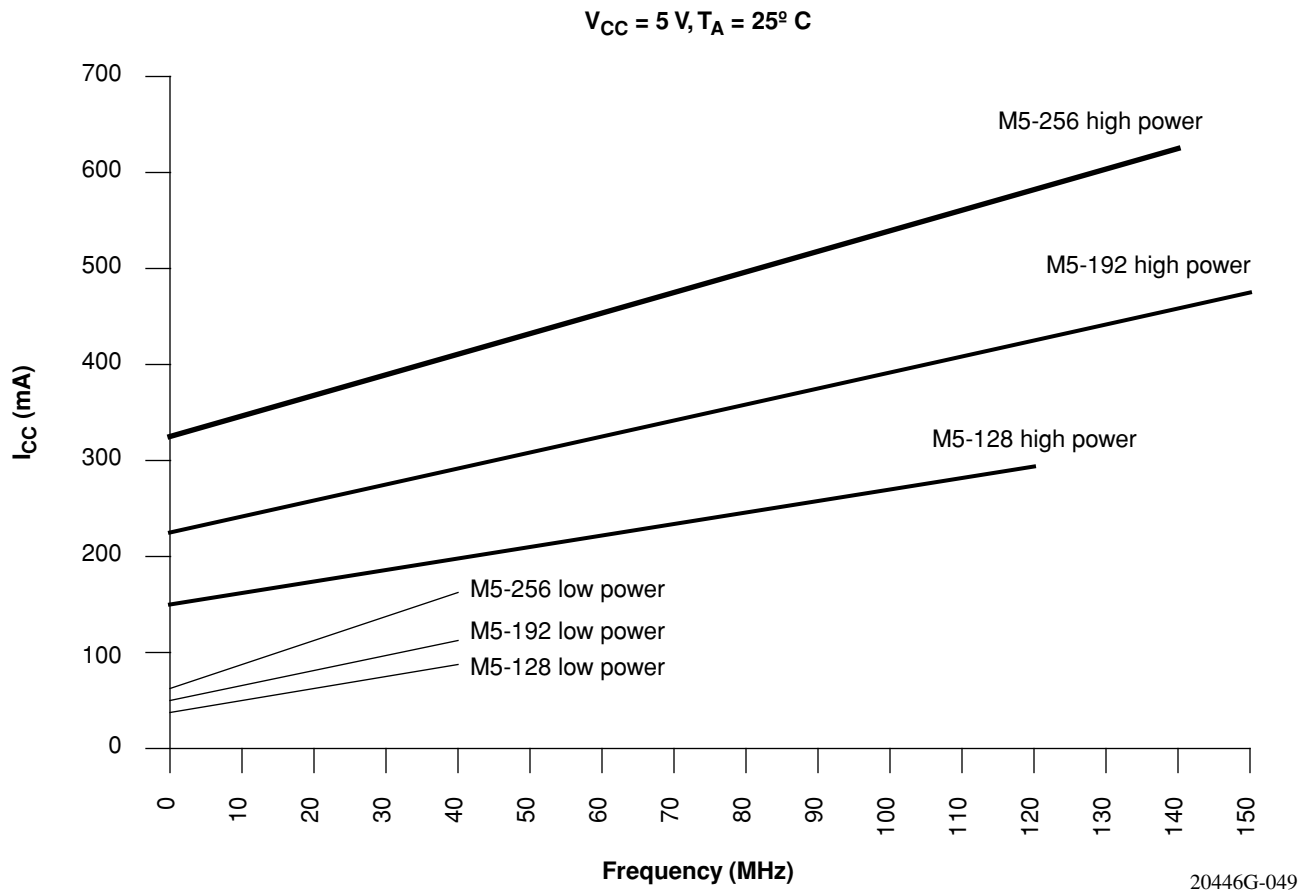


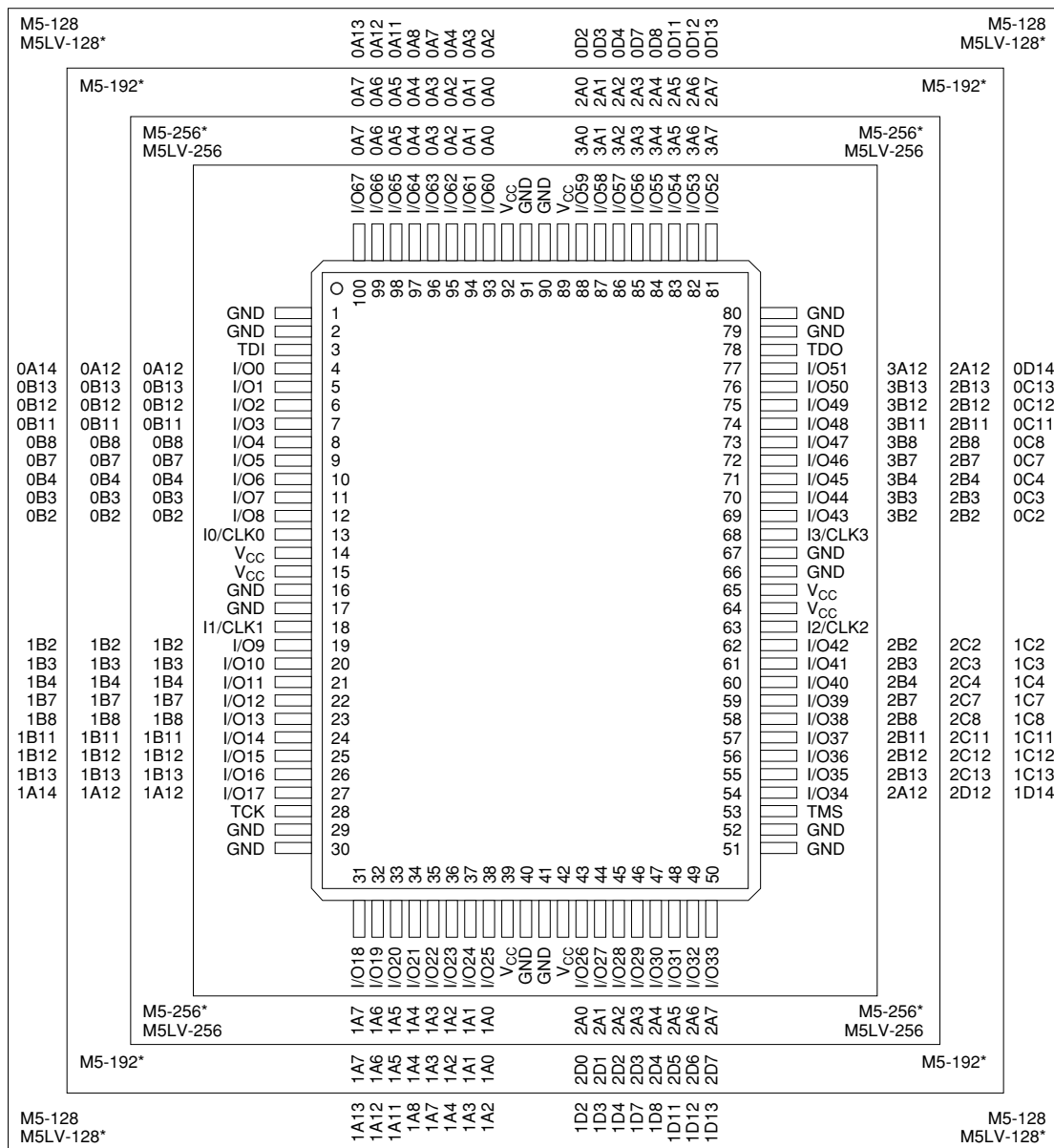
Figure 9. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued.
See Ordering Information section for product status.

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)



*Package obsolete, contact factory.

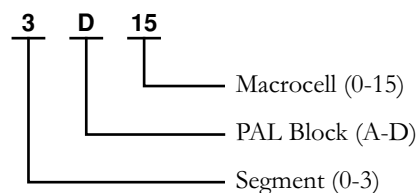
20446G-016

Select devices have been discontinued.
See Ordering Information section for product status.

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

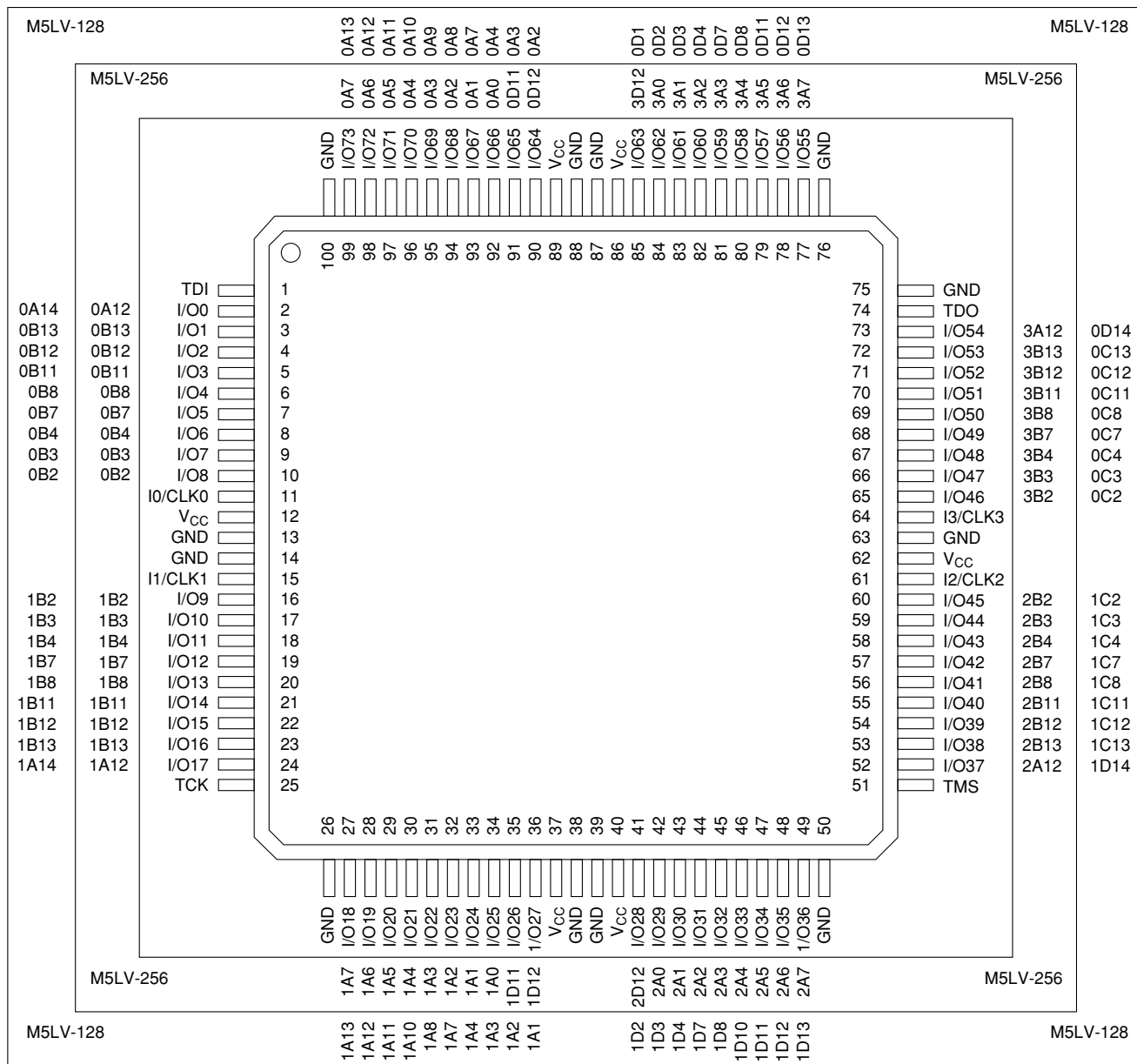
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (256 Macrocells)

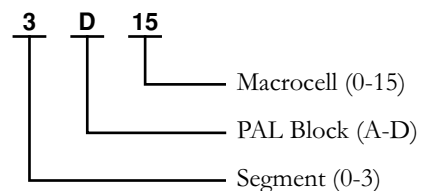


Select devices have been discontinued.
See Ordering Information section for product status.

20446G-023

Pin Designations

CLK = Clock	VCC = Supply Voltage
GND = Ground	TDI = Test Data In
I = Input	TCK = Test Clock
I/O = Input/Output	TMS = Test Mode Select
NC = No Connect	TDO = Test Data Out



352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I/O233 I ₃ /CLK ₃	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O224	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	NC
3	GND	GND	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I/O211	I/O212	I/O213	I/O214	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	TMS	NC	NC	NC
4	NC	I/O188	NC	TDO	I/O189	I/O190	I/O191	V _{CC}	I/O192	V _{CC}	I/O193	I/O194	I/O195	V _{CC}	I/O196	I/O197	I/O198	V _{CC}	I/O199	V _{CC}	I/O200	I/O201	V _{CC}	I/O202	I/O203	I/O204
5	GND	I/O183	I/O184	V _{CC}																			I/O185	I/O186	I/O187	GND
6	NC	I/O176	I/O177	I/O178	I/O171																		I/O179	I/O180	I/O181	I/O182
7	GND	I/O169	I/O170	I/O171	I/O165																		I/O172	I/O173	I/O174	I/O175
8	I/O162	I/O163	I/O164	I/O165																			I/O166	I/O167	I/O168	NC
9	I/O156	I/O157	I/O158	I/O159																			V _{CC}	I/O160	I/O161	GND
10	GND	I/O150	I/O151	V _{CC}	I/O145																		I/O152	I/O153	I/O154	I/O155
11	I/O142	I/O143	I/O144	I/O145																			I/O146	I/O147	I/O148	I/O149
12	I/O134	I/O135	I/O136	I/O137																			I/O138	I/O139	I/O140	I/O141
13	I/O128	I/O129	I/O130	I/O131																			V _{CC}	I/O132	I/O133	GND
14	GND	I/O122	I/O123	V _{CC}																			I/O124	I/O125	I/O126	I/O127
15	I/O114	I/O115	I/O116	I/O117																			I/O118	I/O119	I/O120	I/O121
16	NC	I/O107	I/O108	I/O109																			I/O110	I/O111	I/O112	I/O113
17	I/O101	I/O102	I/O103	I/O104																			V _{CC}	I/O105	I/O106	GND
18	GND	I/O87	I/O88	V _{CC}																			I/O97	I/O98	I/O99	I/O100
19	I/O80	I/O81	I/O82	I/O83																			I/O91	I/O92	I/O93	I/O94
20	I/O73	I/O74	I/O75	I/O76																			I/O84	I/O85	I/O86	GND
21	GND	I/O68	I/O69	I/O70																			I/O77	I/O78	I/O79	NC
22																							V _{CC}	I/O71	I/O72	GND
23	I/O51	I/O52	I/O53	V _{CC}	I/O54	I/O55	V _{CC}	I/O56	V _{CC}	I/O57	I/O58	I/O59	V _{CC}	I/O60	I/O61	I/O62	V _{CC}	I/O63	V _{CC}	I/O64	I/O65	I/O66	TCK	NC	NC	NC
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	NC	NC	NC	NC
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	NC	NC	NC
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	NC	GND	NC	NC	NC

Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

20446G-030

Select devices have been discontinued.
See Ordering Information section for product status.

5V M5 ORDERING INFORMATION^{1,2}

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC ¹ , YI ¹
M5-128/120		YC, YI
M5-192/68		VC, VI
M5-192/120		YC, YI
M5-256/68		VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial: -6, -7, -10, -12, -15	YC, YI
M5-320/192		SAC, SAI
M5-384/160		YC, YI
M5-512/160	Industrial: -7, -10, -12, -15, -20	YC, YI
M5-512/256		SAC, SAI

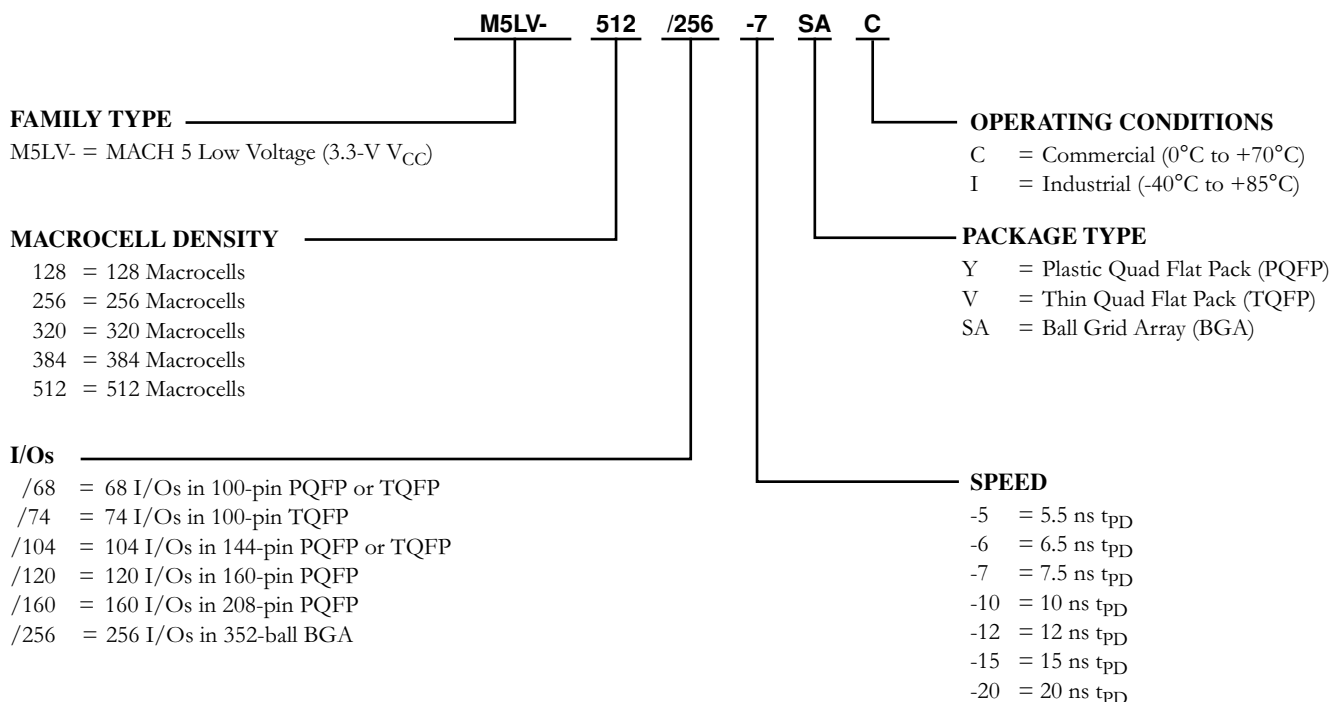
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.

3.3V M5LV ORDERING INFORMATION¹

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68	Industrial: -7, -10, -12, -15	YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15	YC, YI
M5LV-320/160		YC, YI
M5LV-384/120		YC, YI
M5LV-384/160		YC, YI
M5LV-512/120	Industrial: -10, -12, -15, -20	YC, YI
M5LV-512/160		YC, YI
M5LV-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.