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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

|                                 |                                                                                                                                                                       |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                              |
| Programmable Type               | In System Programmable                                                                                                                                                |
| Delay Time tpd(1) Max           | 7.5 ns                                                                                                                                                                |
| Voltage Supply - Internal       | 3V ~ 3.6V                                                                                                                                                             |
| Number of Logic Elements/Blocks | -                                                                                                                                                                     |
| Number of Macrocells            | 128                                                                                                                                                                   |
| Number of Gates                 | -                                                                                                                                                                     |
| Number of I/O                   | 104                                                                                                                                                                   |
| Operating Temperature           | -40°C ~ 85°C (TA)                                                                                                                                                     |
| Mounting Type                   | Surface Mount                                                                                                                                                         |
| Package / Case                  | 144-LQFP                                                                                                                                                              |
| Supplier Device Package         | 144-TQFP (20x20)                                                                                                                                                      |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-128-104-7vi">https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-128-104-7vi</a> |

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



Figure 1. MACH 5 Block Diagram

20446G-001

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Select devices have been discontinued.  
See Ordering Information section for product status.

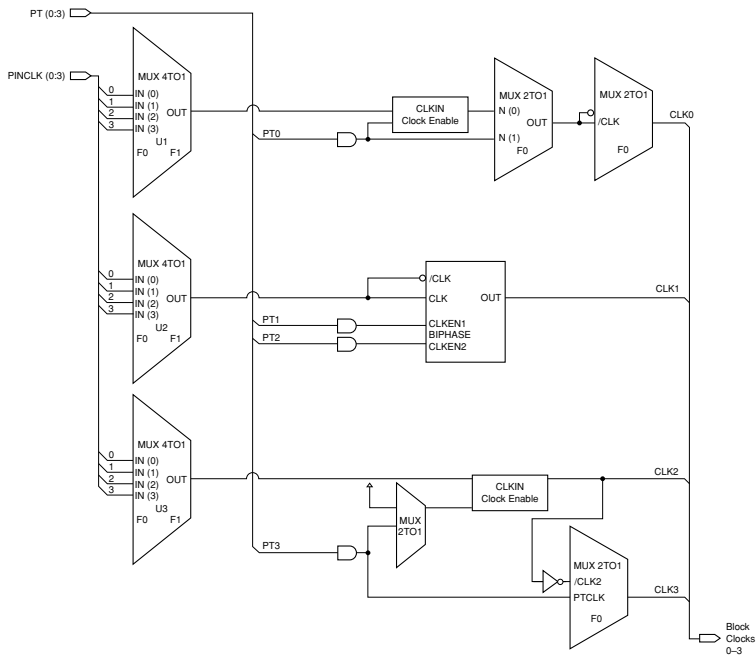
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

#### Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

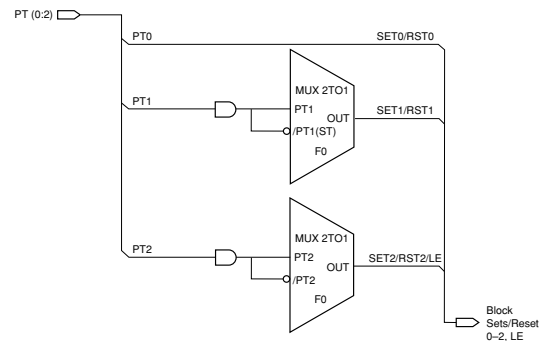
#### Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

**Figure 4. Clock Generator**



20446G-005

**Figure 5. Set/Reset Generator**

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.  
See Ordering Information section for product status.**

## OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

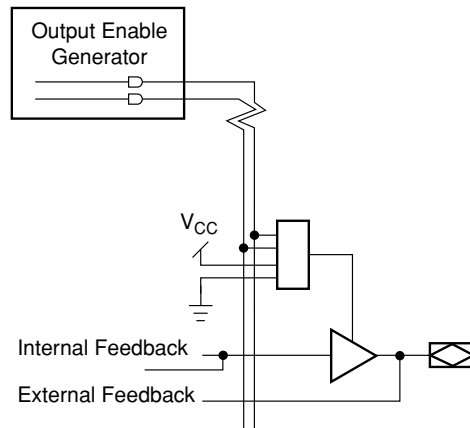


Figure 6. Output Enable Generator and I/O Cell

20446G-006

Select devices have been discontinued.  
See Ordering Information section for product status.



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## MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

## IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

## IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

## PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above  $V_{CC}$  because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.  
See Ordering Information section for product status.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS <sup>1</sup>

Both the 3.3-V and 5-V  $V_{CC}$  MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

### Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

## BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

|                                     |            |
|-------------------------------------|------------|
| High Speed/High Power               | 100% Power |
| Medium High Speed/Medium High Power | 67% Power  |
| Medium Low Speed/Medium Low Power   | 40% Power  |
| Low Speed/Low Power                 | 20% Power  |

## PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

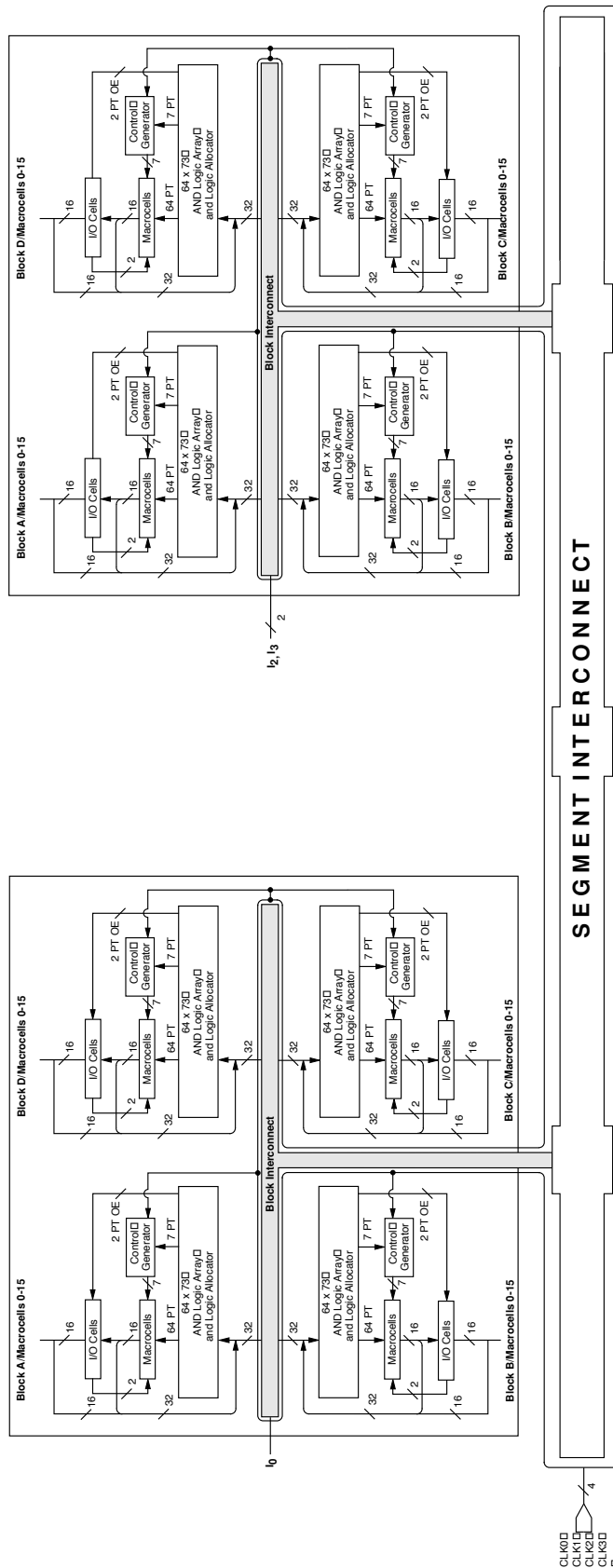
## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

Select devices have been discontinued.  
See Ordering Information section for product status.

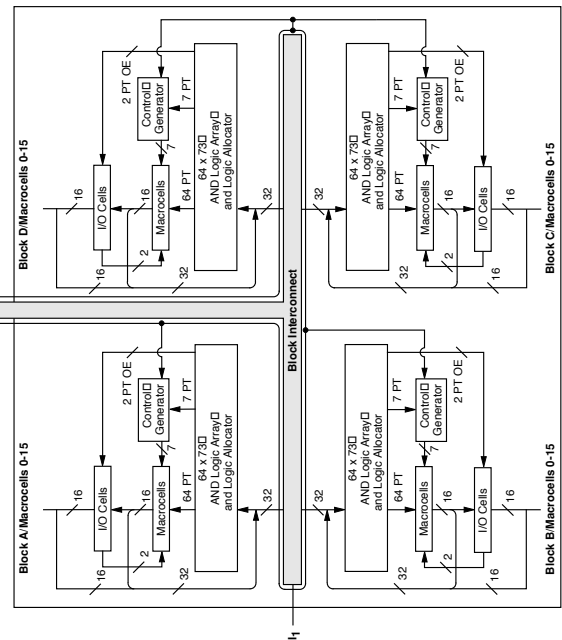
## BLOCK DIAGRAM — M5-192/XXX

### SEGMENT 2



### SEGMENT INTERCONNECT

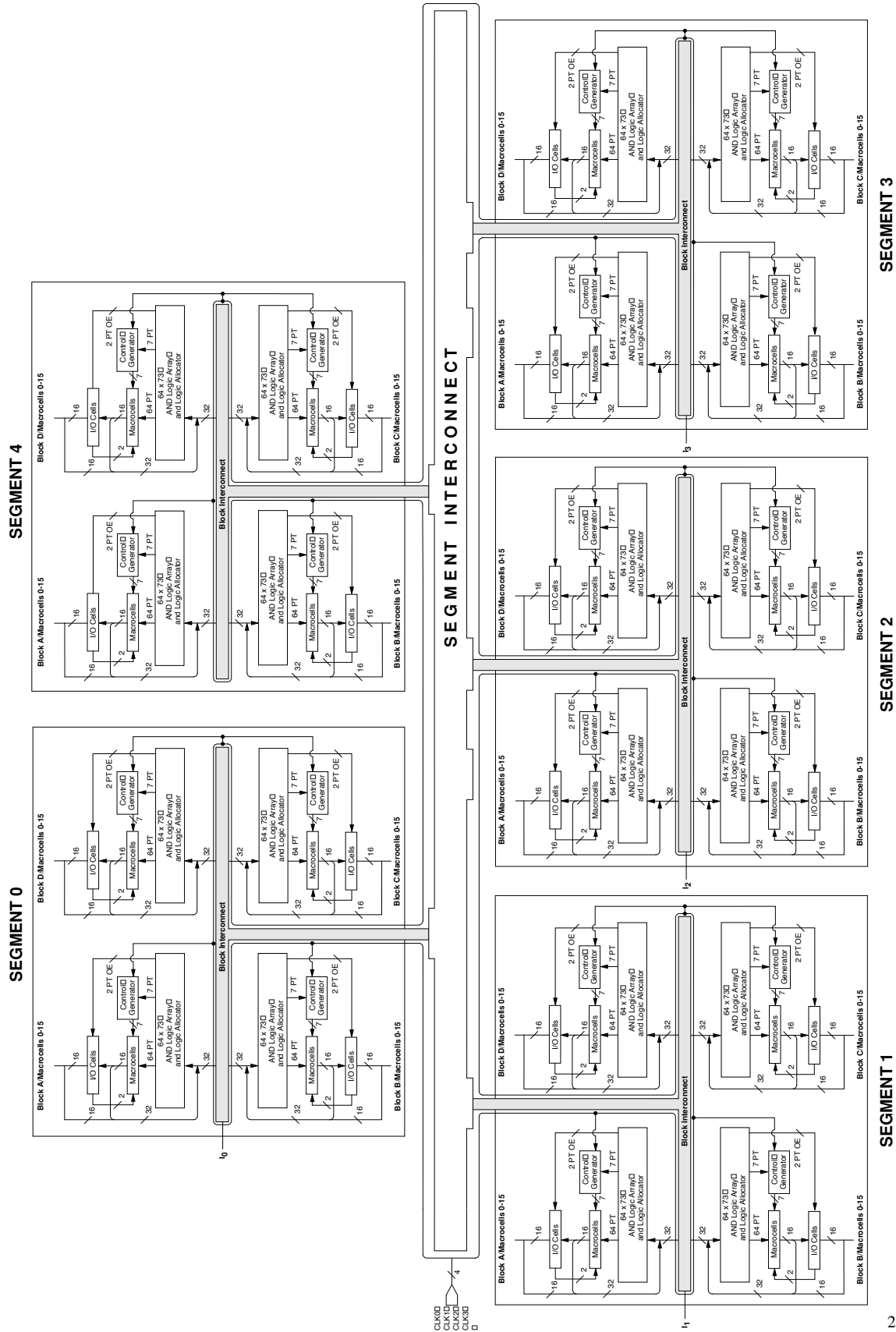
### SEGMENT 1



Select devices have been discontinued.  
See Ordering Information section for product status.

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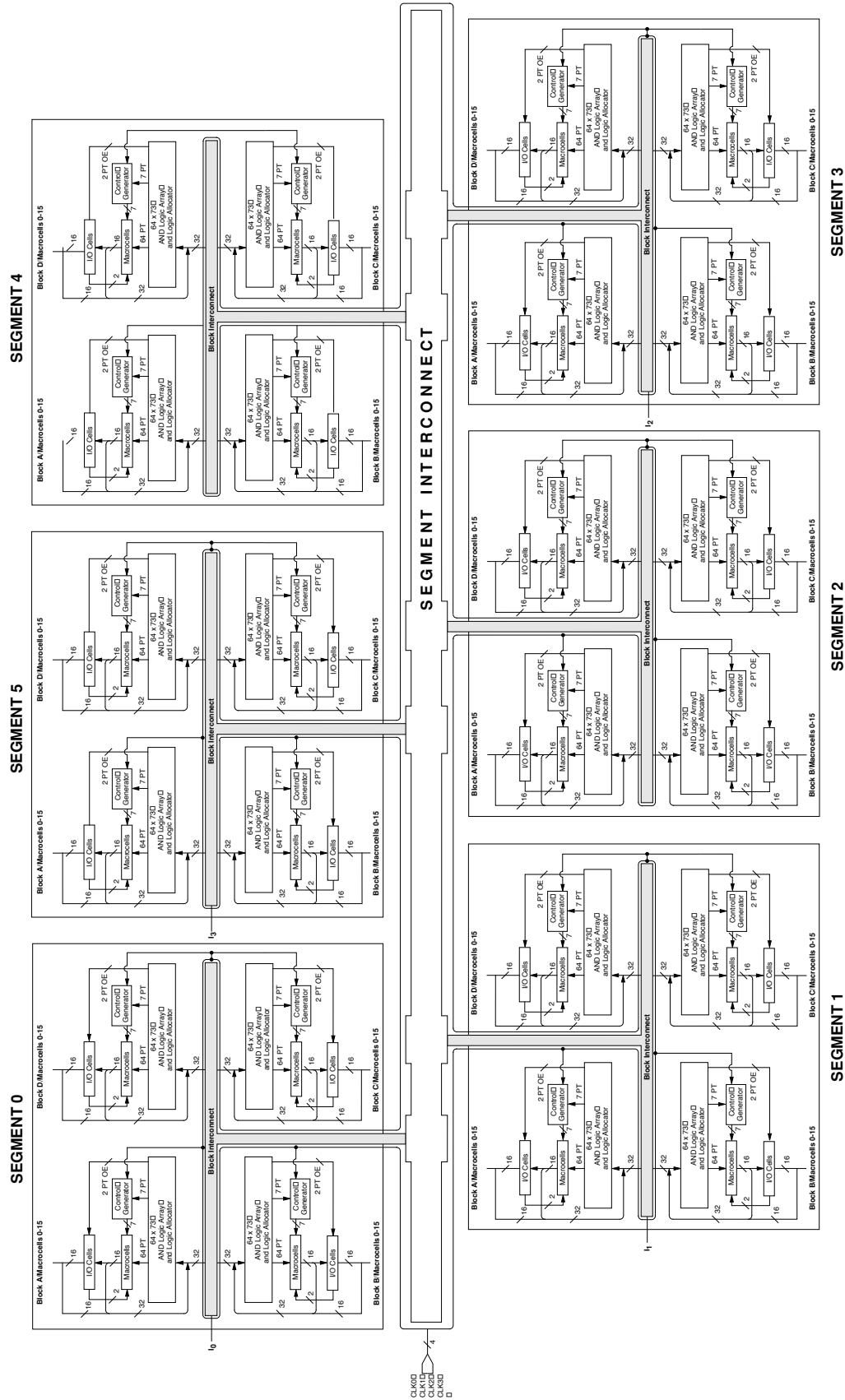
# BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-010

# BLOCK DIAGRAM — M5(LV)-384/XXX

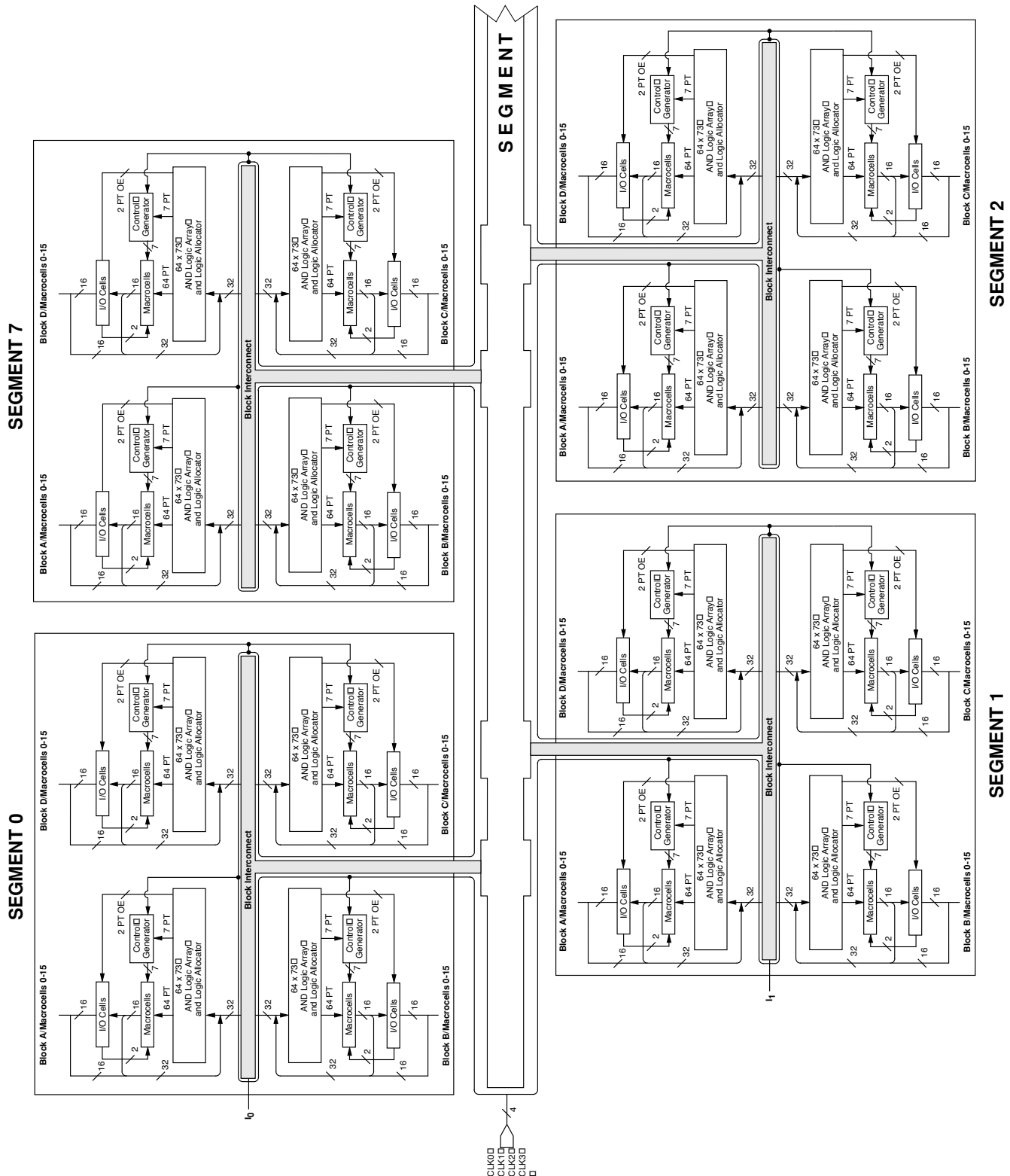


Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-011

# BLOCK DIAGRAM — M5(LV)-512/XXX

Continued



Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-012

## ABSOLUTE MAXIMUM RATINGS

### M5

Storage Temperature. . . . . -65°C to +150°C  
 Device Junction  
 Temperature (Note 1) . . . . . +130°C or +150°C  
 Supply Voltage  
 with Respect to Ground . . . . . -0.5 V to +7.0 V  
 DC Input Voltage . . . . . -0.5 V to 5.5 V  
 Static Discharge Voltage . . . . . 2000 V  
 Latchup Current (-40°C to +85°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . 0°C to +70°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . . -40°C to +85°C  
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

Select devices have been discontinued.  
See Ordering Information section for product status.

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                                                                     | Test Description                                                                              | Min | Typ | Max  | Unit          |
|------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage<br>(For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices) | $I_{OH} = -3.2 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$     | 2.4 |     |      | V             |
|                  |                                                                                           | $I_{OH} = -100 \mu\text{A}$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$    |     | 3.3 | 3.6  | V             |
|                  | Output HIGH Voltage<br>(For M5-128, M5-192, M5-256 Devices)                               | $I_{OH} = -3.2 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$     | 2.4 |     |      | V             |
|                  |                                                                                           | $I_{OH} = -2.5 \text{ mA}$ , $V_{CC} = 5.25 \text{ V}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ |     |     | 3.6  | V             |
| $V_{OL}$         | Output LOW Voltage (Note 2)                                                               | $I_{OL} = +16 \text{ mA}$ , $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$      |     |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                                                                        | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)                                 | 2.0 |     |      | V             |
| $V_{IL}$         | Input LOW Voltage                                                                         | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)                                  |     |     | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current                                                                | $V_{IN} = 5.25$ , $V_{CC} = \text{Max}$ (Note 4)                                              |     |     | 10   | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current                                                                 | $V_{IN} = 0$ , $V_{CC} = \text{Max}$ (Note 4)                                                 |     |     | -10  | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH                                                     | $V_{OUT} = 5.25$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)      |     |     | 10   | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW                                                      | $V_{OUT} = 0$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)         |     |     | -10  | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current                                                              | $V_{OUT} = 0.5 V_{CC} = \text{Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 5)           | -30 |     | -180 | mA            |

### Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.
- Total  $I_{OL}$  between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

## ABSOLUTE MAXIMUM RATINGS

### M5LV

Storage Temperature. . . . . -65°C to +150°C  
Device Junction Temperature. . . . . +130°C  
Supply Voltage  
with Respect to Ground . . . . . -0.5 V to +4.5 V  
DC Input Voltage . . . . . -0.5 V to 5.5 V  
Static Discharge Voltage . . . . . 2000 V  
Latchup Current (-40°C to +85°C) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
Operating in Free Air. . . . . 0°C to +70°C  
Supply Voltage ( $V_{CC}$ )  
with Respect to Ground. . . . . +3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
Operating in Free Air. . . . . -40°C to +85°C  
Supply Voltage ( $V_{CC}$ )  
with Respect to Ground. . . . . +3.0 V to +3.6 V  
*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Description                                                                          |                                   | Min            | Max  | Unit    |
|------------------|---------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------|----------------|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $V_{CC} = \text{Min}$                                                                     | $I_{OH} = -100 \mu A$             | $V_{CC} - 0.2$ |      | V       |
|                  |                                       | $V_{IN} = V_{IH} \text{ or } V_{IL}$                                                      | $I_{OH} = 3.2 \text{ mA}$         | 2.4            |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $V_{CC} = \text{Min}$                                                                     | $I_{OL} = 100 \mu A$              |                | 0.2  | V       |
|                  |                                       | $V_{IN} = V_{IH} \text{ or } V_{IL}$                                                      | $I_{OL} = 16 \text{ mA (Note 1)}$ |                | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | $V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$            |                                   | 2.0            | 5.5  | V       |
| $V_{IL}$         | Input LOW Voltage                     | $V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$            |                                   | -0.3           | 0.8  | V       |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$                                              |                                   |                | 10   | $\mu A$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$                                                |                                   |                | -10  | $\mu A$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$ |                                   |                | 10   | $\mu A$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$   |                                   |                | -10  | $\mu A$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$  |                                   | -15            | -160 | mA      |

#### Notes:

1. Total  $I_{OL}$  between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

Select devices have been discontinued.  
See Ordering Information section for product status.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                        |                                                       | -5  |     | -6  |      | -7  |      | -10 |      | -12 |      | -15 |      | -20  |      | Unit |
|------------------------|-------------------------------------------------------|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|------|------|------|
|                        |                                                       | Min | Max | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min  | Max  |      |
| Combinatorial Delay:   |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>PDi</sub>       | Internal combinatorial propagation delay              |     | 3.5 |     | 4.5  |     | 5.5  |     | 8.0  |     | 10.0 |     | 13.0 |      | 18.0 | ns   |
| t <sub>PD</sub>        | Combinatorial propagation delay                       |     | 5.5 |     | 6.5  |     | 7.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |
| Registered Delays:     |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SS</sub>        | Synchronous clock setup time                          | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 8.0 |      | 10.0 |      | ns   |
| t <sub>SA</sub>        | Asynchronous clock setup time                         | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>HS</sub>        | Synchronous clock hold time                           | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HA</sub>        | Asynchronous clock hold time                          | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>COSi</sub>      | Synchronous clock to internal output                  |     | 2.5 |     | 3.0  |     | 4.0  |     | 5.0  |     | 6.0  |     | 8.0  |      | 10.0 | ns   |
| t <sub>COS</sub>       | Synchronous clock to output                           |     | 4.5 |     | 5.0  |     | 6.0  |     | 7.0  |     | 8.0  |     | 10.0 |      | 12.0 | ns   |
| t <sub>COAi</sub>      | Asynchronous clock to internal output                 |     | 6.0 |     | 6.0  |     | 8.0  |     | 10.0 |     | 13.0 |     | 15.0 |      | 18.0 | ns   |
| t <sub>COA</sub>       | Asynchronous clock to output                          |     | 8.0 |     | 8.0  |     | 10.0 |     | 12.0 |     | 15.0 |     | 17.0 |      | 20.0 | ns   |
| Latched Delays:        |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SAL</sub>       | Latch setup time                                      | 3.0 |     | 4.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>HAL</sub>       | Latch hold time                                       | 3.0 |     | 3.0 |      | 4.0 |      | 5.0 |      | 6.0 |      | 7.0 |      | 8.0  |      | ns   |
| t <sub>PDLi</sub>      | Transparent latch internal                            |     | 6.0 |     | 7.0  |     | 7.0  |     | 8.0  |     | 9.0  |     | 10.0 |      | 10.0 | ns   |
| t <sub>PDL</sub>       | Propagation delay through transparent latch           |     | 8.0 |     | 9.0  |     | 9.0  |     | 10.0 |     | 11.0 |     | 12.0 |      | 12.0 | ns   |
| t <sub>GOAi</sub>      | Gate to internal output                               |     | 7.0 |     | 8.0  |     | 8.0  |     | 9.0  |     | 10.0 |     | 11.0 |      | 12.0 | ns   |
| t <sub>GOA</sub>       | Gate to output                                        |     | 9.0 |     | 10.0 |     | 10.0 |     | 11.0 |     | 12.0 |     | 13.0 |      | 14.0 | ns   |
| Input Register Delays: |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SIRS</sub>      | Input register setup time using a synchronous clock   | 2.0 |     | 2.0 |      | 2.0 |      | 3.0 |      | 3.0 |      | 3.0 |      | 3.0  |      | ns   |
| t <sub>SIRA</sub>      | Input register setup time using an asynchronous clock | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HIRS</sub>      | Input register hold time using a synchronous clock    | 3.0 |     | 3.0 |      | 3.0 |      | 4.0 |      | 4.0 |      | 4.0 |      | 4.0  |      | ns   |
| t <sub>HIRA</sub>      | Input register hold time using an asynchronous clock  | 6.0 |     | 6.0 |      | 6.0 |      | 7.0 |      | 7.0 |      | 7.0 |      | 7.0  |      | ns   |
| Input Latch Delays:    |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>SIL</sub>       | Input latch setup time                                | 2.0 |     | 2.0 |      | 2.0 |      | 3.0 |      | 3.0 |      | 3.0 |      | 3.0  |      | ns   |
| t <sub>HIL</sub>       | Input latch hold time                                 | 6.0 |     | 6.0 |      | 6.0 |      | 7.0 |      | 7.0 |      | 7.0 |      | 7.0  |      | ns   |
| t <sub>PDILi</sub>     | Transparent input latch                               |     | 5.0 |     | 5.0  |     | 5.5  |     | 6.0  |     | 6.0  |     | 6.0  |      | 6.0  | ns   |
| Output Delays:         |                                                       |     |     |     |      |     |      |     |      |     |      |     |      |      |      |      |
| t <sub>BUF</sub>       | Output buffer delay                                   |     | 2.0 |     | 2.0  |     | 2.0  |     | 2.0  |     | 2.0  |     | 2.0  |      | 2.0  | ns   |
| t <sub>SLW</sub>       | Slow slew rate delay                                  |     | 2.5 |     | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |     | 2.5  |      | 2.5  | ns   |
| t <sub>EA</sub>        | Output enable time                                    |     | 7.5 |     | 7.5  |     | 9.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |
| t <sub>ER</sub>        | Output disable time                                   |     | 7.5 |     | 7.5  |     | 9.5  |     | 10.0 |     | 12.0 |     | 15.0 |      | 20.0 | ns   |

Select devices have been discontinued.  
See Ordering Information section for product status.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup> (CONTINUED)

|                   |                                                                                                                                 | -5  |     | -6  |     | -7   |     | -10  |     | -12  |     | -15  |     | -20  |     | Unit |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|
|                   |                                                                                                                                 | Min | Max | Min | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |
| Frequency:        |                                                                                                                                 |     |     |     |     |      |     |      |     |      |     |      |     |      |     |      |
| f <sub>MAX</sub>  | External feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COS</sub> )  | 133 |     | 125 |     | 100  |     | 83.3 |     | 71.4 |     | 55.6 |     | 45.5 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COSi</sub> ) | 182 |     | 167 |     | 125  |     | 100  |     | 83.3 |     | 62.5 |     | 50.0 |     | MHz  |
|                   | No feedback PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>HS</sub> )          | 200 |     | 167 |     | 167  |     | 125  |     | 100  |     | 83.3 |     | 83.3 |     | MHz  |
| f <sub>MAXA</sub> | External feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COA</sub> )  | 91  |     | 91  |     | 71.4 |     | 58.8 |     | 47.6 |     | 41.7 |     | 35.7 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COAi</sub> ) | 111 |     | 111 |     | 83.3 |     | 66.7 |     | 52.6 |     | 45.5 |     | 38.5 |     | MHz  |
|                   | No feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>HA</sub> )         | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |
| f <sub>MAXI</sub> | Maximum input register frequency 1/(t <sub>SIRS</sub> +t <sub>HIRS</sub> ) or 1/(2 x t <sub>WICW</sub> )                        | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |

### Notes:

- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ( $f_{MAX}/2$ ).

Select devices have been discontinued.  
See Ordering Information section for product status.

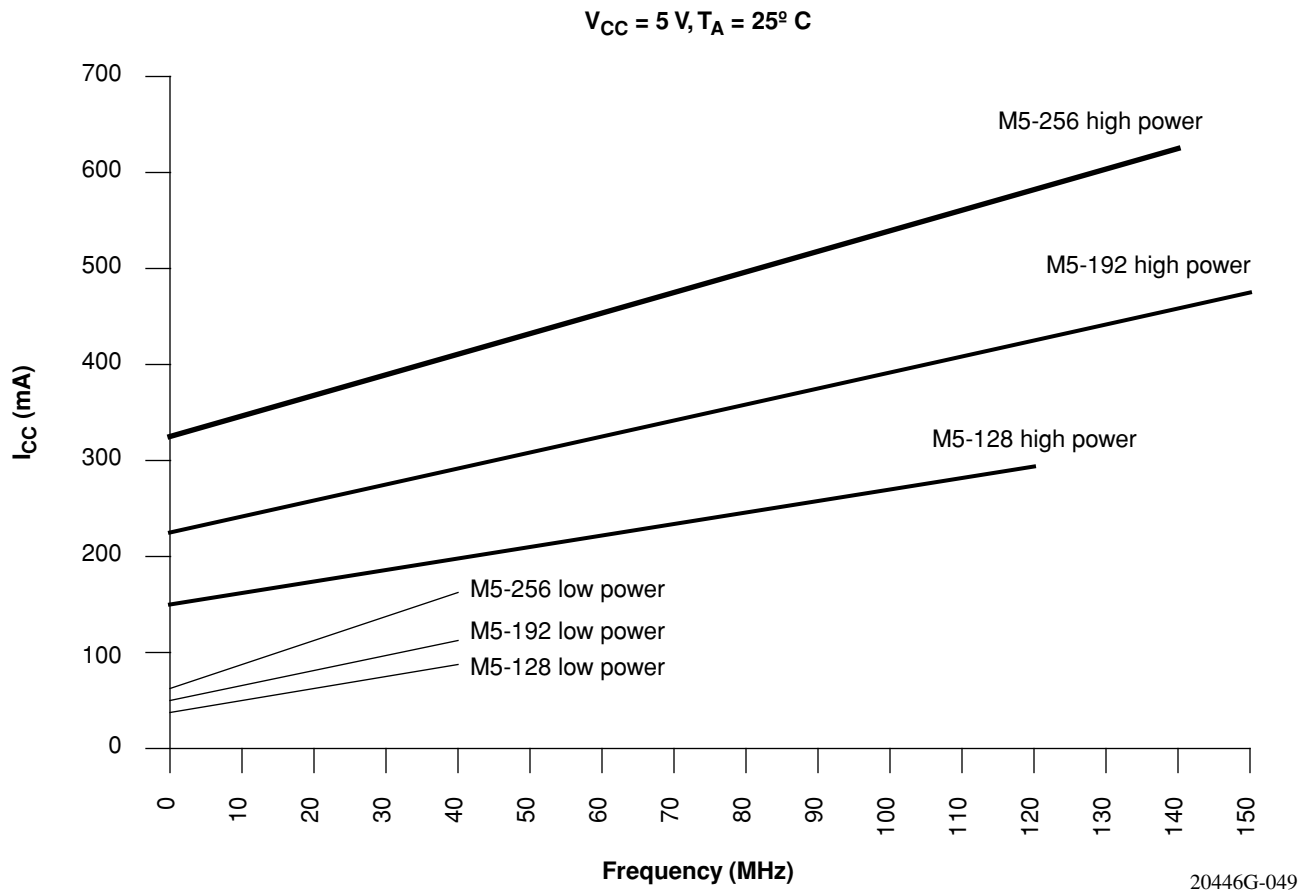


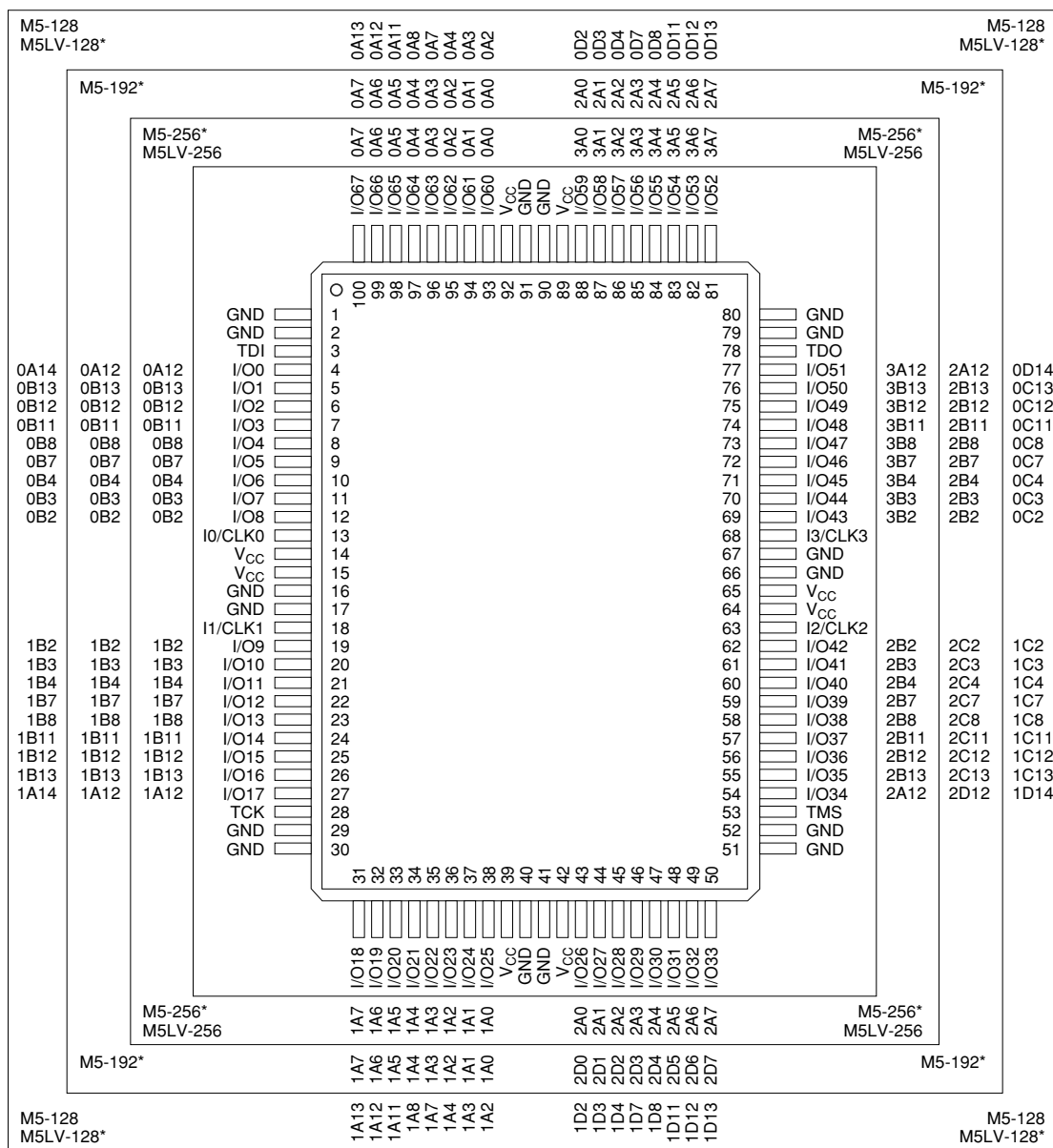
Figure 9.  $I_{CC}$  Curves at High/Low Power Modes

Select devices have been discontinued.  
See Ordering Information section for product status.

# 100-PIN PQFP CONNECTION DIAGRAM

## Top View

100-Pin PQFP (68 I/O)



\*Package obsolete, contact factory.

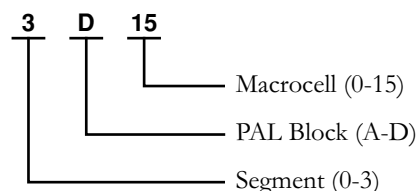
20446G-016

Select devices have been discontinued.  
See Ordering Information section for product status.

## Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

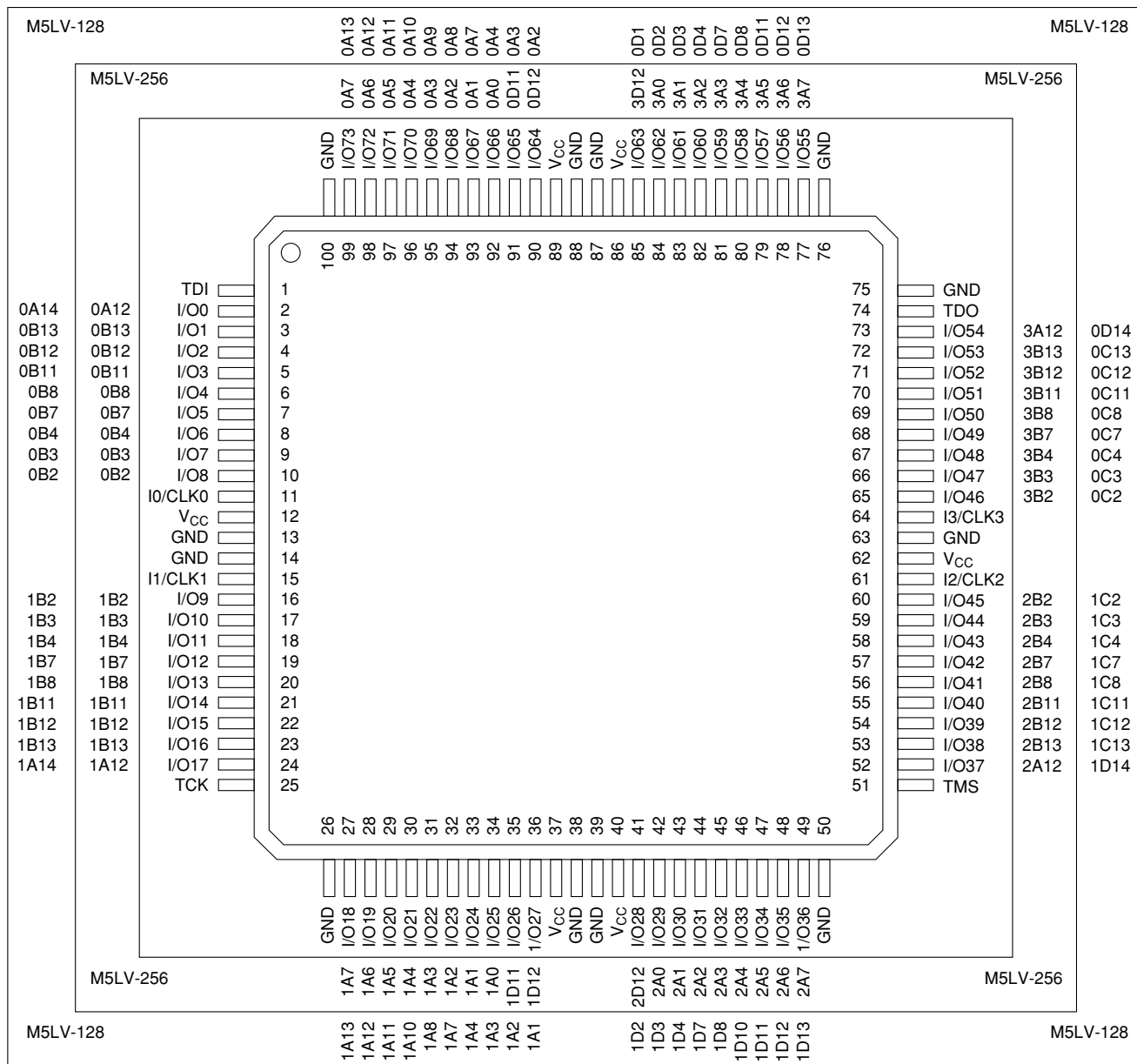
V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



# 100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

## Top View

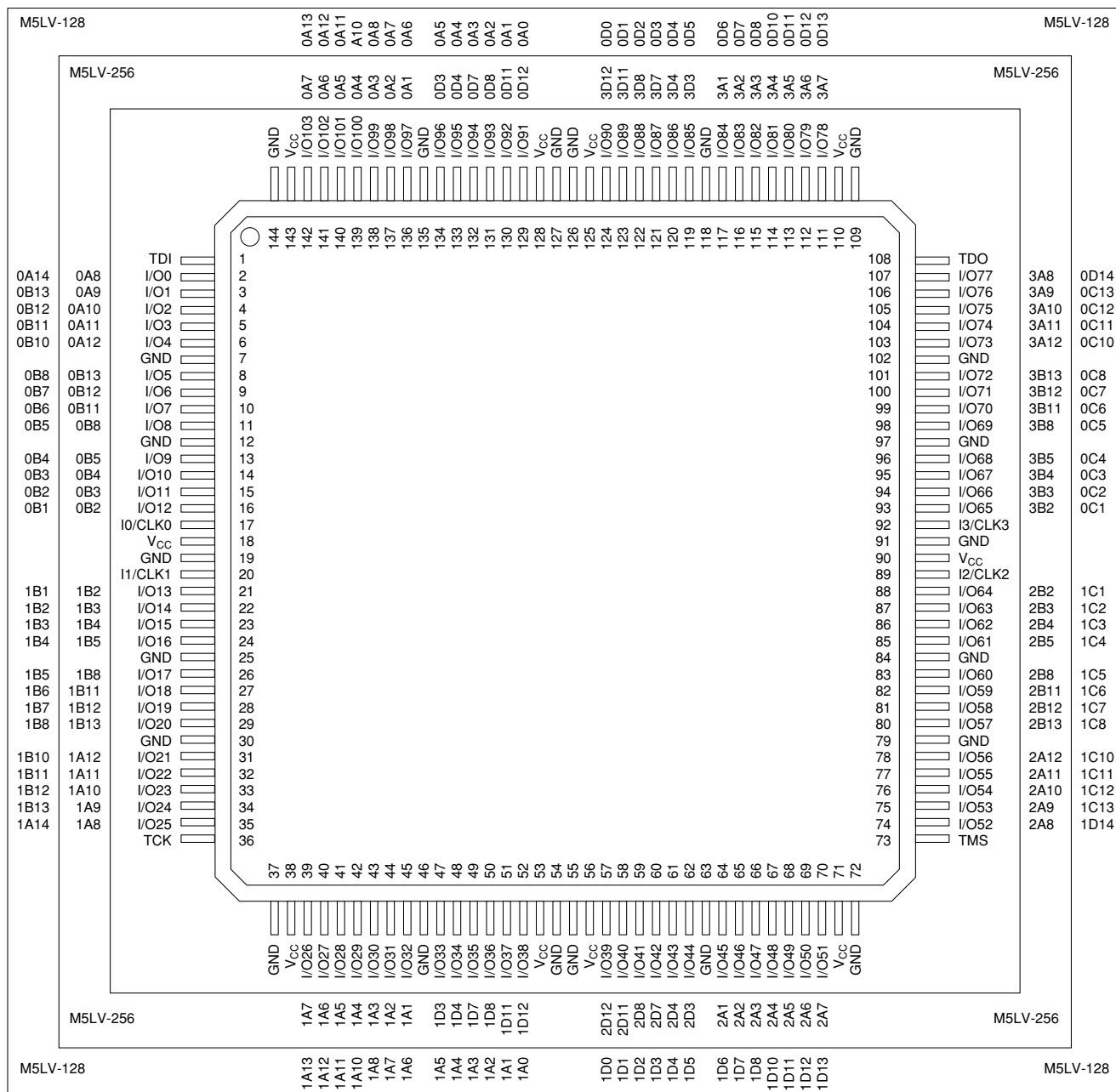
100-Pin TQFP (74 I/O)



# 144-PIN TQFP CONNECTION DIAGRAM

## Top View

144-Pin TQFP



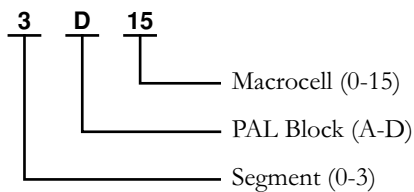
Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-020

### Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

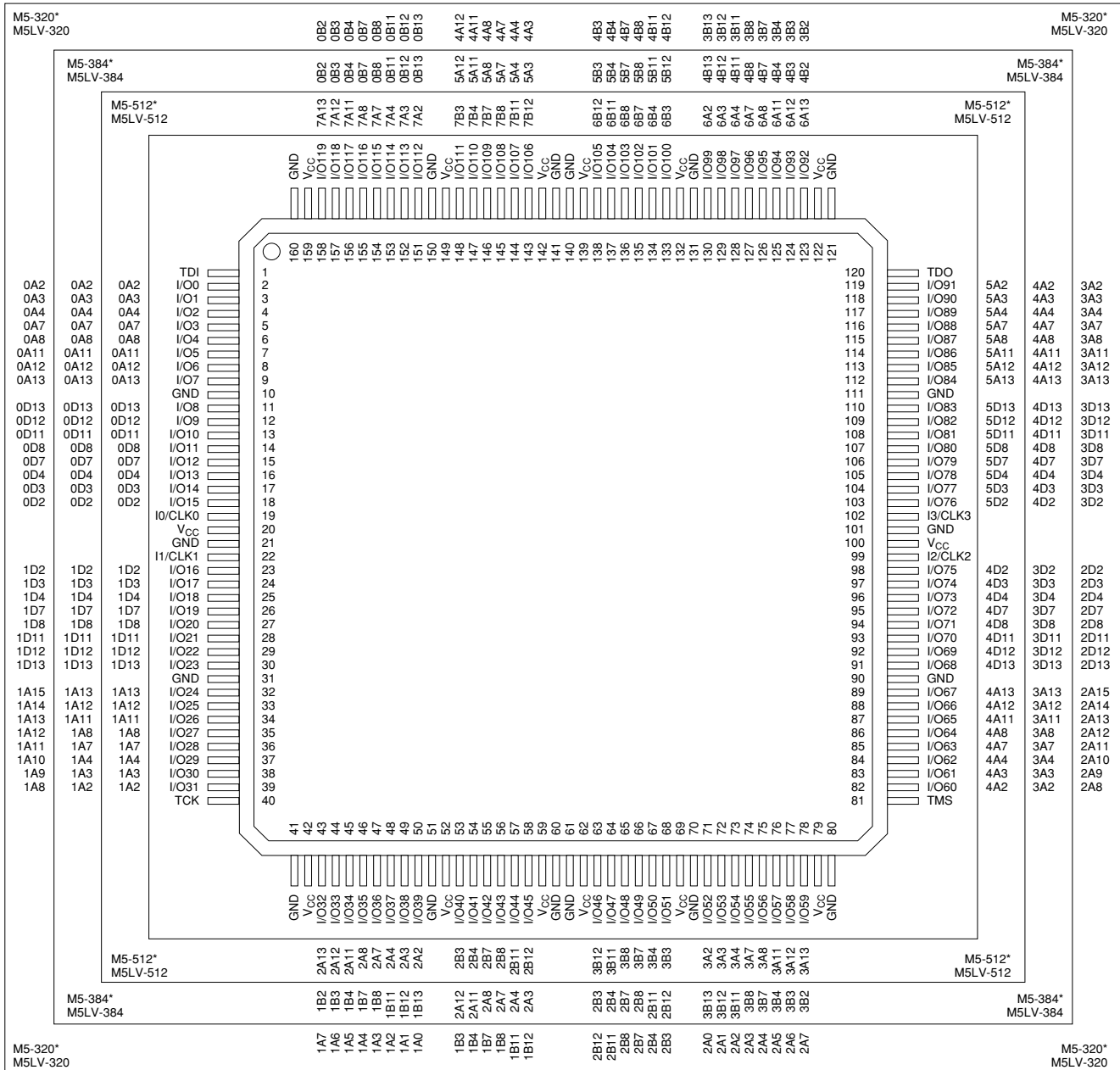
V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



# 160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

160-Pin PQFP (320, 384, 512 Macrocells)

Select devices have been discontinued.  
See Ordering Information section for product status.



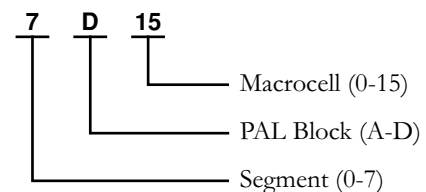
\*Package obsolete, contact factory.

20446G-022

## Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



## 256-BALL BGA CONNECTION DIAGRAM — M5-320

### Bottom View (I/O Pin-outs)

256-Ball BGA

|   | 20    | 19    | 18              | 17              | 16              | 15    | 14              | 13    | 12    | 11    | 10    | 9      | 8      | 7               | 6      | 5               | 4               | 3               | 2      | 1      |   |
|---|-------|-------|-----------------|-----------------|-----------------|-------|-----------------|-------|-------|-------|-------|--------|--------|-----------------|--------|-----------------|-----------------|-----------------|--------|--------|---|
| A | GND   | I/O11 | GND             | I/O44           | I/O58           | GND   | I/O70           | I/O76 | GND   | GND   | GND   | GND    | I/O108 | I/O116          | GND    | I/O128          | I/O134          | GND             | GND    | GND    | A |
| B | GND   | I/O12 | I/O28           | I/O45           | I/O59           | I/O64 | I/O71           | I/O77 | I/O84 | I/O90 | I/O96 | I/O102 | I/O109 | I/O117          | I/O122 | I/O129          | I/O135          | I/O148          | I/O164 | GND    | B |
| C | I/O0  | I/O13 | V <sub>CC</sub> | I/O46           | I/O60           | I/O65 | I/O72           | I/O78 | I/O85 | I/O91 | I/O97 | I/O103 | I/O110 | I/O118          | I/O123 | I/O130          | I/O136          | V <sub>CC</sub> | I/O165 | I/O181 | C |
| D | I/O1  | I/O14 | I/O29           | V <sub>CC</sub> | V <sub>CC</sub> | I/O66 | V <sub>CC</sub> | I/O79 | I/O86 | I/O92 | I/O98 | I/O104 | I/O111 | V <sub>CC</sub> | I/O124 | V <sub>CC</sub> | V <sub>CC</sub> | I/O149          | I/O166 | I/O182 | D |
| E | I/O2  | I/O15 | I/O30           | TDI             |                 |       |                 |       |       |       |       |        |        |                 |        |                 | TDI             | I/O150          | I/O167 | I/O183 | E |
| F | GND   | I/O16 | I/O31           | I/O47           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O137          | I/O151          | I/O168 | GND    | F |
| G | I/O3  | I/O17 | I/O32           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O152          | I/O169 | I/O184 | G |
| H | GND   | I/O18 | I/O33           | I/O48           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O138          | I/O153          | I/O170 | GND    | H |
| J | I/O4  | I/O19 | I/O34           | I/O49           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O139          | I/O154          | I/O171 | I/O185 | J |
| K | GND   | I/O20 | I/O35           | I/O50           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O140          | I/O155          | I/O172 | I/O186 | K |
| L | I/O5  | I/O21 | I/O36           | I/O51           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O141          | I/O156          | I/O173 | GND    | L |
| M | I/O6  | I/O22 | I/O37           | I/O52           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O142          | I/O157          | I/O174 | I/O187 | M |
| N | GND   | I/O23 | I/O38           | I/O53           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O143          | I/O158          | I/O175 | GND    | N |
| P | I/O7  | I/O24 | I/O39           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O159          | I/O176 | I/O188 | P |
| R | GND   | I/O25 | I/O40           | I/O54           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O144          | I/O160          | I/O177 | GND    | R |
| T | I/O8  | I/O26 | I/O41           | TCK             |                 |       |                 |       |       |       |       |        |        |                 |        |                 | TMS             | I/O161          | I/O178 | I/O189 | T |
| U | I/O9  | I/O27 | I/O42           | V <sub>CC</sub> |                 |       |                 |       |       |       |       |        |        |                 |        |                 | V <sub>CC</sub> | I/O162          | I/O179 | I/O190 | U |
| V | I/O10 | I/O28 | V <sub>CC</sub> | I/O55           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O145          | V <sub>CC</sub> | I/O180 | I/O191 | V |
| W | GND   | I/O29 | I/O43           | I/O56           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O146          | I/O163          | I/O181 | GND    | W |
| Y | GND   | I/O30 | GND             | I/O57           |                 |       |                 |       |       |       |       |        |        |                 |        |                 | I/O147          | GND             | I/O182 | I/O192 | Y |

#### Pin Designations

|                 |   |                  |
|-----------------|---|------------------|
| CLK             | = | Clock            |
| GND             | = | Ground           |
| I               | = | Input            |
| I/O             | = | Input/Output     |
| NC              | = | No Connect       |
| V <sub>CC</sub> | = | Supply Voltage   |
| TDI             | = | Test Data In     |
| TCK             | = | Test Clock       |
| TMS             | = | Test Mode Select |
| TDO             | = | Test Data Out    |

Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-026

# 352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

## Bottom View (I/O Pin-outs)

### 352-Ball BGA

|    | A      | B      | C      | D               | E               | F      | G      | H      | J               | K      | L               | M      | N      | P      | R               | T      | U      | V      | W               | Y      | AA              | AB     | AC     | AD     | AE     | AF     |
|----|--------|--------|--------|-----------------|-----------------|--------|--------|--------|-----------------|--------|-----------------|--------|--------|--------|-----------------|--------|--------|--------|-----------------|--------|-----------------|--------|--------|--------|--------|--------|
| 1  | NC     | NC     | NC     | GND             | NC              | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 2  | NC     | NC     | NC     | I/O205          | I/O224          | I/O206 | I/O207 | I/O208 | I/O209          | I/O210 | I/O211          | I/O212 | I/O213 | I/O214 | I/O215          | I/O216 | I/O217 | I/O218 | I/O219          | I/O220 | I/O221          | I/O222 | I/O223 | I/O243 | I/O255 | I/O255 |
| 3  | GND    | GND    | NC     | NC              | TDO             | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 4  | NC     | I/O188 | NC     | I/O184          | V <sub>CC</sub> | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 5  | GND    | I/O183 | I/O177 | I/O178          | I/O178          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 6  | NC     | I/O176 | I/O177 | I/O178          | I/O178          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 7  | GND    | I/O169 | I/O170 | I/O171          | I/O171          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 8  | I/O162 | I/O163 | I/O164 | I/O165          | I/O165          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 9  | I/O156 | I/O157 | I/O158 | I/O159          | I/O159          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 10 | GND    | I/O150 | I/O151 | V <sub>CC</sub> | V <sub>CC</sub> | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 11 | I/O142 | I/O143 | I/O144 | I/O145          | I/O145          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 12 | I/O134 | I/O135 | I/O136 | I/O137          | I/O137          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 13 | I/O128 | I/O129 | I/O130 | I/O131          | I/O131          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 14 | GND    | I/O122 | I/O123 | V <sub>CC</sub> | V <sub>CC</sub> | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 15 | I/O114 | I/O115 | I/O116 | I/O117          | I/O117          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 16 | NC     | I/O107 | I/O108 | I/O109          | I/O109          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 17 | I/O101 | I/O102 | I/O103 | I/O104          | I/O104          | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 18 | GND    | I/O95  | I/O96  | V <sub>CC</sub> | V <sub>CC</sub> | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 19 | I/O87  | I/O88  | I/O89  | I/O90           | I/O90           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 20 | I/O80  | I/O81  | I/O82  | I/O83           | I/O83           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 21 | I/O73  | I/O74  | I/O75  | I/O76           | I/O76           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 22 | GND    | I/O68  | I/O69  | I/O70           | I/O70           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 23 | I/O51  | I/O52  | I/O53  | V <sub>CC</sub> | I/O54           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 24 | NC     | NC     | TDI    | I/O32           | I/O33           | I/O189 | I/O190 | I/O191 | V <sub>CC</sub> | I/O192 | V <sub>CC</sub> | I/O193 | I/O194 | I/O195 | V <sub>CC</sub> | I/O196 | I/O197 | I/O198 | V <sub>CC</sub> | I/O199 | V <sub>CC</sub> | I/O200 | I/O201 | I/O223 | I/O243 | I/O255 |
| 25 | GND    | GND    | I/O11  | I/O12           | I/O13           | I/O14  | I/O15  | I/O16  | I/O17           | I/O18  | I/O19           | I/O20  | I/O21  | I/O22  | I/O23           | I/O24  | I/O25  | I/O26  | I/O27           | I/O28  | I/O29           | I/O30  | I/O31  | NC     | NC     | NC     |
| 26 | NC     | NC     | GND    | I/O0            | NC              | GND    | I/O1   | I/O2   | GND             | I/O3   | I/O4            | I/O5   | GND    | I/O6   | I/O7            | GND    | I/O8   | I/O9   | GND             | I/O10  | NC              | NC     | GND    | NC     | NC     | NC     |

Pin Designations

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

NC = No Connect

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

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### Pin Designations

|                 |   |                  |
|-----------------|---|------------------|
| CLK             | = | Clock            |
| GND             | = | Ground           |
| I               | = | Input            |
| I/O             | = | Input/Output     |
| NC              | = | No Connect       |
| V <sub>CC</sub> | = | Supply Voltage   |
| TDI             | = | Test Data In     |
| TCK             | = | Test Clock       |
| TMS             | = | Test Mode Select |
| TDO             | = | Test Data Out    |

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Select devices have been discontinued.  
See Ordering Information section for product status.