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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

|                                 |                                                                                                                                                                       |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                              |
| Programmable Type               | In System Programmable                                                                                                                                                |
| Delay Time tpd(1) Max           | 15 ns                                                                                                                                                                 |
| Voltage Supply - Internal       | 3V ~ 3.6V                                                                                                                                                             |
| Number of Logic Elements/Blocks | -                                                                                                                                                                     |
| Number of Macrocells            | 128                                                                                                                                                                   |
| Number of Gates                 | -                                                                                                                                                                     |
| Number of I/O                   | 74                                                                                                                                                                    |
| Operating Temperature           | -40°C ~ 85°C (TA)                                                                                                                                                     |
| Mounting Type                   | Surface Mount                                                                                                                                                         |
| Package / Case                  | 100-LQFP                                                                                                                                                              |
| Supplier Device Package         | 100-TQFP (14x14)                                                                                                                                                      |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-128-74-15vi">https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-128-74-15vi</a> |



Table 1. MACH 5 Device Features <sup>1</sup>

| Feature                             | M5-128/1<br>M5LV-128 |     | M5-192/1 | M5-256/1<br>M5LV-256 |     | M5-320<br>M5LV-320 |     | M5-384<br>M5LV-384 |     | M5-512<br>M5LV-512 |     |
|-------------------------------------|----------------------|-----|----------|----------------------|-----|--------------------|-----|--------------------|-----|--------------------|-----|
| Supply Voltage (V)                  | 5                    | 3.3 | 5        | 5                    | 3.3 | 5                  | 3.3 | 5                  | 3.3 | 5                  | 3.3 |
| Macrocells                          | 128                  | 128 | 192      | 256                  | 256 | 320                | 320 | 384                | 384 | 512                | 512 |
| Maximum User I/O Pins               | 120                  | 120 | 120      | 160                  | 160 | 192                | 160 | 160                | 160 | 256                | 256 |
| t <sub>PD</sub> (ns)                | 5.5                  | 5.5 | 5.5      | 5.5                  | 5.5 | 6.5                | 6.5 | 6.5                | 6.5 | 6.5                | 6.5 |
| t <sub>SS</sub> (ns)                | 3.0                  | 3.0 | 3.0      | 3.0                  | 3.0 | 3.0                | 3.0 | 3.0                | 3.0 | 3.0                | 3.0 |
| t <sub>COS</sub> (ns)               | 4.5                  | 4.5 | 4.5      | 4.5                  | 4.5 | 5.0                | 5.0 | 5.0                | 5.0 | 5.0                | 5.0 |
| f <sub>CNT</sub> (MHz)              | 182                  | 182 | 182      | 182                  | 182 | 167                | 167 | 167                | 167 | 167                | 167 |
| Typical Static Power (mA)           | 35                   | 35  | 45       | 55                   | 55  | 70                 | 70  | 75                 | 75  | 100                | 100 |
| IEEE 1149.1 Boundary Scan Compliant | Yes                  | Yes | Yes      | Yes                  | Yes | Yes                | Yes | Yes                | Yes | Yes                | Yes |
| PCI-Compliant                       | Yes                  | Yes | Yes      | Yes                  | Yes | Yes                | Yes | Yes                | Yes | Yes                | Yes |

**Note:**

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

## GENERAL DESCRIPTION

The MACH<sup>®</sup> 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E<sup>2</sup>CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.  
See Ordering Information section for product status.

Table 2. MACH 5 Speed Grades

| Device              | Speed Grade <sup>1</sup> |    |      |      |      |      |     |
|---------------------|--------------------------|----|------|------|------|------|-----|
|                     | -5                       | -6 | -7   | -10  | -12  | -15  | -20 |
| M5-128 <sup>2</sup> |                          |    | C    | C, I | C, I | C, I | I   |
| M5-128/1            | C                        |    | C, I | C, I | C, I | C, I | I   |
| M5LV-128            | C                        |    | C, I | C, I | C, I | I    |     |
| M5-192/1            | C                        |    | C, I | C, I | C, I | C, I | I   |
| M5-256 <sup>2</sup> |                          |    | C    | C, I | C, I | C, I | I   |
| M5-256/1            | C                        |    | C, I | C, I | C, I | C, I | I   |
| M5LV-256            | C                        |    | C, I | C, I | C, I | I    |     |
| M5-320              |                          | C  | C, I | C, I | C, I | C, I | I   |
| M5LV-320            |                          | C  | C, I | C, I | C, I | C, I | I   |
| M5-384              |                          | C  | C, I | C, I | C, I | C, I | I   |
| M5LV-384            |                          | C  | C, I | C, I | C, I | C, I | I   |
| M5-512              |                          | C  | C, I | C, I | C, I | C, I | I   |
| M5LV-512            |                          | C  | C, I | C, I | C, I | C, I | I   |

**Note:**

1. C = Commercial grade, I = Industrial grade
2. /1 version recommended for new designs

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL<sup>®</sup> block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options <sup>1</sup>

|              | M5-128/1<br>M5LV-128 |        | M5-192/1 | M5-256/1<br>M5LV-256 |         | M5-320<br>M5LV-320 |      | M5-384<br>M5LV-384 |      | M5-512<br>M5LV-512 |      |
|--------------|----------------------|--------|----------|----------------------|---------|--------------------|------|--------------------|------|--------------------|------|
|              | 5                    | 3.3    |          | 5                    | 3.3     | 5                  | 3.3  | 5                  | 3.3  | 5                  | 3.3  |
| 100-pin TQFP | 68                   | 68, 74 | 68       | 68                   | 68*, 74 |                    |      |                    |      |                    |      |
| 100-pin PQFP | 68                   | 68*    | 68*      | 68*                  | 68      |                    |      |                    |      |                    |      |
| 144-pin TQFP |                      | 104    |          |                      | 104     |                    |      |                    |      |                    |      |
| 144-pin PQFP | 104                  | 104*   | 104*     | 104*                 | 104*    |                    |      |                    |      |                    |      |
| 160-pin PQFP | 120                  | 120    | 120      | 120                  | 120     | 120*               | 120  | 120*               | 120  | 120*               | 120  |
| 208-pin PQFP |                      |        |          | 160                  | 160     | 160                | 160  | 160                | 160  | 160                | 160  |
| 240-pin PQFP |                      |        |          |                      |         | 184*               | 184* | 184*               | 184* | 184*               | 184* |
| 256-ball BGA |                      |        |          |                      |         | 192                | 192* | 192*               | 192* | 192*               | 192* |
| 352-ball BGA |                      |        |          |                      |         |                    |      |                    |      | 256                | 256  |

**Note:**

1. The I/O options indicated with a "\*" are obsolete, please contact factory for more information.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued.  
See Ordering Information section for product status.

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.

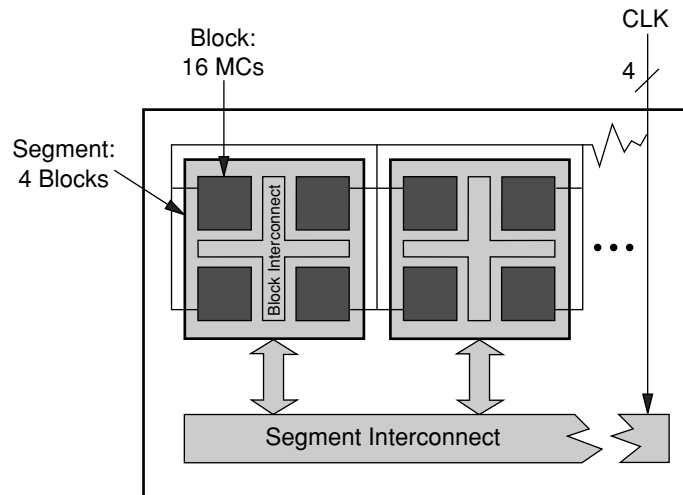


Figure 1. MACH 5 Block Diagram

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The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Select devices have been discontinued.  
See Ordering Information section for product status.

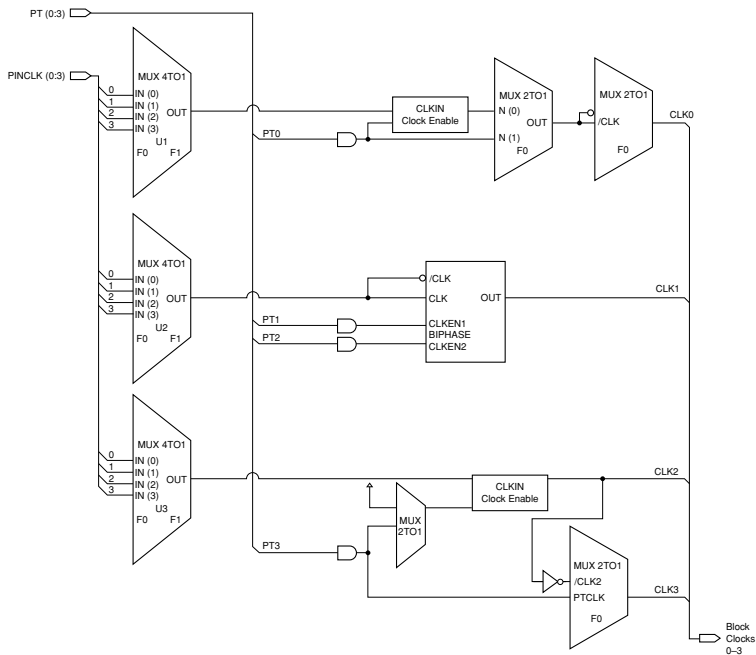
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

#### Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

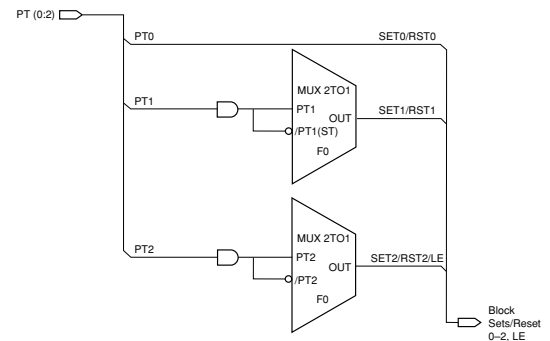
#### Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



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**Figure 4. Clock Generator**



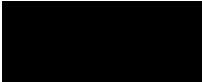
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**Figure 5. Set/Reset Generator**

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.  
See Ordering Information section for product status.**





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## MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

## IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

## IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

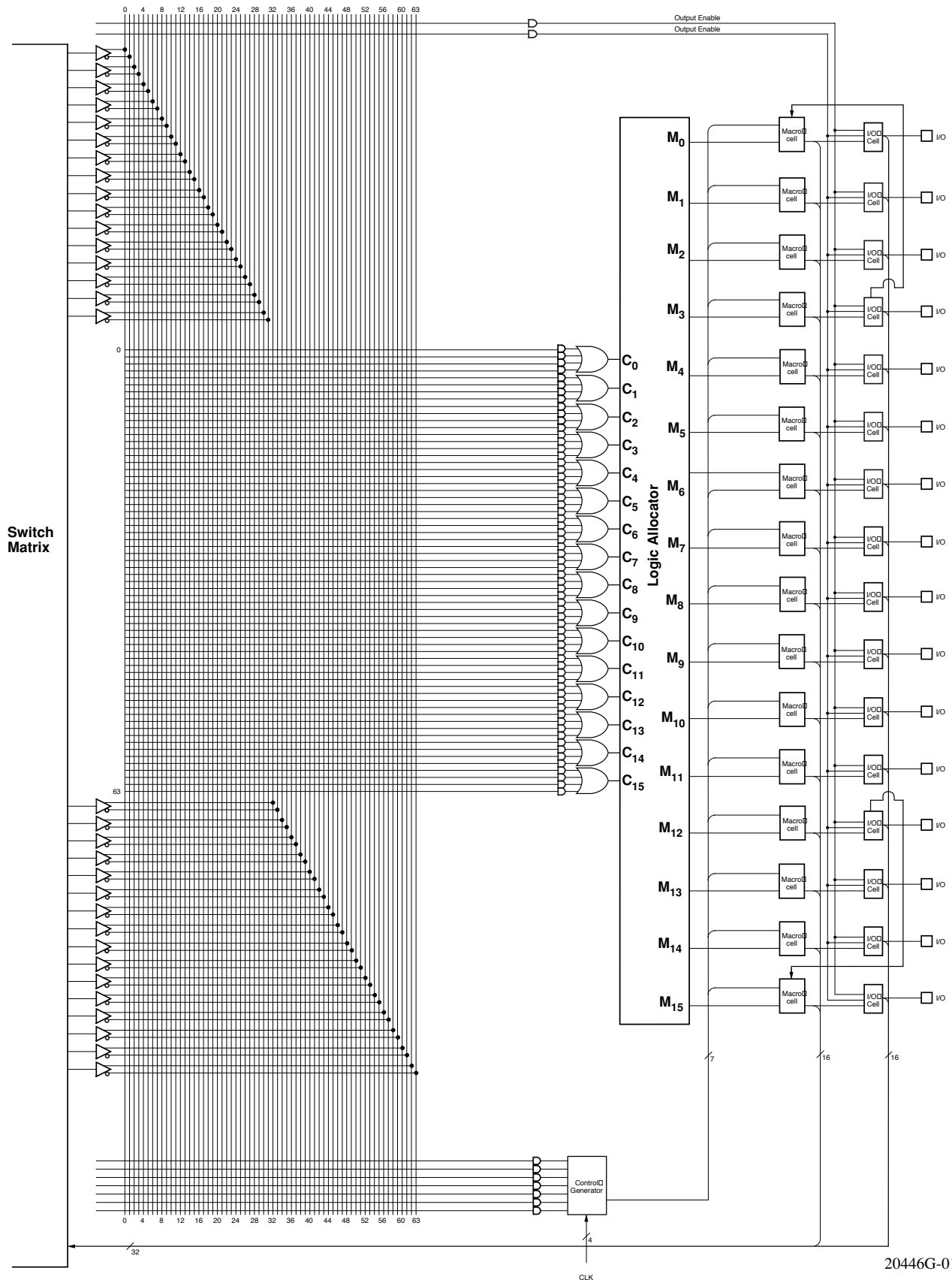
MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

## PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above  $V_{CC}$  because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.  
See Ordering Information section for product status.

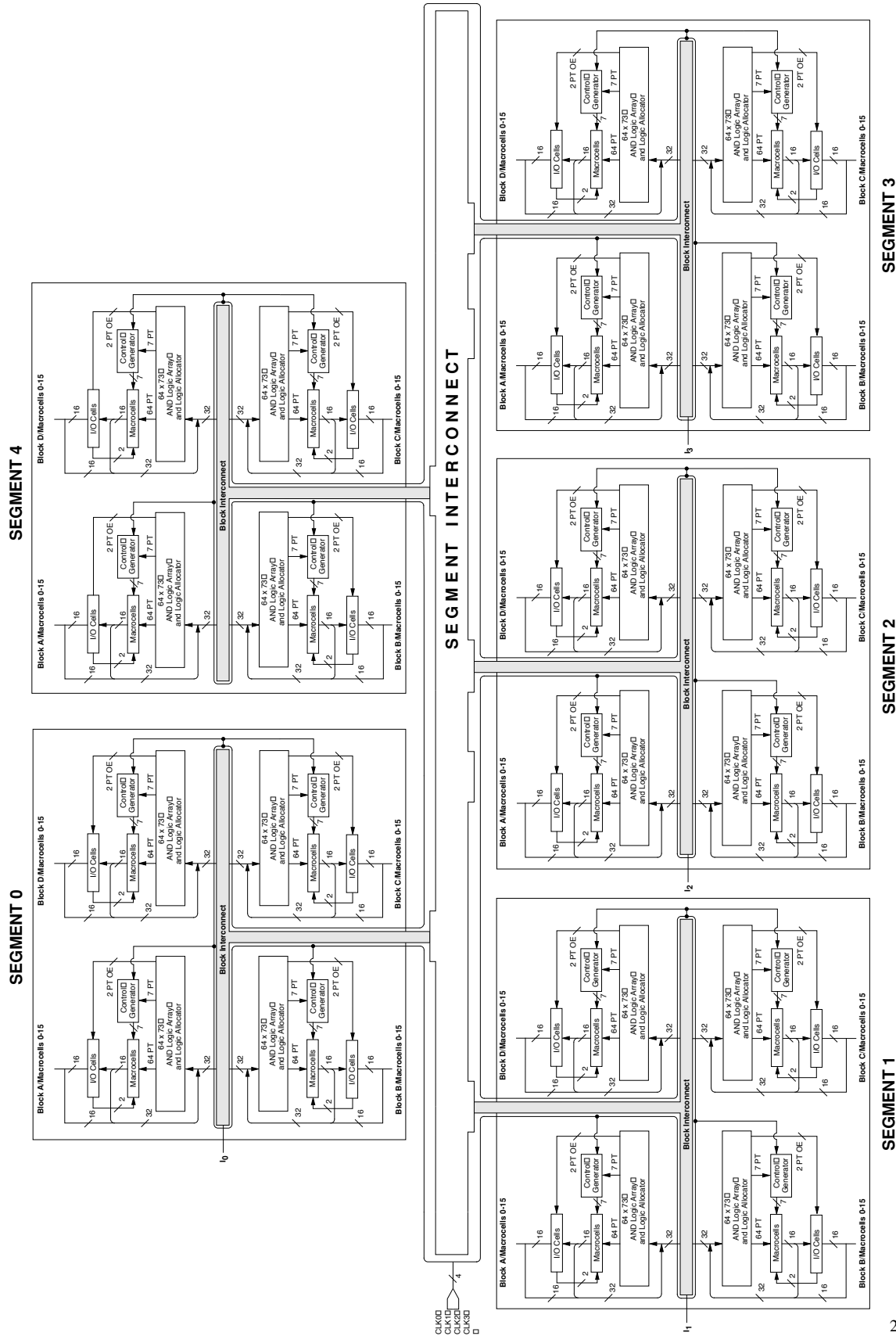
## MACH 5 PAL BLOCK



Select devices have been discontinued.  
See Ordering Information section for product status.

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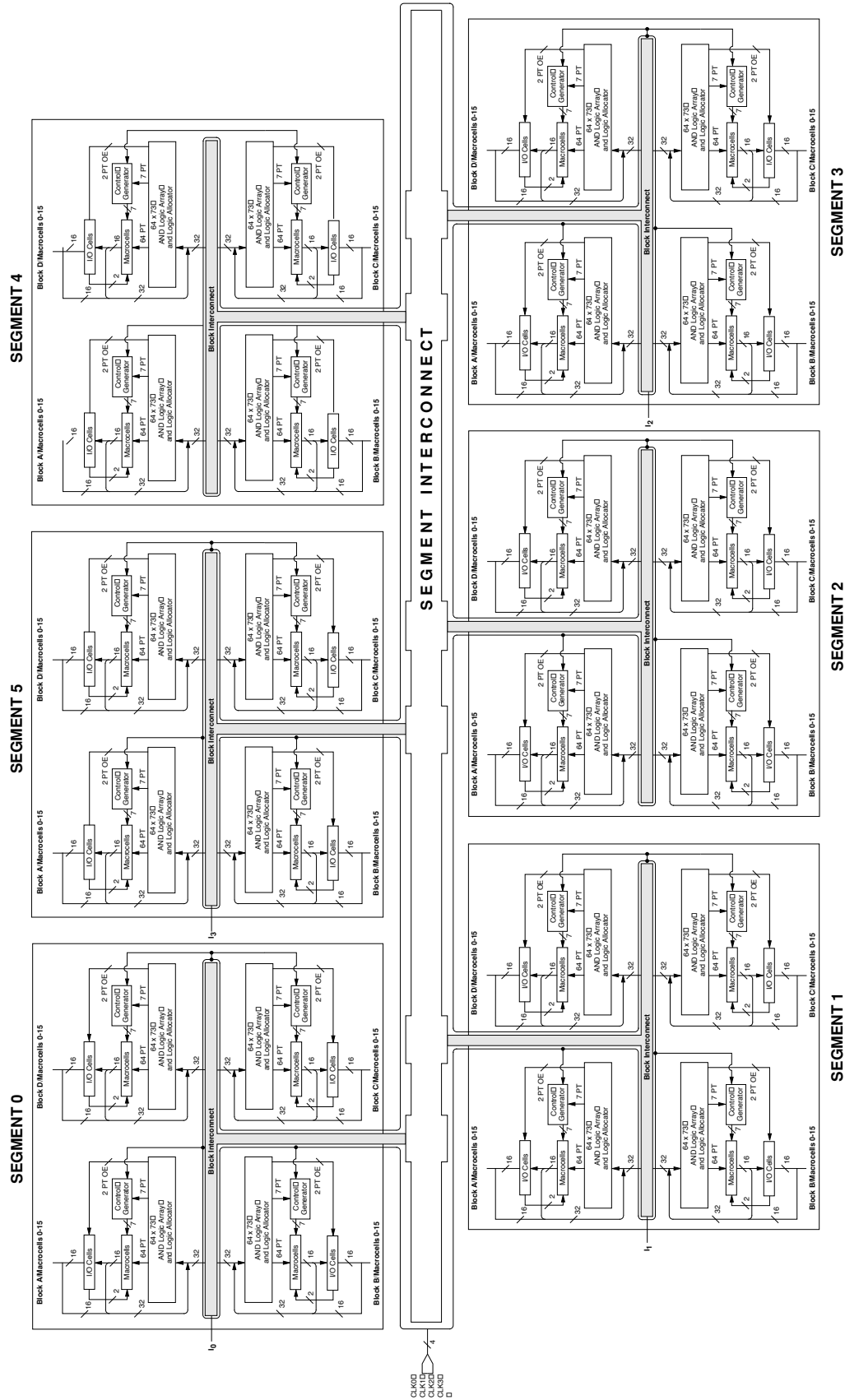
# BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.  
See Ordering Information section for product status.

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# BLOCK DIAGRAM — M5(LV)-384/XXX



20446G-011

Select devices have been discontinued.  
See Ordering Information section for product status.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup> (CONTINUED)

|                           |                                                                     | -5  |               | -6  |      | -7  |               | -10 |               | -12 |               | -15  |               | -20  |               | Unit |
|---------------------------|---------------------------------------------------------------------|-----|---------------|-----|------|-----|---------------|-----|---------------|-----|---------------|------|---------------|------|---------------|------|
|                           |                                                                     | Min | Max           | Min | Max  | Min | Max           | Min | Max           | Min | Max           | Min  | Max           | Min  | Max           |      |
| Power Delays:             |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>PL1</sub>          | Power level 1 delay (Note 2)                                        |     | 4.0<br>(5.0)  |     | 4.0  |     | 4.0<br>(5.0)  |     | 4.0<br>(5.0)  |     | 4.0<br>(5.0)  |      | 4.0<br>(5.0)  |      | 4.0<br>(5.0)  | ns   |
| t <sub>PL2</sub>          | Power level 2 delay (Note 2)                                        |     | 6.0<br>(9.0)  |     | 6.0  |     | 6.0<br>(9.0)  |     | 6.0<br>(9.0)  |     | 6.0<br>(9.0)  |      | 6.0<br>(9.0)  |      | 6.0<br>(9.0)  | ns   |
| t <sub>PL3</sub>          | Power level 3 delay (Note 2)                                        |     | 9.0<br>(17.5) |     | 9.0  |     | 9.0<br>(17.5) |     | 9.0<br>(17.5) |     | 9.0<br>(17.5) |      | 9.0<br>(17.5) |      | 9.0<br>(17.5) | ns   |
| Additional Cluster Delay: |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>PT</sub>           | Product term cluster delay                                          |     | 0.3           |     | 0.3  |     | 0.3           |     | 0.3           |     | 0.3           |      | 0.3           |      | 0.3           | ns   |
| Interconnect Delays:      |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>BLK</sub>          | Block interconnect delay                                            |     | 1.5           |     | 1.5  |     | 1.5           |     | 2.0           |     | 2.0           |      | 2.0           |      | 2.0           | ns   |
| t <sub>SEG</sub>          | Segment interconnect delay                                          |     | 4.5           |     | 4.5  |     | 5.0           |     | 6.0           |     | 6.0           |      | 6.0           |      | 6.0           | ns   |
| Reset and Preset Delays:  |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>SRI</sub>          | Asynchronous reset or preset to internal register output            |     | 6.0           |     | 8.0  |     | 8.0           |     | 10.0          |     | 12.0          |      | 14.0          |      | 16.0          | ns   |
| t <sub>SR</sub>           | Asynchronous reset or preset to register output                     |     | 8.0           |     | 10.0 |     | 10.0          |     | 12.0          |     | 14.0          |      | 16.0          |      | 18.0          | ns   |
| t <sub>SRR</sub>          | Reset and set register recovery time                                | 5.5 |               | 7.5 |      | 7.5 |               | 8.0 |               | 9.0 |               | 10.0 |               | 11.0 |               | ns   |
| t <sub>SRW</sub>          | Asynchronous reset or preset width                                  | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 7.0  |               | 8.0  |               | ns   |
| Clock Enable Delays:      |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>CES</sub>          | Clock enable setup time                                             | 4.0 |               | 5.0 |      | 5.0 |               | 6.0 |               | 7.0 |               | 7.0  |               | 8.0  |               | ns   |
| t <sub>CEH</sub>          | Clock enable hold time                                              | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 6.0  |               | 7.0  |               | ns   |
| Width:                    |                                                                     |     |               |     |      |     |               |     |               |     |               |      |               |      |               |      |
| t <sub>WLS</sub>          | Global clock width low (Note 3)                                     | 2.5 |               | 3.0 |      | 3.0 |               | 4.0 |               | 5.0 |               | 6.0  |               | 6.0  |               | ns   |
| t <sub>WHS</sub>          | Global clock width high (Note 3)                                    | 2.5 |               | 3.0 |      | 3.0 |               | 4.0 |               | 5.0 |               | 6.0  |               | 6.0  |               | ns   |
| t <sub>WLA</sub>          | Product term clock width low                                        | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 7.0  |               | 8.0  |               | ns   |
| t <sub>WHA</sub>          | Product term clock width high                                       | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 7.0  |               | 8.0  |               | ns   |
| t <sub>GWA</sub>          | Gate width low (for low transparent) or high (for high transparent) | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 7.0  |               | 8.0  |               | ns   |
| t <sub>WIR</sub>          | Input register clock width low or high                              | 3.0 |               | 4.0 |      | 4.0 |               | 5.0 |               | 6.0 |               | 7.0  |               | 8.0  |               | ns   |

Select devices have been discontinued.  
See Ordering Information section for product status.

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup> (CONTINUED)

|                   |                                                                                                                                 | -5  |     | -6  |     | -7   |     | -10  |     | -12  |     | -15  |     | -20  |     | Unit |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|
|                   |                                                                                                                                 | Min | Max | Min | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |
| Frequency:        |                                                                                                                                 |     |     |     |     |      |     |      |     |      |     |      |     |      |     |      |
| f <sub>MAX</sub>  | External feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COS</sub> )  | 133 |     | 125 |     | 100  |     | 83.3 |     | 71.4 |     | 55.6 |     | 45.5 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COSi</sub> ) | 182 |     | 167 |     | 125  |     | 100  |     | 83.3 |     | 62.5 |     | 50.0 |     | MHz  |
|                   | No feedback PAL block level. Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>HS</sub> )          | 200 |     | 167 |     | 167  |     | 125  |     | 100  |     | 83.3 |     | 83.3 |     | MHz  |
| f <sub>MAXA</sub> | External feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COA</sub> )  | 91  |     | 91  |     | 71.4 |     | 58.8 |     | 47.6 |     | 41.7 |     | 35.7 |     | MHz  |
|                   | Internal feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COAi</sub> ) | 111 |     | 111 |     | 83.3 |     | 66.7 |     | 52.6 |     | 45.5 |     | 38.5 |     | MHz  |
|                   | No feedback, PAL block level. Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>HA</sub> )         | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |
| f <sub>MAXI</sub> | Maximum input register frequency 1/(t <sub>SIRS</sub> + t <sub>HIRS</sub> ) or 1/(2 x t <sub>WICW</sub> )                       | 167 |     | 125 |     | 125  |     | 100  |     | 83.3 |     | 71.4 |     | 62.5 |     | MHz  |

### Notes:

- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ( $f_{MAX}/2$ ).

Select devices have been discontinued.  
See Ordering Information section for product status.

## CAPACITANCE<sup>1</sup>

| Parameter Symbol | Parameter Description | Test conditions           |                            | Typ | Unit |
|------------------|-----------------------|---------------------------|----------------------------|-----|------|
| $C_{IN}$         | I/CLK pin             | $V_{IN} = 2.0 \text{ V}$  | 3.3 V or 5 V, 25° C, 1 MHz | 12  | pF   |
| $C_{I/O}$        | I/O pin               | $V_{OUT} = 2.0 \text{ V}$ | 3.3 V or 5 V, 25° C, 1 MHz | 10  | pF   |

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

## $I_{CC}$ vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

## $I_{CC}$ CURVES AT HIGH /LOW POWER MODES

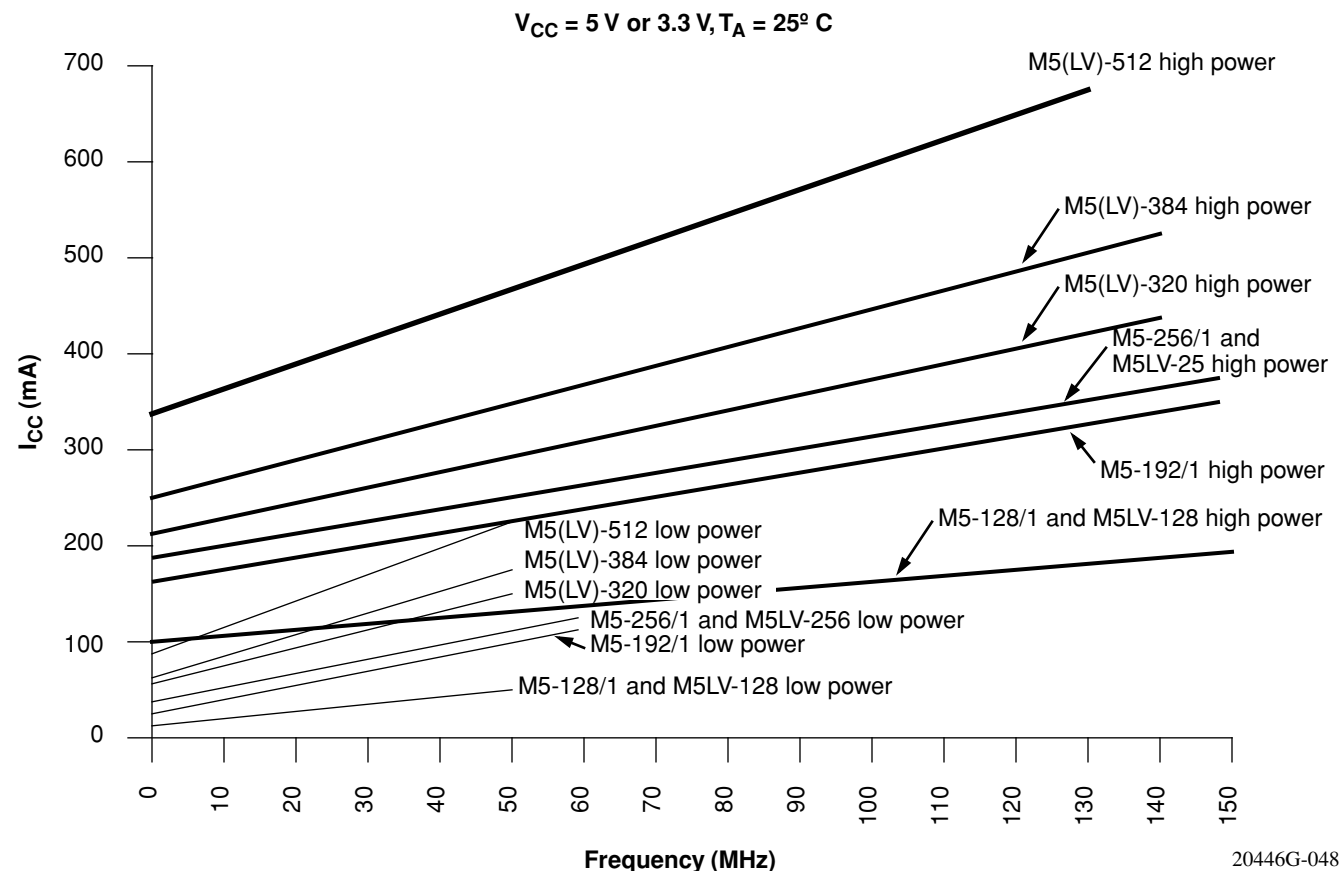


Figure 8.  $I_{CC}$  Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

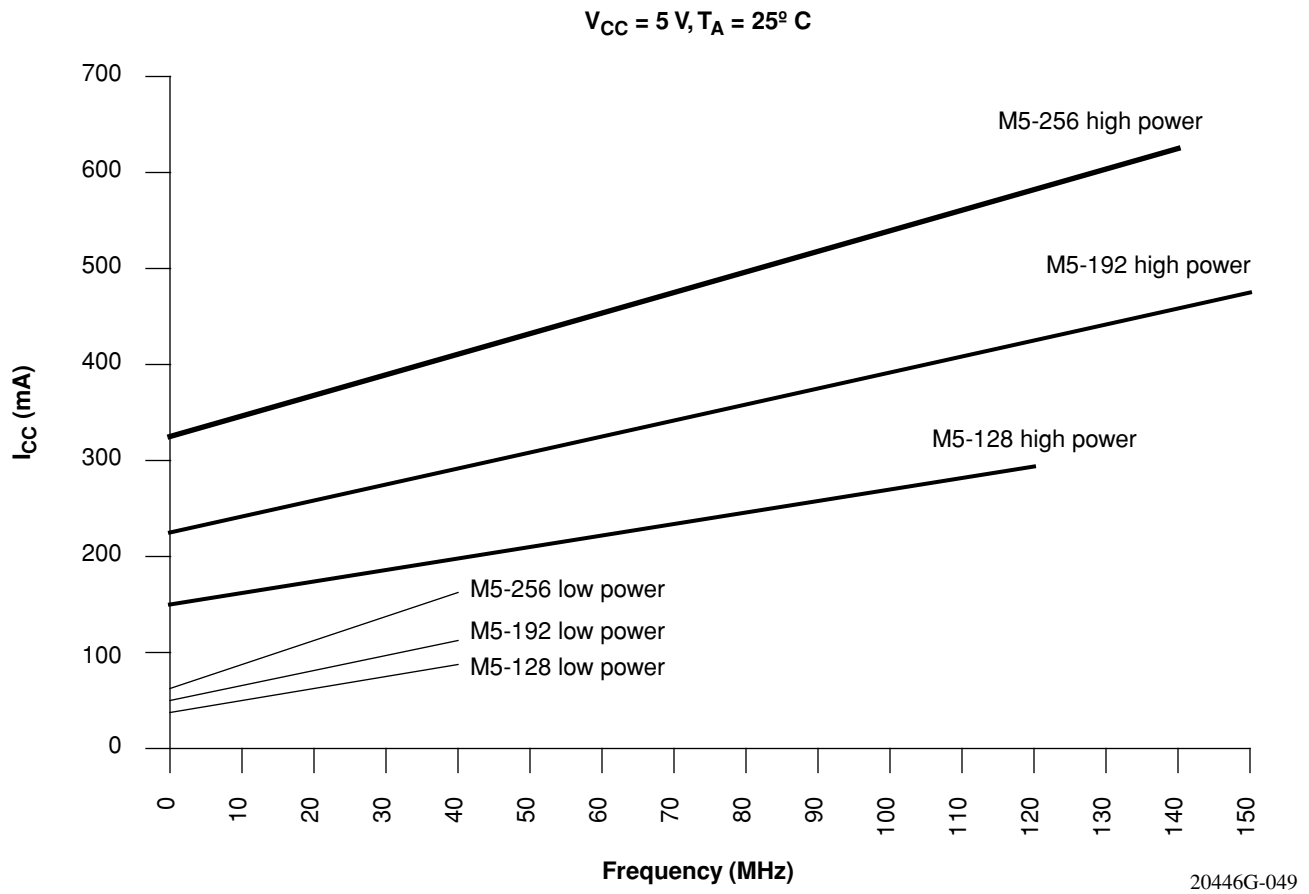


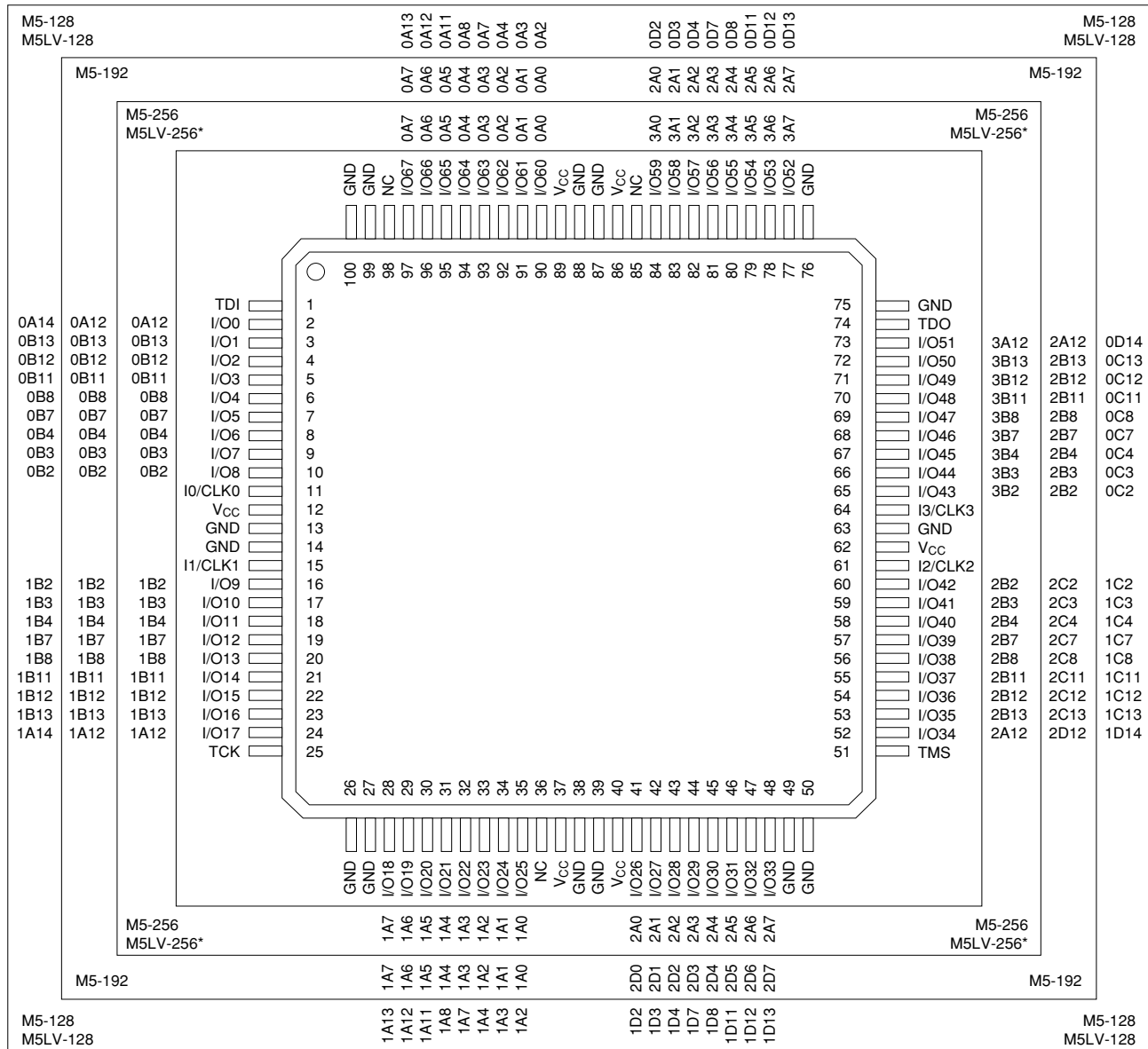
Figure 9.  $I_{CC}$  Curves at High/Low Power Modes

Select devices have been discontinued.  
See Ordering Information section for product status.

# 100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

## Top View

100-Pin TQFP (68 I/O)



\*Package obsolete, contact factory.

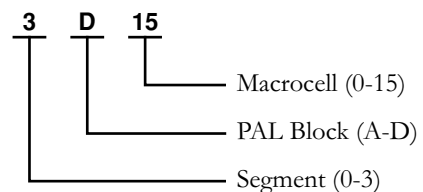
Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-017

### Pin Designations

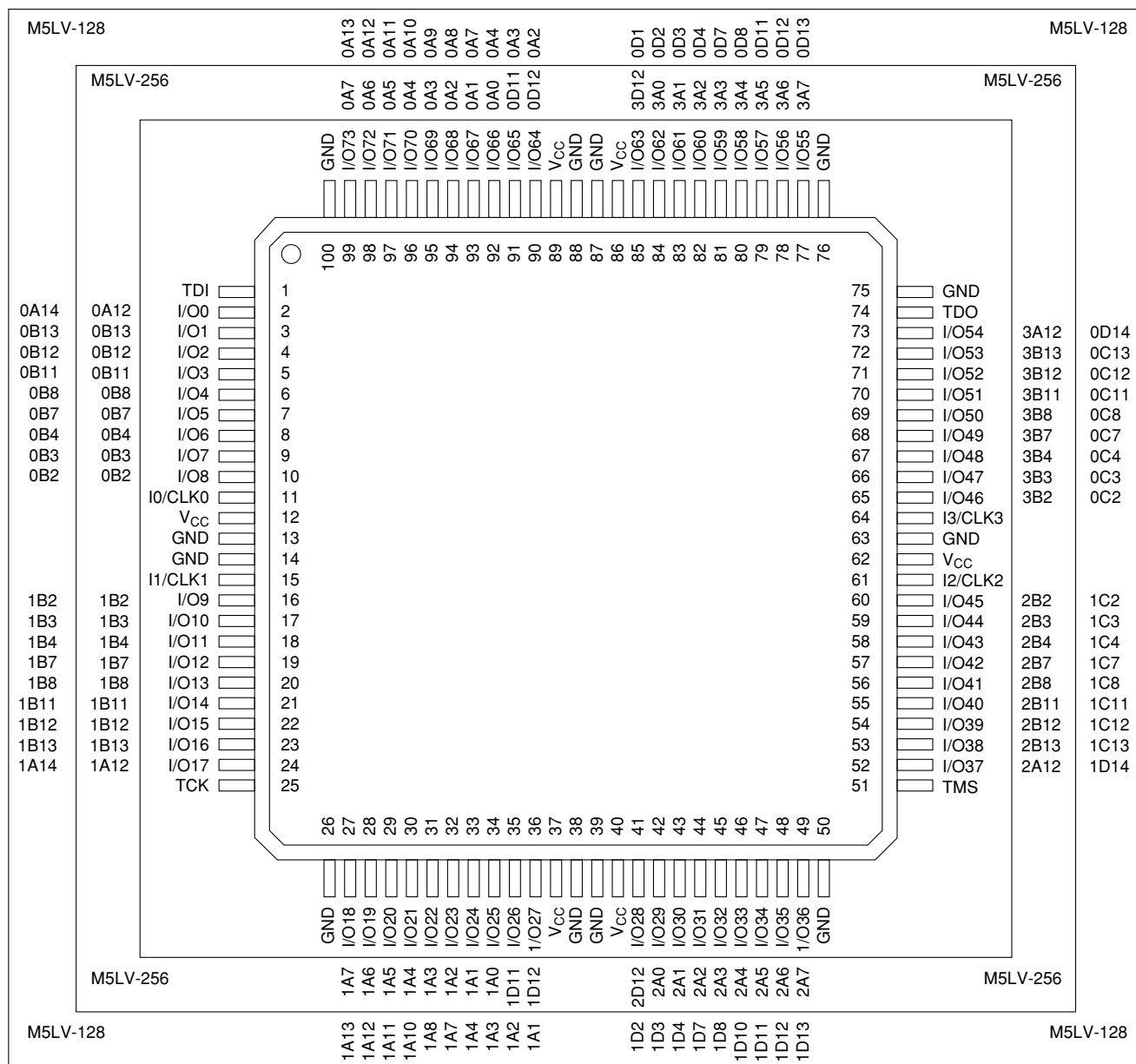
CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



### Top View

### 100-Pin TQFP (74 I/O)



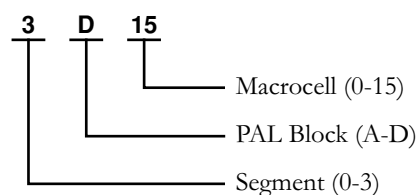
**Select devices have been discontinued.  
See Ordering Information for product status.**

20446G-018

## Pin Designations

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 NC = No Connect

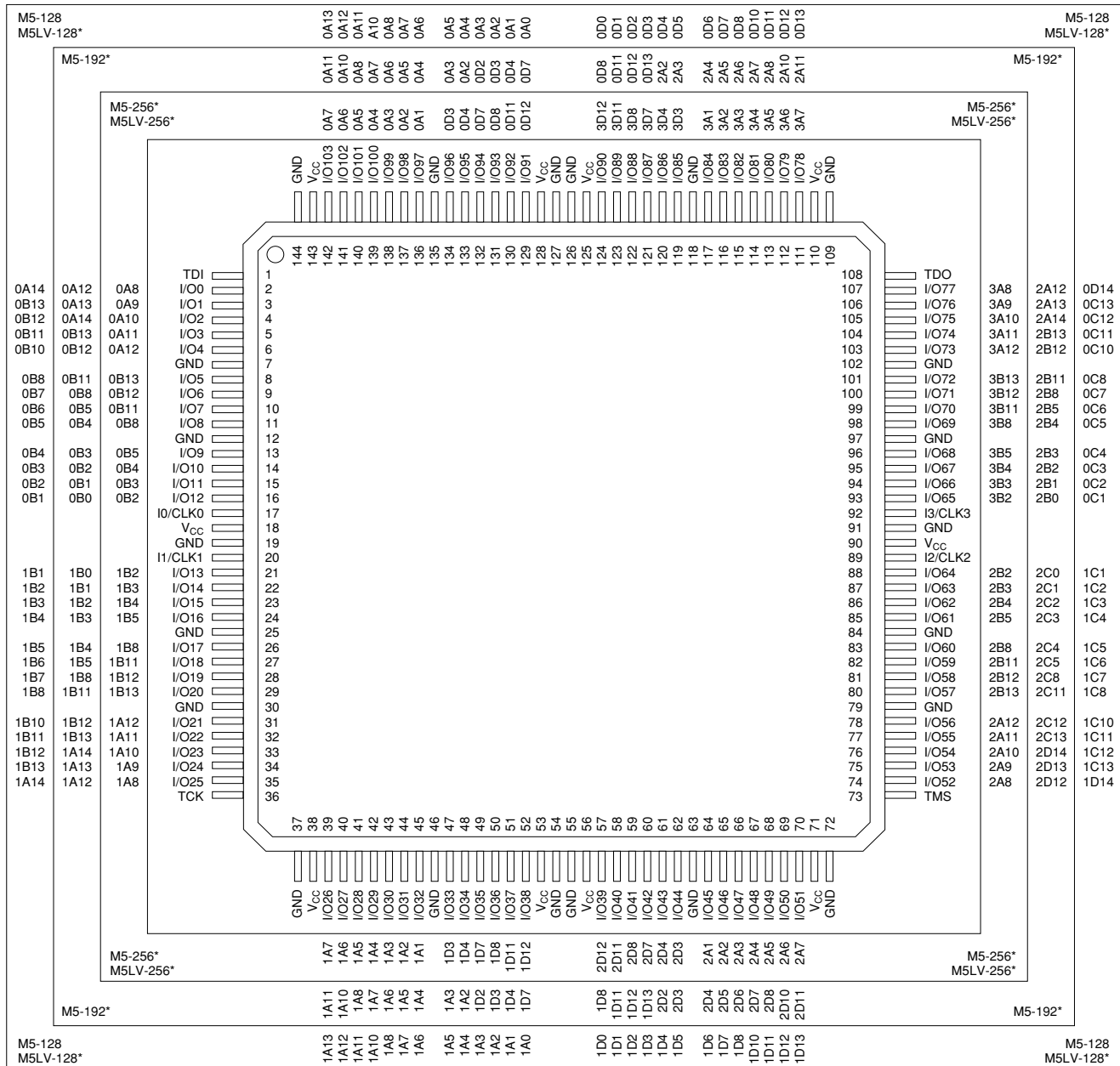
|                 |   |                  |
|-----------------|---|------------------|
| V <sub>CC</sub> | = | Supply Voltage   |
| TDI             | = | Test Data In     |
| TCK             | = | Test Clock       |
| TMS             | = | Test Mode Select |
| TDO             | = | Test Data Out    |



# 144-PIN PQFP CONNECTION DIAGRAM

## Top View

144-Pin PQFP



Select devices have been discontinued.  
See Ordering Information section for product status.

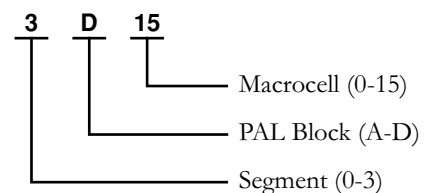
\*Package obsolete, contact factory.

20446G-019

### Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out

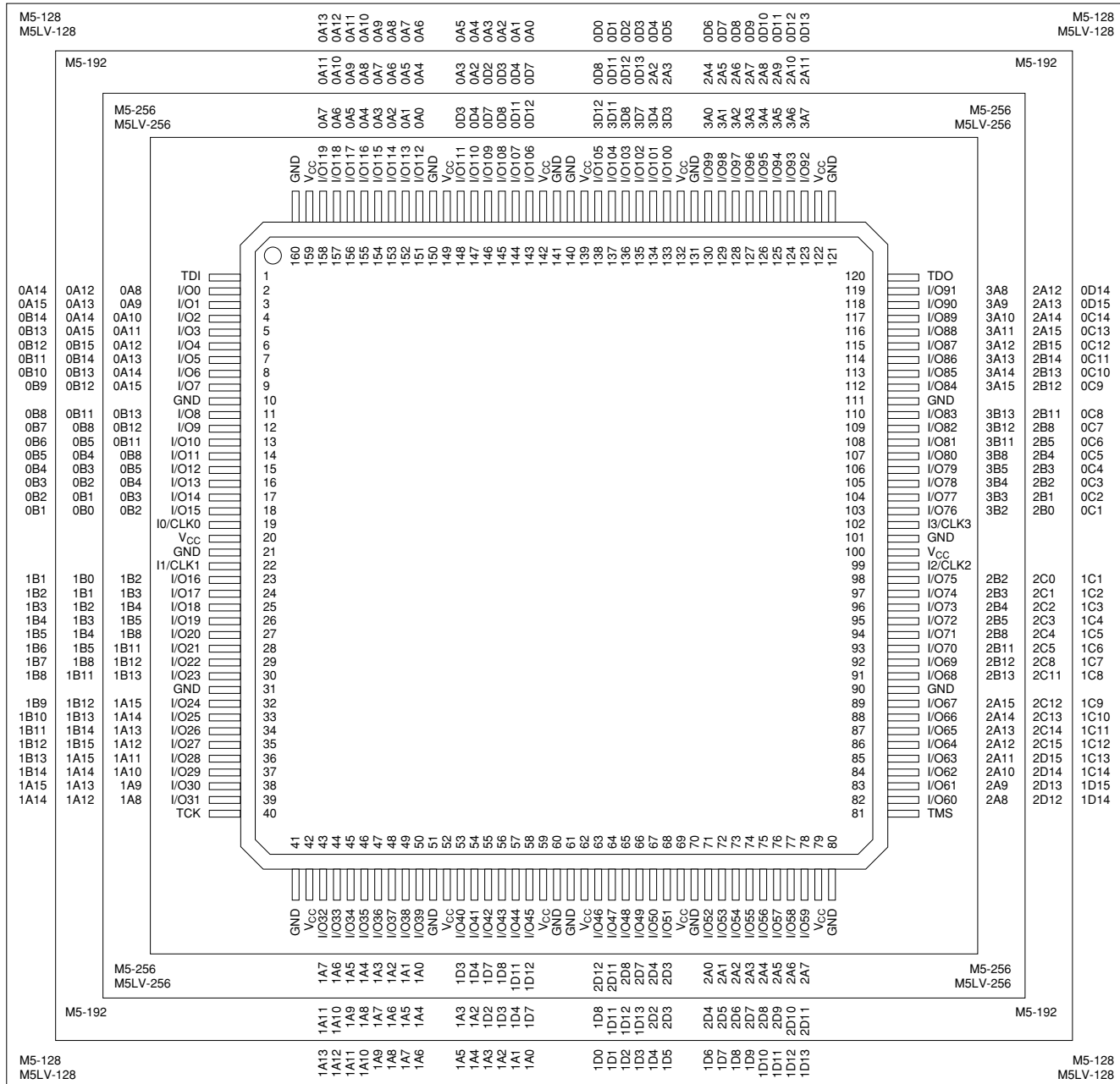


# 160-PIN PQFP CONNECTION DIAGRAM

## Top View

### 160-Pin PQFP (128, 192, 256 Macrocells)

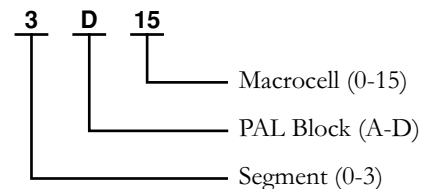
Select devices have been discontinued.  
See Ordering Information section for product status.



### Pin Designations

CLK = Clock  
GND = Ground  
I = Input  
I/O = Input/Output  
NC = No Connect

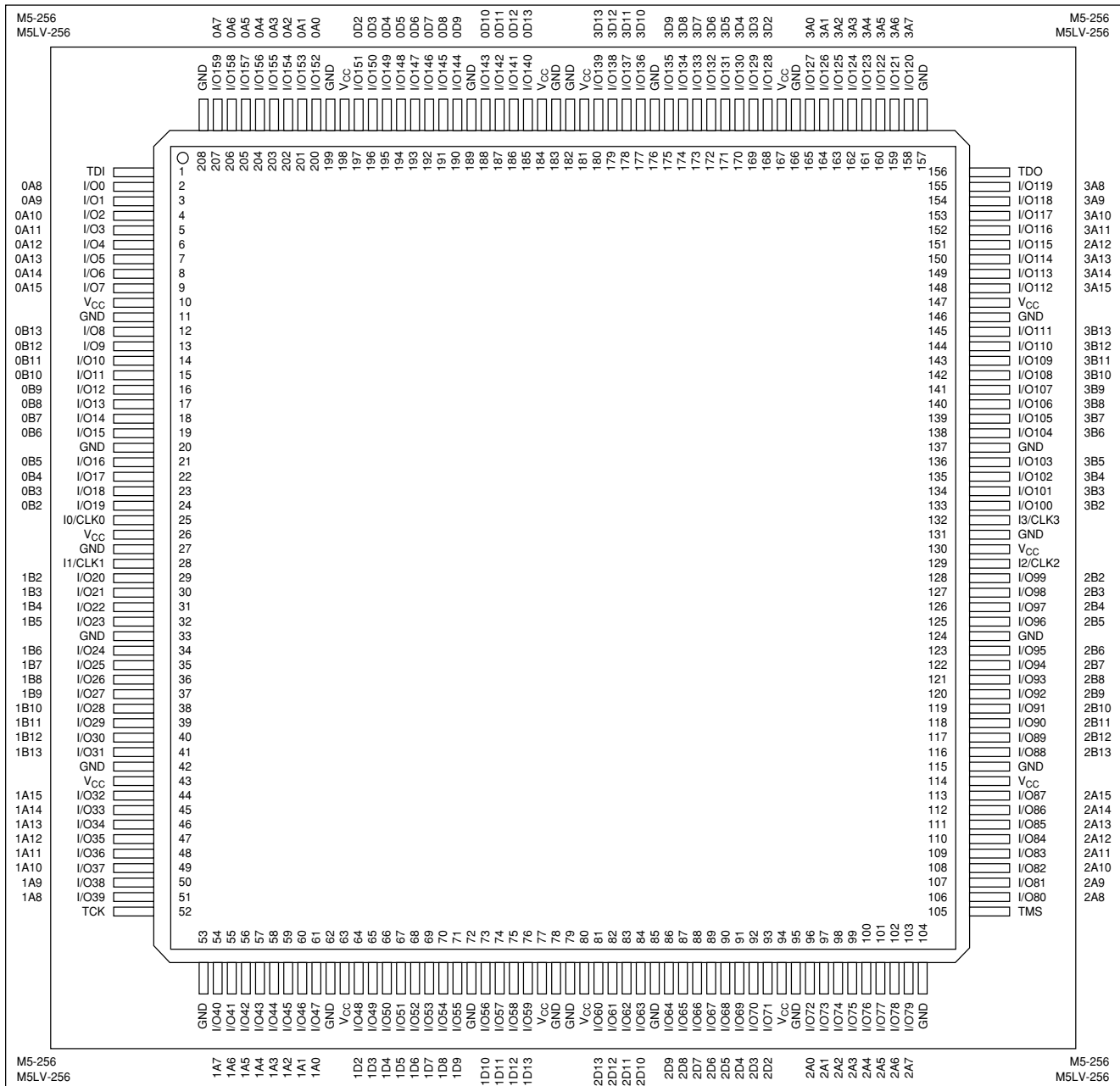
V<sub>CC</sub> = Supply Voltage  
TDI = Test Data In  
TCK = Test Clock  
TMS = Test Mode Select  
TDO = Test Data Out



## 208-PIN PQFP CONNECTION DIAGRAM

### Top View

208-Pin PQFP (256 Macrocells)



Select devices have been discontinued.  
See Ordering Information section for product status.

20446G-023

# 256-BALL BGA CONNECTION DIAGRAM — M5-320

## Bottom View (Macrocell Association)

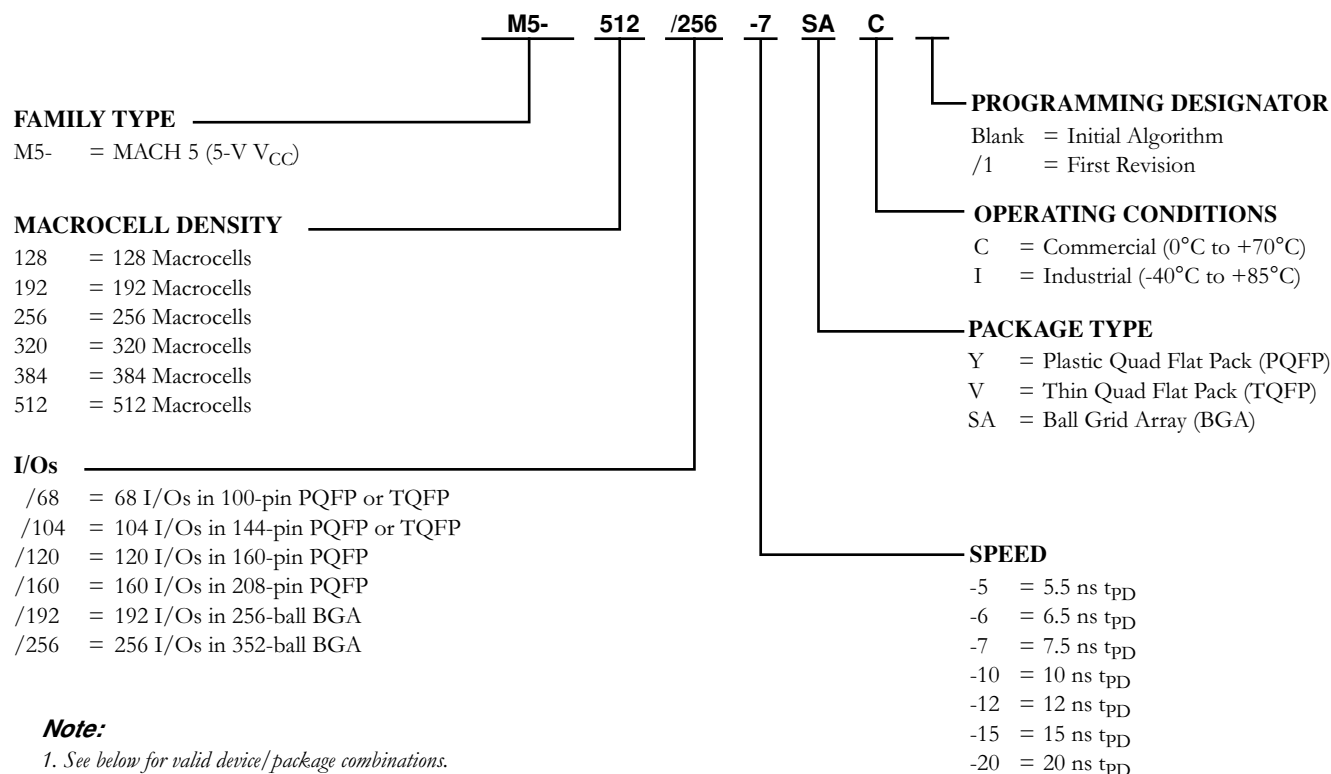
256-Ball BGA

|    | A    | B    | C               | D               | E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | F    | G               | H    | J   | K       | L       | M   | N    | P               | R    | T    | U               | V               | W    | Y    |     |   |
|----|------|------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------|------|-----|---------|---------|-----|------|-----------------|------|------|-----------------|-----------------|------|------|-----|---|
| 1  | GND  | GND  | 3A11            | 3D15            | 3D12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | GND  | 3D7             | GND  | 3D3 | 3D2     | GND     | 2D2 | GND  | 2D7             | GND  | 2D10 | 2D13            | 2D15            | GND  | GND  | 1   |   |
| 2  | GND  | 3B2  | 3A3             | 3A8             | 3A13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 3D13 | 3D9             | 3D8  | 3D4 | I3/CLK3 | I2/CLK2 | 2D3 | 2D4  | 2D8             | 2D12 | 2A15 | 2A13            | 2A12            | 2A9  | 2A7  | 2   |   |
| 3  | GND  | 3B8  | V <sub>CC</sub> | 3A2             | 3A4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 3A12 | 3D14            | 3D10 | 3D5 | 3D0     | 2D0     | 2D5 | 2D9  | 2D14            | 2A14 | 2A10 | 2A8             | V <sub>CC</sub> | 2A3  | GND  | 3   |   |
| 4  | 3B13 | 3B11 | 3B3             | V <sub>CC</sub> | TDO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 3A7  | V <sub>CC</sub> | 3D11 | 3D6 | 3D1     | 2D1     | 2D6 | 2D11 | V <sub>CC</sub> | 2A11 | TMS  | V <sub>CC</sub> | 2A6             | 2A2  | 2A0  | 4   |   |
| 5  | 4B14 | 4B15 | 3B4             | V <sub>CC</sub> | <div>Pin Designations</div> <div>CLK = Clock</div> <div>GND = Ground</div> <div>I = Input</div> <div>I/O = Input/Output</div> <div>NC = No Connect</div> <div>V<sub>CC</sub> = Supply Voltage</div> <div>TDI = Test Data In</div> <div>TCK = Test Clock</div> <div>TMS = Test Mode Select</div> <div>TDO = Test Data Out</div> <div><div><div>4</div><div>D</div><div>15</div></div><div>Macrocell (0-15)</div><div>PAL Block (A-D)</div><div>Segment (0-4)</div></div> <td>V<sub>CC</sub></td> <td>2A4</td> <td>2A1</td> <td>2B0</td> <td>2B1</td> <td>5</td> |      |                 |      |     |         |         |     |      |                 |      |      | V <sub>CC</sub> | 2A4             | 2A1  | 2B0  | 2B1 | 5 |
| 6  | GND  | 4B11 | 3B12            | 3B7             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | V <sub>CC</sub> | 2A1             | 2B4  | GND  | 6   |   |
| 7  | 4B8  | 4B10 | 4B13            | V <sub>CC</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | V <sub>CC</sub> | 2B2             | 2B5  | 2B7  | 7   |   |
| 8  | 4B4  | 4B6  | 4B9             | 4B12            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 2B3             | 2B6             | 2B9  | 2B11 | 8   |   |
| 9  | GND  | 4B3  | 4B5             | 4B7             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 2B8             | 2B10            | 2B12 | GND  | 9   |   |
| 10 | GND  | 4B0  | 4B1             | 4B2             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 2B13            | 2B14            | 2B15 | GND  | 10  |   |
| 11 | GND  | 4A0  | 4A1             | 4A2             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 1B13            | 1B14            | 1B15 | GND  | 11  |   |
| 12 | GND  | 4A3  | 4A5             | 4A7             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 1B8             | 1B10            | 1B12 | GND  | 12  |   |
| 13 | 4A4  | 4A6  | 4A9             | 4A12            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 1B3             | 1B6             | 1B9  | 1B11 | 13  |   |
| 14 | 4A8  | 4A10 | 4A13            | V <sub>CC</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | V <sub>CC</sub> | 1B2             | 1B5  | 1B7  | 14  |   |
| 15 | GND  | 4A11 | 0B12            | 0B7             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | 1A4             | 1A1             | 1B4  | GND  | 15  |   |
| 16 | 4A14 | 4A15 | 0B4             | V <sub>CC</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |                 |      |     |         |         |     |      |                 |      |      | V <sub>CC</sub> | 1A5             | 1B0  | 1B1  | 16  |   |
| 17 | 0B13 | 0B11 | 0B3             | V <sub>CC</sub> | TDI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0A7  | V <sub>CC</sub> | 0D11 | 0D6 | 0D1     | 1D1     | 1D6 | 1D11 | V <sub>CC</sub> | 1A11 | TCK  | V <sub>CC</sub> | 1A6             | 1A2  | 1A0  | 17  |   |
| 18 | GND  | 0B8  | V <sub>CC</sub> | 0A2             | 0A4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0A12 | 0D14            | 0D9  | 0D5 | 0D0     | 1D0     | 1D5 | 1D10 | 1D14            | 1A14 | 1A10 | 1A8             | V <sub>CC</sub> | 1A3  | GND  | 18  |   |
| 19 | 0B2  | 0A3  | 0A8             | 0A11            | 0A13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0D12 | 0D8             | 0D4  | 0D3 | I0/CLK0 | I1/CLK1 | 1D4 | 1D8  | 1D9             | 1D13 | 1A15 | 1A12            | 1A9             | 1A7  | GND  | 19  |   |
| 20 | GND  | GND  | 0D15            | 0D13            | 0D10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | GND  | 0D7             | GND  | 0D2 | GND     | 1D2     | 1D3 | GND  | 1D7             | GND  | 1D12 | 1D15            | 1A13            | GND  | GND  | 20  |   |

Select devices have been discontinued.  
See Ordering Information section for product status.

## 5V M5 ORDERING INFORMATION<sup>1,2</sup>

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



### Note:

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

| Valid Combinations |                                                                               |                                   |
|--------------------|-------------------------------------------------------------------------------|-----------------------------------|
| M5-128/68          | Commercial:<br>-5, -7, -10, -12, -15<br>Industrial:<br>-7, -10, -12, -15, -20 | YC, VC, YI, VI                    |
| M5-128/104         |                                                                               | YC <sup>1</sup> , YI <sup>1</sup> |
| M5-128/120         |                                                                               | YC, YI                            |
| M5-192/68          |                                                                               | VC, VI                            |
| M5-192/120         |                                                                               | YC, YI                            |
| M5-256/68          |                                                                               | VC, VI                            |
| M5-256/120         |                                                                               | YC, YI                            |
| M5-256/160         |                                                                               | YC, YI                            |

### Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

| Valid Combinations |                                       |          |
|--------------------|---------------------------------------|----------|
| M5-320/160         | Commercial:<br>-6, -7, -10, -12, -15  | YC, YI   |
| M5-320/192         |                                       | SAC, SAI |
| M5-384/160         |                                       | YC, YI   |
| M5-512/160         | Industrial:<br>-7, -10, -12, -15, -20 | YC, YI   |
| M5-512/256         |                                       | SAC, SAI |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.  
See Ordering Information section for product status.