# Lattice Semiconductor Corporation - M5LV-256/104-12VC Datasheet

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 12 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 104 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-256-104-12vc |

Table 1. MACH 5 Device Features [1]

| Feature | M5-128/1 M5LV-128 | | M5-192/1 | M5-256/1 M5LV-256 | | M5-320 M5LV-320 | | M5-384 M5LV-384 | | M5-512 M5LV-512 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage (V) | 5 | 3.3 | 5 | 5 | 3.3 | 5 | 3.3 | 5 | 3.3 | 5 | 3.3 |
| Macrocells | 128 | 128 | 192 | 256 | 256 | 320 | 320 | 384 | 384 | 512 | 512 |
| Maximum User I/O Pins | 120 | 120 | 120 | 160 | 160 | 192 | 160 | 160 | 160 | 256 | 256 |
| $t_{PD}$ (ns) | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | 6.5 | 6.5 | 6.5 | 6.5 | 6.5 | 6.5 |
| $t_{SS}$ (ns) | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 |
| $t_{COS}$ (ns) | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 |
| $f_{CNT}$ (MHz) | 182 | 182 | 182 | 182 | 182 | 167 | 167 | 167 | 167 | 167 | 167 |
| Typical Static Power (mA) | 35 | 35 | 45 | 55 | 55 | 70 | 70 | 75 | 75 | 100 | 100 |
| IEEE 1149.1 Boundary Scan Compliant | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PCI-Compliant | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

***Note:***

1. *"M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.*

## GENERAL DESCRIPTION

The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on $E^2$CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.
See Ordering Information section for product status.

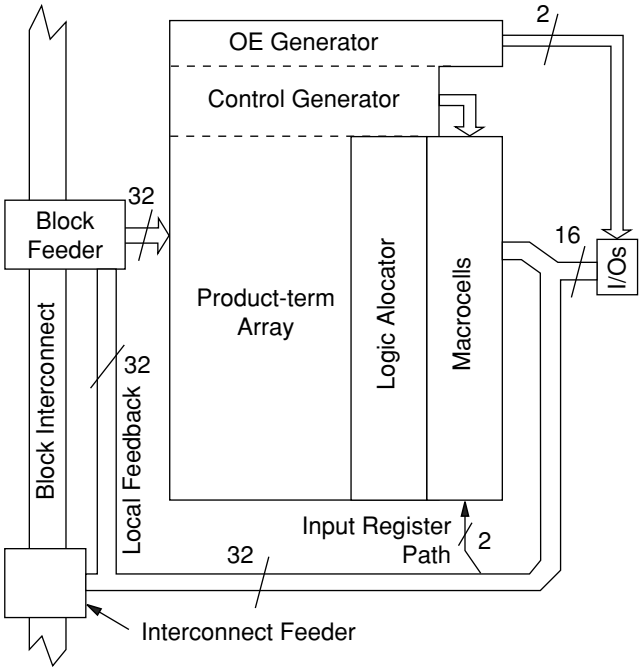


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**Figure 2. PAL Block Structure**

## Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 of 4 product terms.

**Logic allocators** assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

**Table 4. Product Term Steering Options for PT Clusters and Macrocells**

| Macrocell | Available Clusters | Macrocell | Available Clusters |
|---|---|---|---|
| $M_0$ | $C_0, C_1, C_2, C_3, C_4$ | $M_8$ | $C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}$ |
| $M_1$ | $C_0, C_1, C_2, C_3, C_4, C_5$ | $M_9$ | $C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}$ |
| $M_2$ | $C_0, C_1, C_2, C_3, C_4, C_5, C_6$ | $M_{10}$ | $C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}$ |
| $M_3$ | $C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ | $M_{11}$ | $C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$ |
| $M_4$ | $C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ | $M_{12}$ | $C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$ |
| $M_5$ | $C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8$ | $M_{13}$ | $C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$ |
| $M_6$ | $C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9$ | $M_{14}$ | $C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$ |
| $M_7$ | $C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}$ | $M_{15}$ | $C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$ |

Select devices have been discontinued.
See Ordering Information section for product status.

- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

**Clock Line 2 Options**

- Global clock (0, 1, 2, or 3) with clock enable

**Clock Line 3 Options**

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable

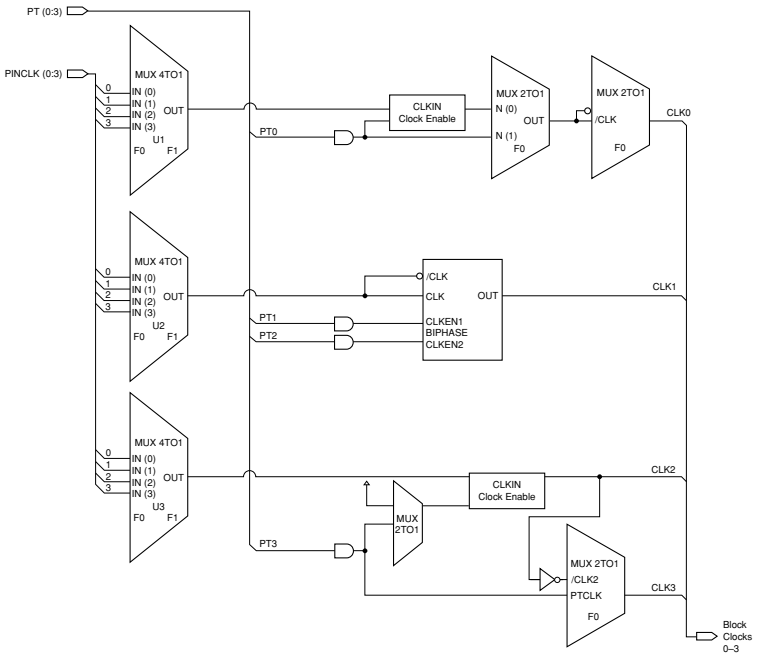


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**Figure 4. Clock Generator**

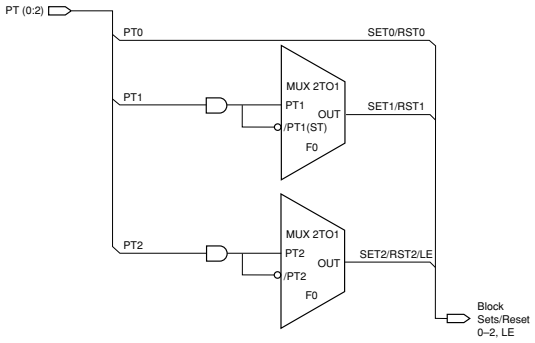


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**Figure 5. Set/Reset Generator**

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

Select devices have been discontinued.
See Ordering Information section for product status.

## MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

## IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

## IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

## PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above $V_{CC}$ because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

**Select devices have been discontinued.**
**See Ordering Information section for product status.**

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS [1]

Both the 3.3-V and 5-V $V_{CC}$ MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

***Note:***

1. *Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".*

## BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

**Table 5. Power Levels**

| | |
|---|---|
| High Speed/High Power | 100% Power |
| Medium High Speed/Medium High Power | 67% Power |
| Medium Low Speed/Medium Low Power | 40% Power |
| Low Speed/Low Power | 20% Power |

## PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the $V_{CC}$ rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

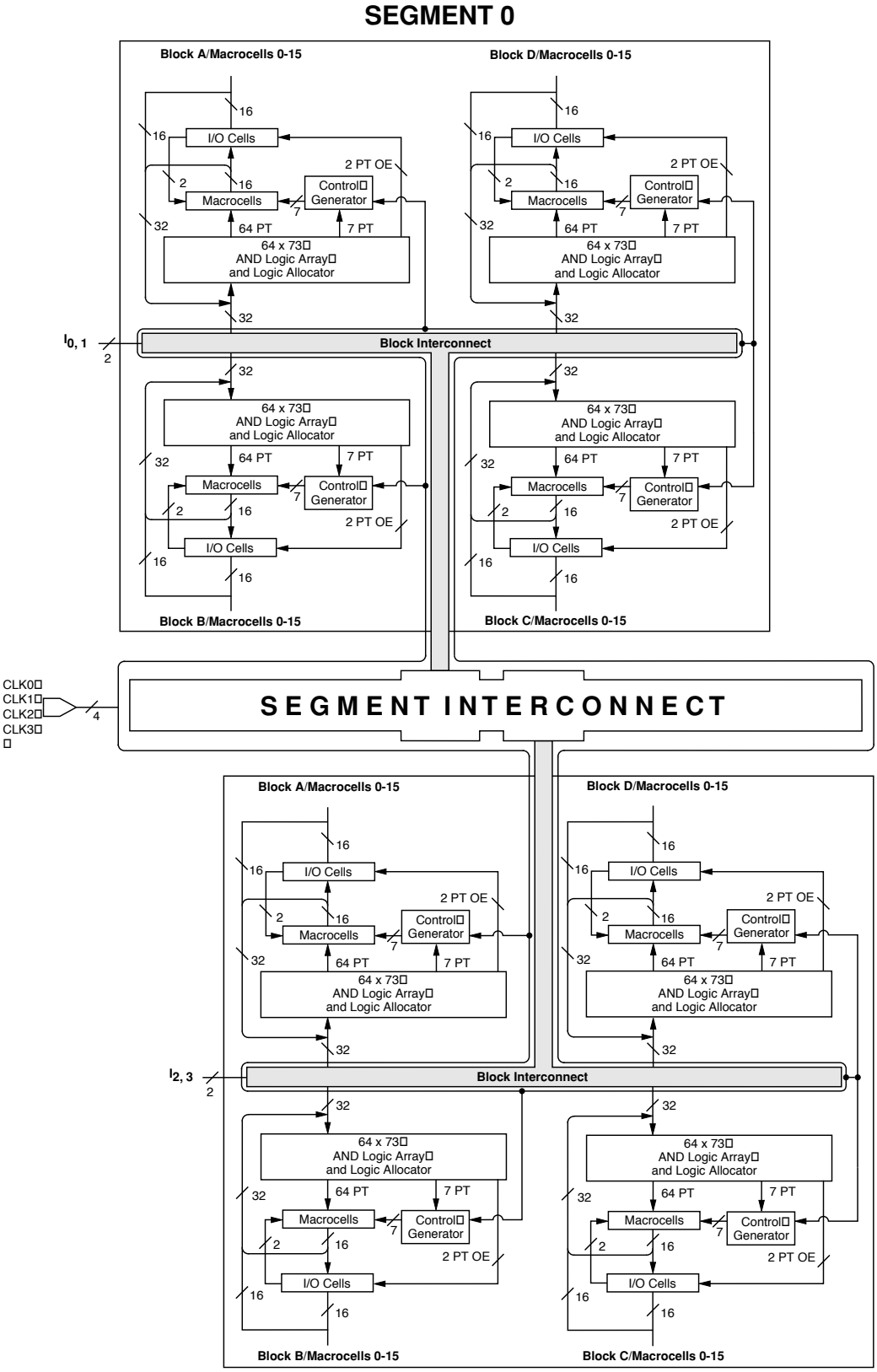
Select devices have been discontinued.
See Ordering Information section for product status.

## SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Select devices have been discontinued.
See Ordering Information section for product status.

## BLOCK DIAGRAM — M5(LV)-128/XXX

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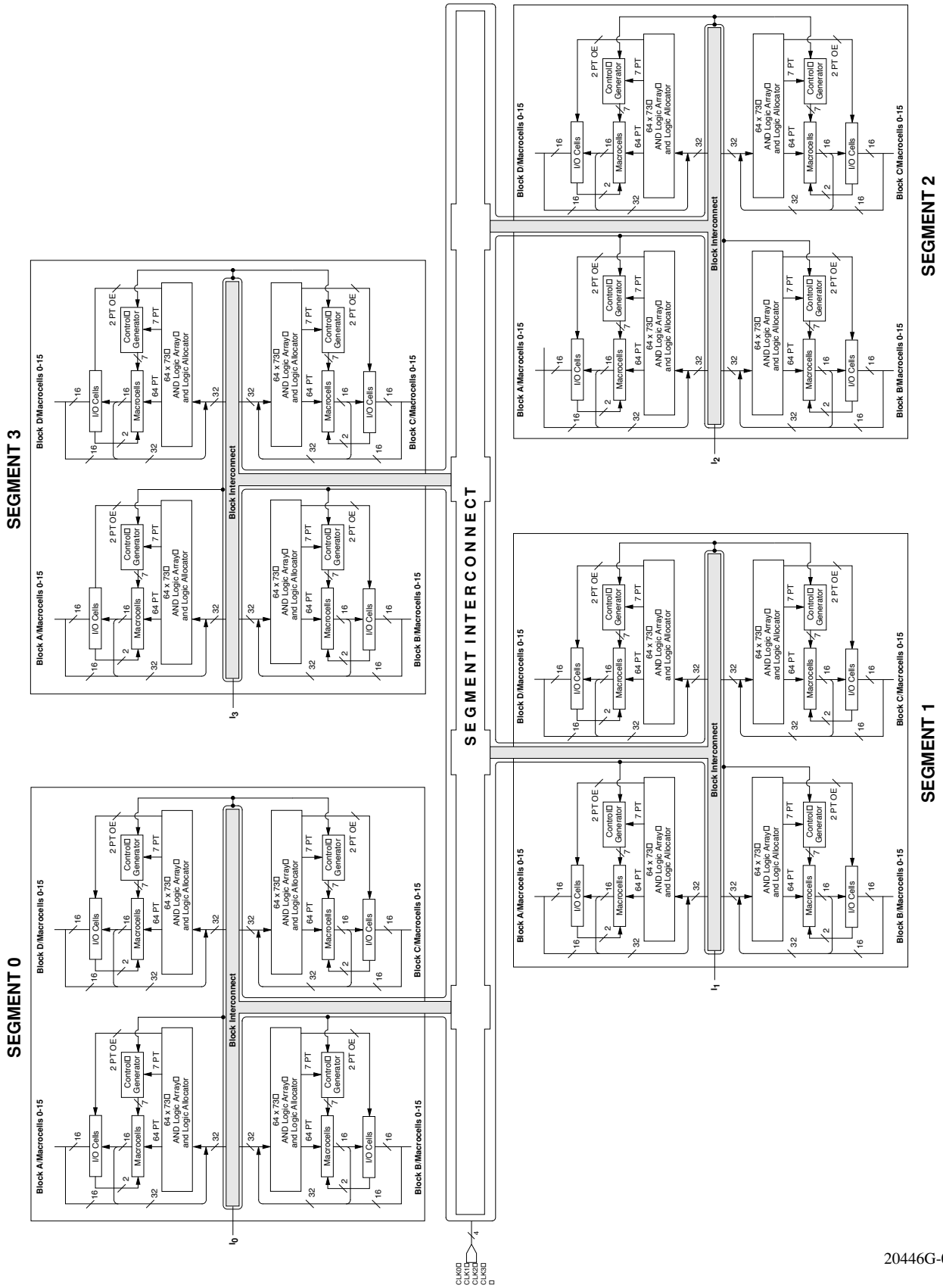
**Select devices have been discontinued.**
**See Ordering Information section for product status.**

## BLOCK DIAGRAM — M5(LV)-256/XXX

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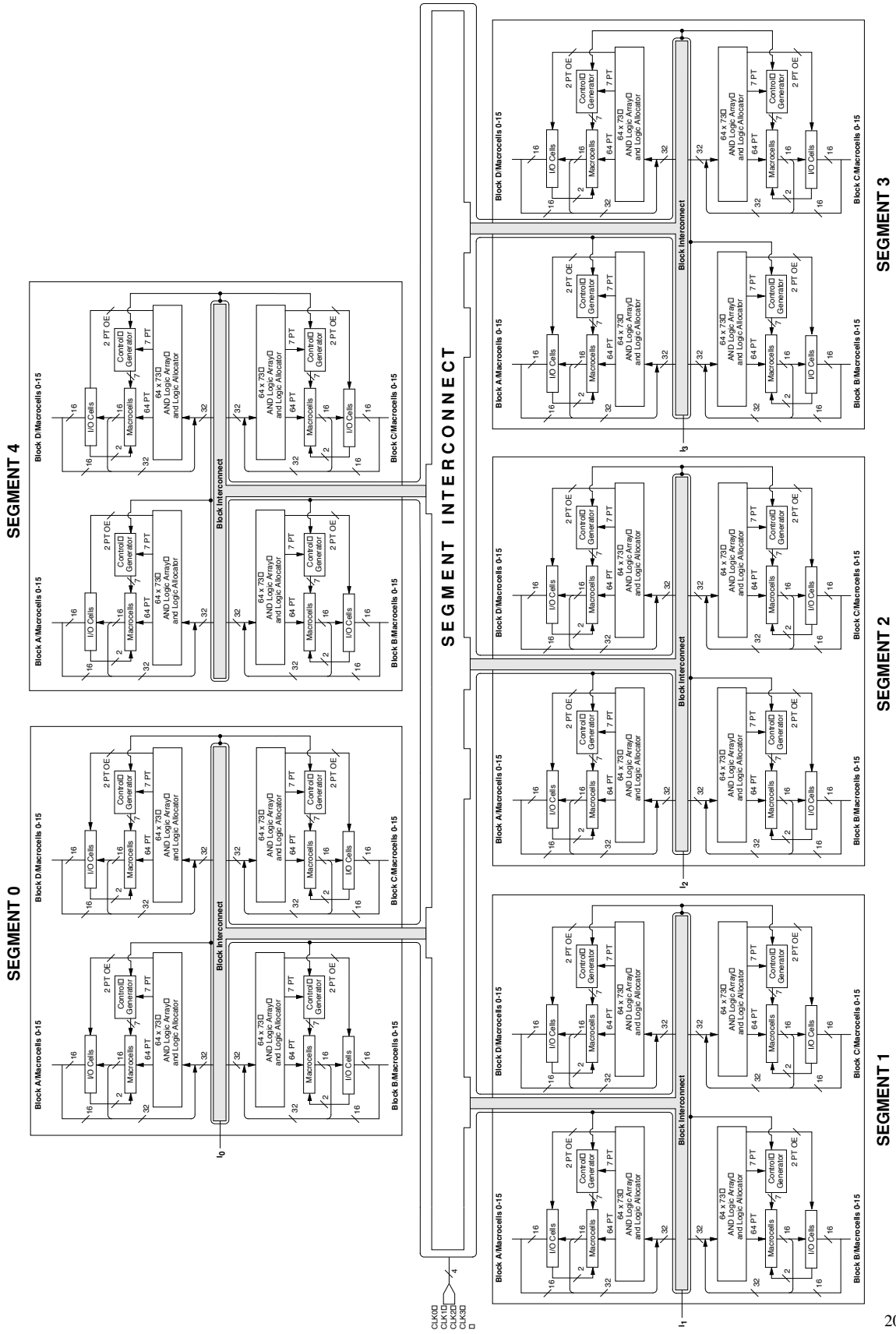
**See Ordering Information section for product status.**

# BLOCK DIAGRAM — M5(LV)-320/XXX

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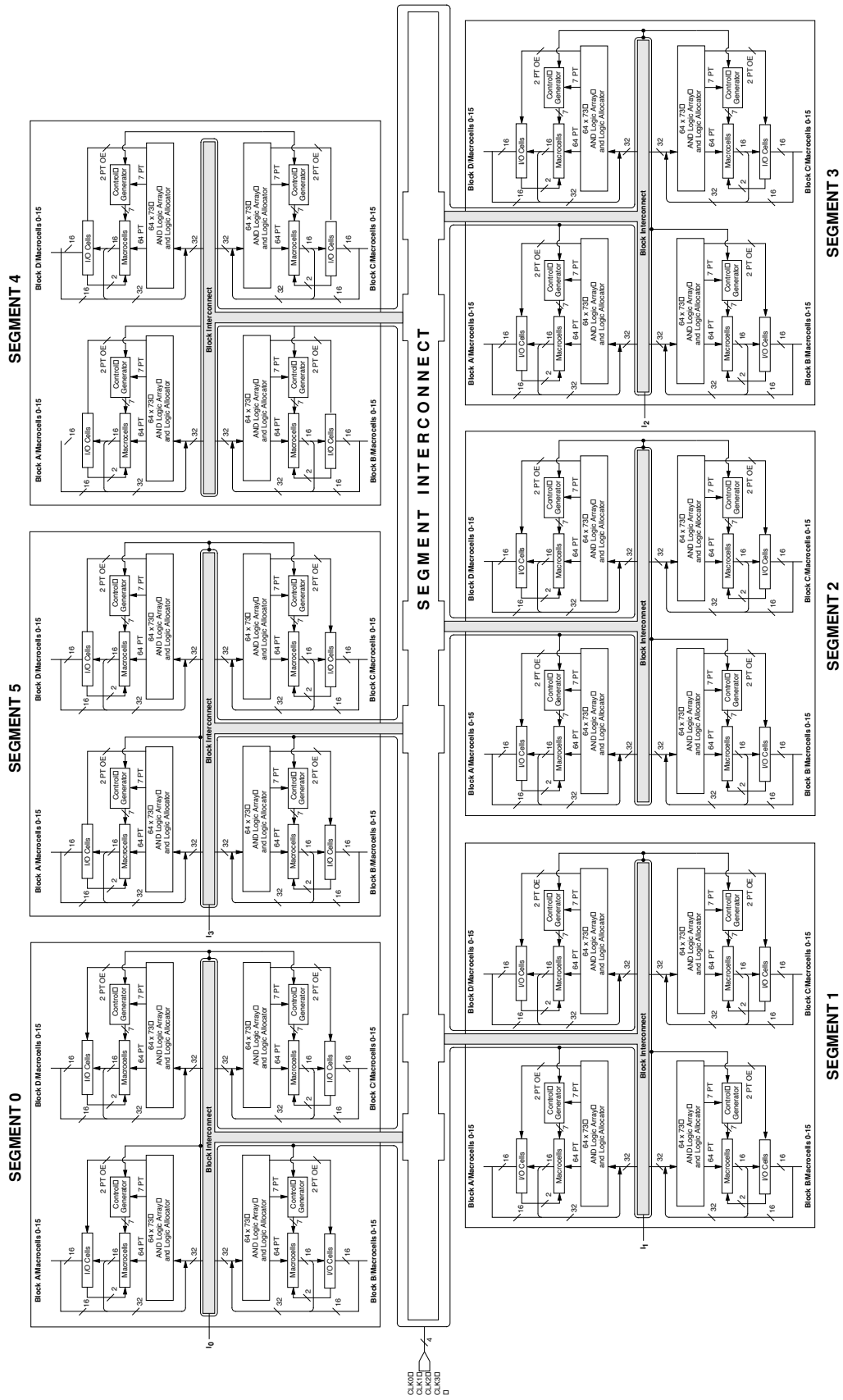
**Select devices have been discontinued.**
**See Ordering Information section for product status.**

## BLOCK DIAGRAM — M5(LV)-384/XXX

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**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# BLOCK DIAGRAM — M5(LV)-512/XXX

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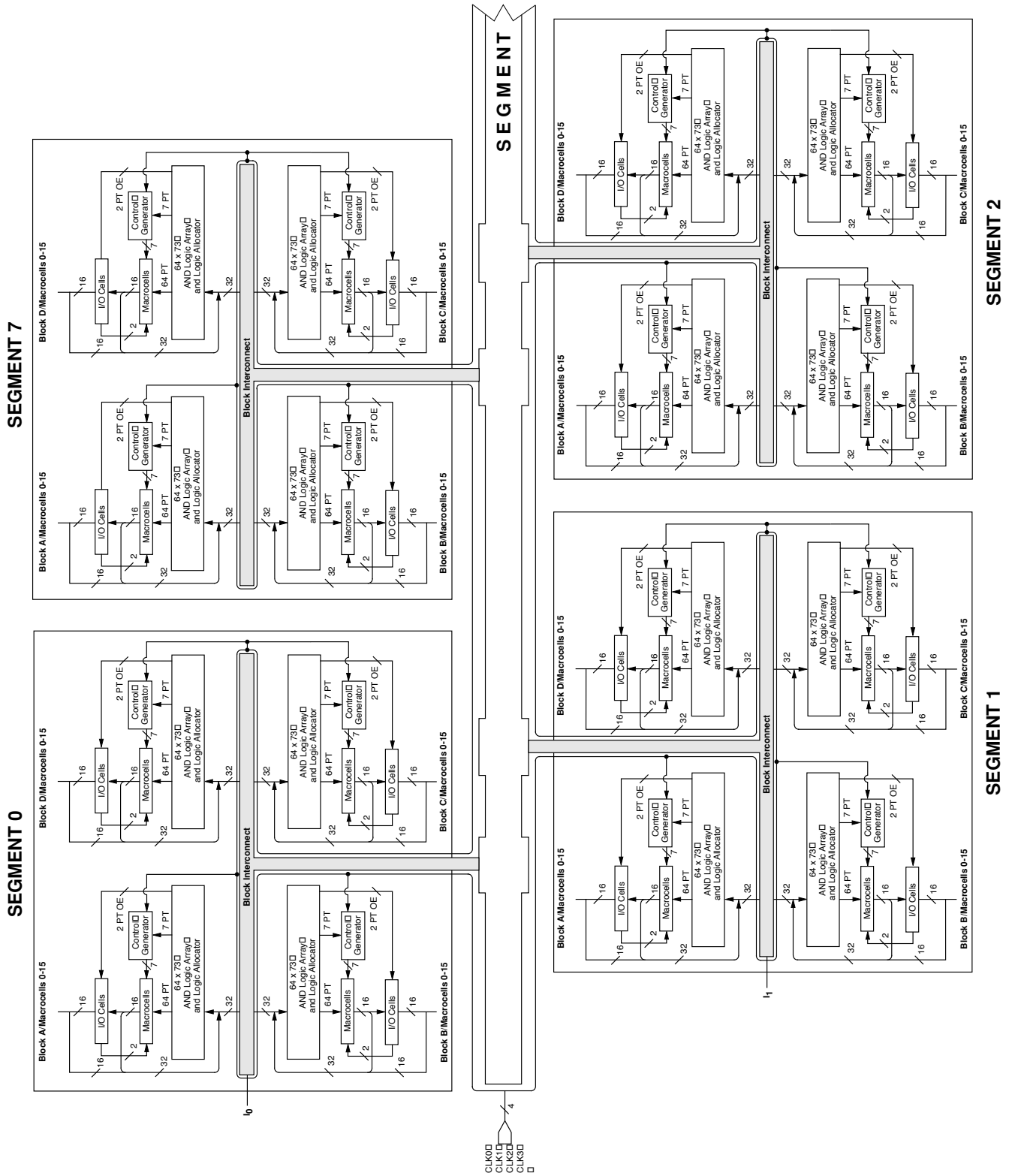


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**Select devices have been discontinued.**
**See Ordering Information section for product status.**

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1]

| | | -5 | | -6 | | -7 | | -10 | | -12 | | -15 | | -20 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Unit |
| **Combinatorial Delay:** | | | | | | | | | | | | | | | | |
| $t_{PDi}$ | Internal combinatorial propagation delay | | 3.5 | | 4.5 | | 5.5 | | 8.0 | | 10.0 | | 13.0 | | 18.0 | ns |
| $t_{PD}$ | Combinatorial propagation delay | | 5.5 | | 6.5 | | 7.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |
| **Registered Delays:** | | | | | | | | | | | | | | | | |
| $t_{SS}$ | Synchronous clock setup time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 8.0 | | 10.0 | | ns |
| $t_{SA}$ | Asynchronous clock setup time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{HS}$ | Synchronous clock hold time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HA}$ | Asynchronous clock hold time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{COSi}$ | Synchronous clock to internal output | | 2.5 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 8.0 | | 10.0 | ns |
| $t_{COS}$ | Synchronous clock to output | | 4.5 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | 10.0 | | 12.0 | ns |
| $t_{COAi}$ | Asynchronous clock to internal output | | 6.0 | | 6.0 | | 8.0 | | 10.0 | | 13.0 | | 15.0 | | 18.0 | ns |
| $t_{COA}$ | Asynchronous clock to output | | 8.0 | | 8.0 | | 10.0 | | 12.0 | | 15.0 | | 17.0 | | 20.0 | ns |
| **Latched Delays:** | | | | | | | | | | | | | | | | |
| $t_{SAL}$ | Latch setup time | 3.0 | | 4.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{HAL}$ | Latch hold time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{PDLi}$ | Transparent latch internal | | 6.0 | | 7.0 | | 7.0 | | 8.0 | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{PDL}$ | Propagation delay through transparent latch | | 8.0 | | 9.0 | | 9.0 | | 10.0 | | 11.0 | | 12.0 | | 12.0 | ns |
| $t_{GOAi}$ | Gate to internal output | | 7.0 | | 8.0 | | 8.0 | | 9.0 | | 10.0 | | 11.0 | | 12.0 | ns |
| $t_{GOA}$ | Gate to output | | 9.0 | | 10.0 | | 10.0 | | 11.0 | | 12.0 | | 13.0 | | 14.0 | ns |
| **Input Register Delays:** | | | | | | | | | | | | | | | | |
| $t_{SIRS}$ | Input register setup time using a synchronous clock | 2.0 | | 2.0 | | 2.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{SIRA}$ | Input register setup time using an asynchronous clock | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HIRS}$ | Input register hold time using a synchronous clock | 3.0 | | 3.0 | | 3.0 | | 4.0 | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{HIRA}$ | Input register hold time using an asynchronous clock | 6.0 | | 6.0 | | 6.0 | | 7.0 | | 7.0 | | 7.0 | | 7.0 | | ns |
| **Input Latch Delays:** | | | | | | | | | | | | | | | | |
| $t_{SIL}$ | Input latch setup time | 2.0 | | 2.0 | | 2.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{HIL}$ | Input latch hold time | 6.0 | | 6.0 | | 6.0 | | 7.0 | | 7.0 | | 7.0 | | 7.0 | | ns |
| $t_{PDILi}$ | Transparent input latch | | 5.0 | | 5.0 | | 5.5 | | 6.0 | | 6.0 | | 6.0 | | 6.0 | ns |
| **Output Delays:** | | | | | | | | | | | | | | | | |
| $t_{BUF}$ | Output buffer delay | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | ns |
| $t_{SLW}$ | Slow slew rate delay | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | ns |
| $t_{EA}$ | Output enable time | | 7.5 | | 7.5 | | 9.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |
| $t_{ER}$ | Output disable time | | 7.5 | | 7.5 | | 9.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |

Select devices have been discontinued.
See Ordering Information section for product status.

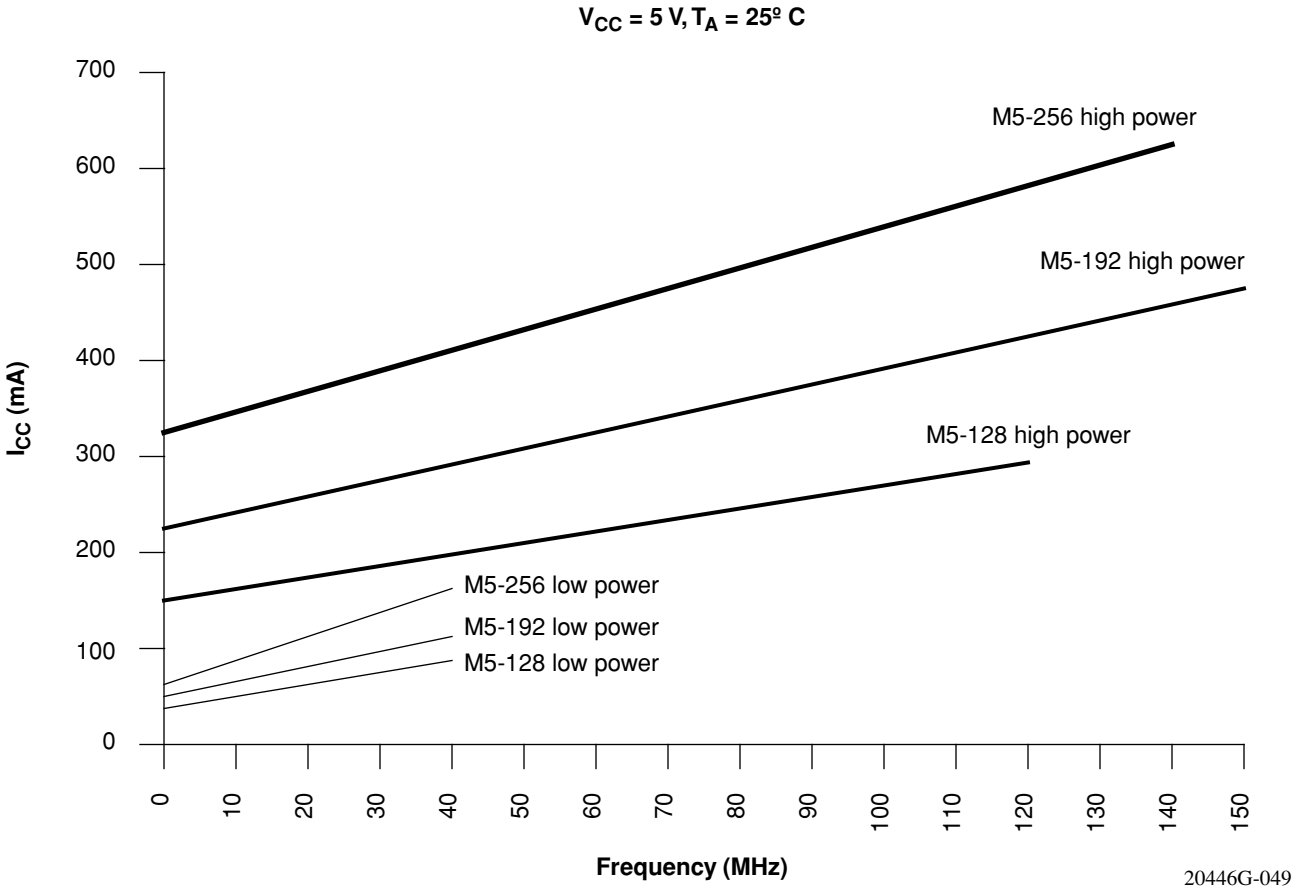


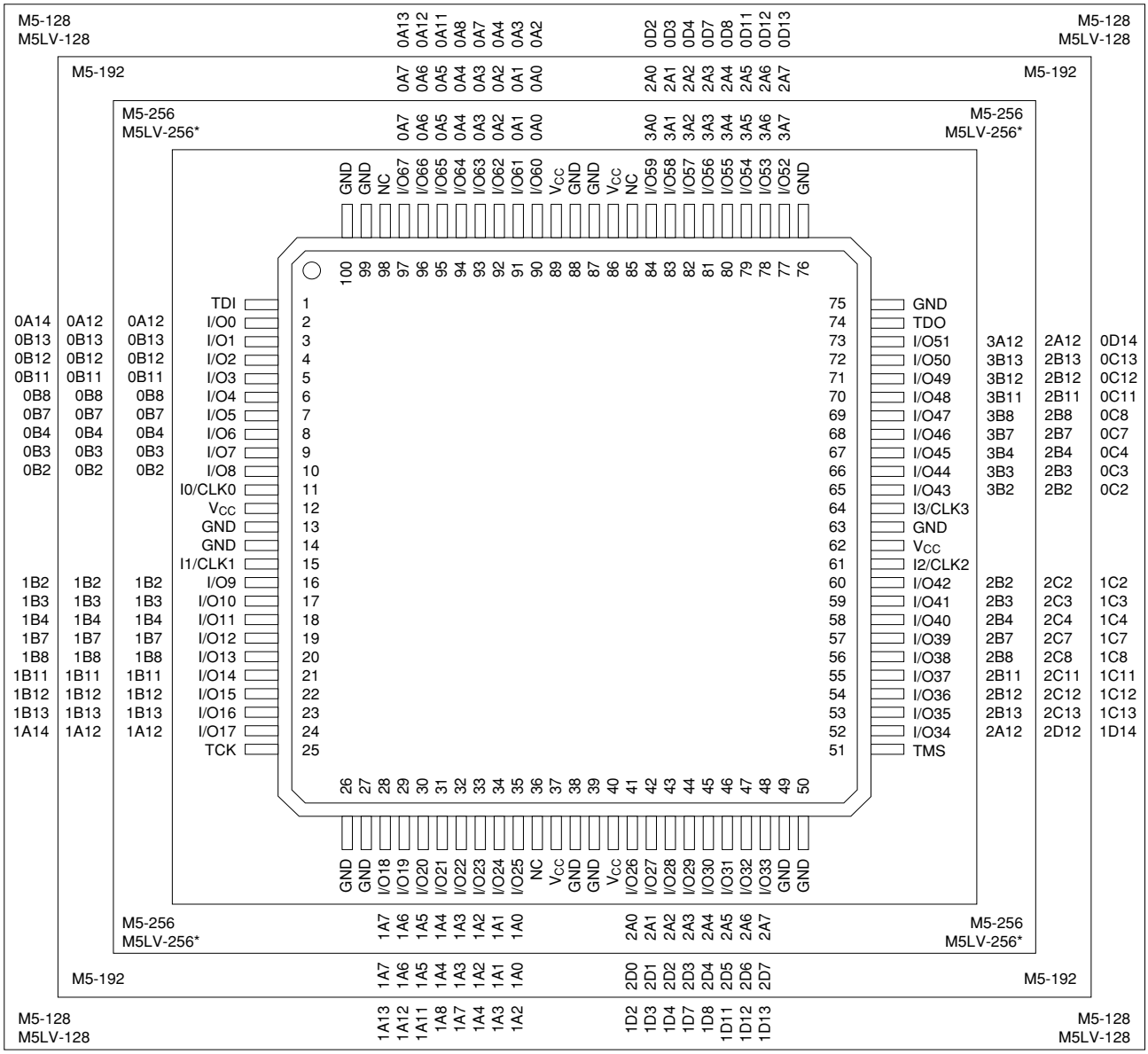

**Figure 9. $I_{CC}$ Curves at High/Low Power Modes**

Select devices have been discontinued.
See Ordering Information section for product status.

# 100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

## Top View

**100-Pin TQFP (68 I/O)**




*Package obsolete, contact factory.

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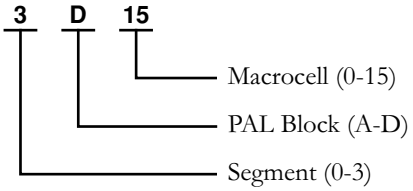
### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |

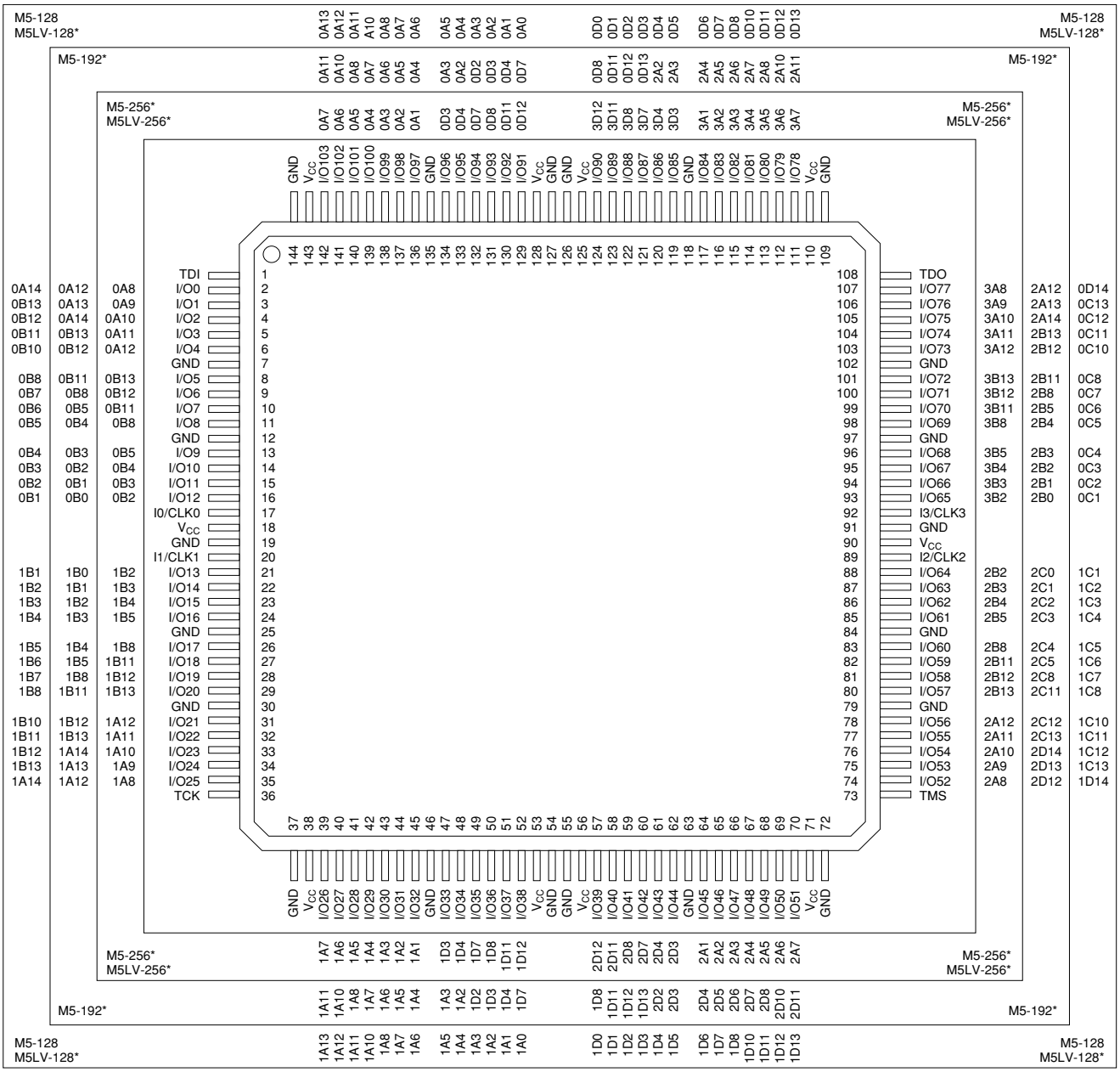



**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# 144-PIN PQFP CONNECTION DIAGRAM

## Top View

**144-Pin PQFP**

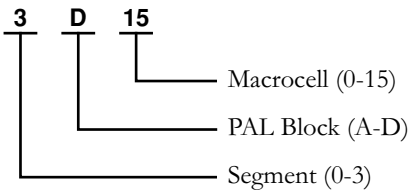



*Package obsolete, contact factory.

20446G-019

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |

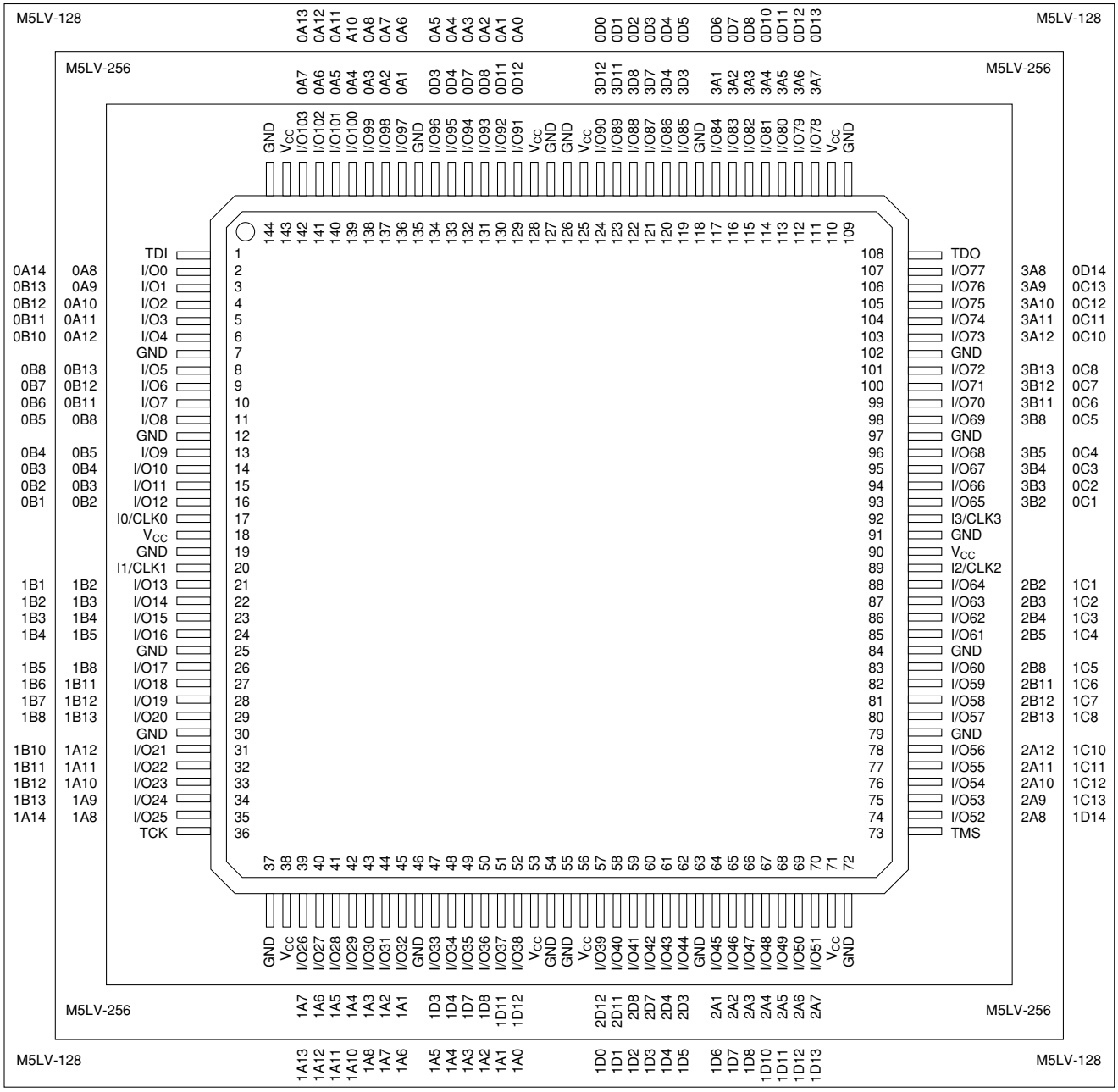



**Select devices have been discontinued. See Ordering Information section for product status.**

# 144-PIN TQFP CONNECTION DIAGRAM

## Top View

**144-Pin TQFP**

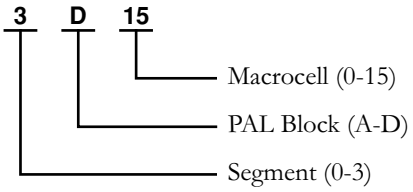



20446G-020

**Select devices have been discontinued. See Ordering Information section for product status.**

### Pin Designations

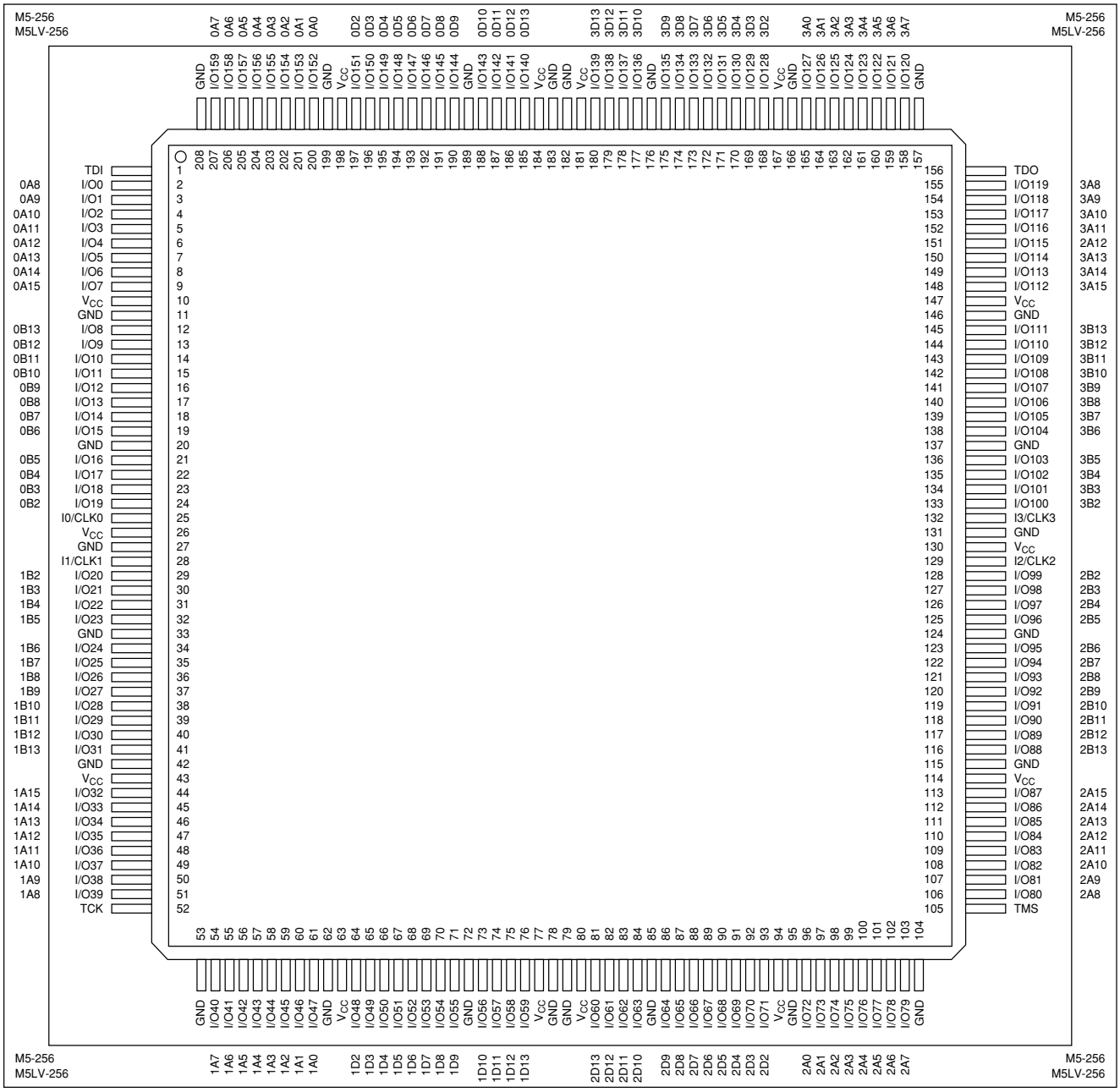
| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |



# 208-PIN PQFP CONNECTION DIAGRAM

## Top View

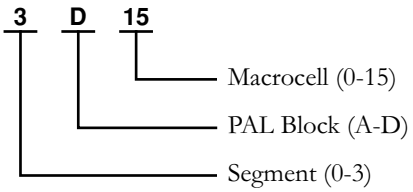
**208-Pin PQFP (256 Macrocells)**




20446G-023

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |




**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# 256-BALL BGA CONNECTION DIAGRAM — M5-320

## Bottom View (Macrocell Association)

**256-Ball BGA**

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | 3A11 | 3D15 | 3D12 | GND | 3D7 | GND | 3D3 | 3D2 | GND | 2D2 | GND | 2D7 | GND | 2D10 | 2D13 | 2D15 | GND | GND |
| 2 | GND | 3B2 | 3A3 | 3A8 | 3A13 | 3D13 | 3D9 | 3D8 | 3D4 | I3/CLK3 | I2/CLK2 | 2D3 | 2D4 | 2D8 | 2D12 | 2A15 | 2A13 | 2A12 | 2A9 | 2A7 |
| 3 | GND | 3B8 | $V_{CC}$ | 3A2 | 3A4 | 3A12 | 3D14 | 3D10 | 3D5 | 3D0 | 2D0 | 2D5 | 2D9 | 2D14 | 2A14 | 2A10 | 2A8 | $V_{CC}$ | 2A3 | GND |
| 4 | 3B13 | 3B11 | 3B3 | $V_{CC}$ | TDO | 3A7 | $V_{CC}$ | 3D11 | 3D6 | 3D1 | 2D1 | 2D6 | 2D11 | $V_{CC}$ | 2A11 | TMS | $V_{CC}$ | 2A6 | 2A2 | 2A0 |
| 5 | 4B14 | 4B15 | 3B4 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 2A5 | 2B0 | 2B1 |
| 6 | GND | 4B11 | 3B12 | 3B7 | | | | | | | | | | | | | 2A4 | 2A1 | 2B4 | GND |
| 7 | 4B8 | 4B10 | 4B13 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 2B2 | 2B5 | 2B7 |
| 8 | 4B4 | 4B6 | 4B9 | 4B12 | | | | | | | | | | | | | 2B3 | 2B6 | 2B9 | 2B11 |
| 9 | GND | 4B3 | 4B5 | 4B7 | | | | | | | | | | | | | 2B8 | 2B10 | 2B12 | GND |
| 10 | GND | 4B0 | 4B1 | 4B2 | | | | | | | | | | | | | 2B13 | 2B14 | 2B15 | GND |
| 11 | GND | 4A0 | 4A1 | 4A2 | | | | | | | | | | | | | 1B13 | 1B14 | 1B15 | GND |
| 12 | GND | 4A3 | 4A5 | 4A7 | | | | | | | | | | | | | 1B8 | 1B10 | 1B12 | GND |
| 13 | 4A4 | 4A6 | 4A9 | 4A12 | | | | | | | | | | | | | 1B3 | 1B6 | 1B9 | 1B11 |
| 14 | 4A8 | 4A10 | 4A13 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 1B2 | 1B5 | 1B7 |
| 15 | GND | 4A11 | 0B12 | 0B7 | | | | | | | | | | | | | 1A4 | 1A1 | 1B4 | GND |
| 16 | 4A14 | 4A15 | 0B4 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 1A5 | 1B0 | 1B1 |
| 17 | 0B13 | 0B11 | 0B3 | $V_{CC}$ | TDI | 0A7 | $V_{CC}$ | 0D11 | 0D6 | 0D1 | 1D1 | 1D6 | 1D11 | $V_{CC}$ | 1A11 | TCK | $V_{CC}$ | 1A6 | 1A2 | 1A0 |
| 18 | GND | 0B8 | $V_{CC}$ | 0A2 | 0A4 | 0A12 | 0D14 | 0D9 | 0D5 | 0D0 | 1D0 | 1D5 | 1D10 | 1D14 | 1A14 | 1A10 | 1A8 | $V_{CC}$ | 1A3 | GND |
| 19 | 0B2 | 0A3 | 0A8 | 0A11 | 0A13 | 0D12 | 0D8 | 0D4 | 0D3 | I0/CLK0 | I1/CLK1 | 1D4 | 1D8 | 1D9 | 1D13 | 1A15 | 1A12 | 1A9 | 1A7 | GND |
| 20 | GND | GND | 0D15 | 0D13 | 0D10 | GND | 0D7 | GND | 0D2 | GND | 1D2 | 1D3 | GND | 1D7 | GND | 1D12 | 1D15 | 1A13 | GND | GND |

**Pin Designations**

| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| NC | = | No Connect |
| $V_{CC}$ | = | Supply Voltage |
| TDI | = | Test Data In |
| TCK | = | Test Clock |
| TMS | = | Test Mode Select |
| TDO | = | Test Data Out |

**4 D 15**

- 15 — Macrocell (0-15)
- D — PAL Block (A-D)
- 4 — Segment (0-4)

20446G-029

**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# 352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

## Bottom View (Macrocell Association)

**352-Ball BGA**

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | Y | AA | AB | AC | AD | AE | AF | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | NC | NC | GND | NC | 5A12 | GND | 5D15 | 5D11 | GND | 5D6 | 5D3 | I3/CLK3 | GND | 4D1 | 4D5 | 4D9 | GND | 4D15 | 4A13 | GND | NC | 4A6 | GND | NC | NC | 1 |
| 2 | NC | NC | NC | 5A2 | 5A5 | 5A9 | 5A14 | 5A15 | 5D13 | 5D10 | 5D8 | 5D4 | 5D0 | 4D0 | 4D2 | 4D6 | 4D10 | 4D13 | 4A15 | 4A12 | 4A9 | 4A8 | 4A3 | 4A1 | GND | GND | 2 |
| 3 | GND | GND | NC | 5A1 | 5A4 | 5A7 | 5A8 | 5A10 | 5A13 | 5D14 | 5D9 | 5D5 | 5D1 | I2/CLK2 | 4D4 | 4D7 | 4D11 | 4D14 | 4A14 | 4A10 | 4A7 | 4A5 | 4A2 | TMS | NC | NC | 3 |
| 4 | NC | 6A14 | NC | TDO | 5A0 | 5A3 | 5A6 | $V_{CC}$ | 5A11 | $V_{CC}$ | 5D12 | 5D7 | 5D2 | $V_{CC}$ | 4D3 | 4D8 | 4D12 | $V_{CC}$ | 4A11 | $V_{CC}$ | 4A4 | 4A0 | $V_{CC}$ | 3A15 | 3A13 | 3A12 | 4 |
| 5 | GND | 6A12 | 6A13 | $V_{CC}$ | | | | | | | | | | | | | | | | | | | 3A14 | 3A11 | 3A9 | GND | 5 |
| 6 | NC | 6A9 | 6A10 | 6A15 | | | | | | | | | | | | | | | | | | | 3A10 | 3A8 | 3A7 | 3A5 | 6 |
| 7 | GND | 6A6 | 6A8 | 6A11 | | | | | | | | | | | | | | | | | | | 3A6 | 3A4 | 3A3 | 3A0 | 7 |
| 8 | 6A1 | 6A4 | 6A5 | 6A7 | | | | | | | | | | | | | | | | | | | 3A2 | 3A1 | 3B0 | NC | 8 |
| 9 | 6B1 | 6A0 | 6A2 | 6A3 | | | | | | | | | | | | | | | | | | | $V_{CC}$ | 3B1 | 3B2 | GND | 9 |
| 10 | GND | 6B2 | 6B0 | $V_{CC}$ | | | | | | | | | | | | | | | | | | | 3B3 | 3B4 | 3B5 | 3B6 | 10 |
| 11 | 6B6 | 6B5 | 6B4 | 6B3 | | | | | | | | | | | | | | | | | | | 3B7 | 3B8 | 3B9 | 3B10 | 11 |
| 12 | 6B10 | 6B9 | 6B8 | 6B7 | | | | | | | | | | | | | | | | | | | 3B11 | 3B12 | 3B13 | 3B14 | 12 |
| 13 | 6B14 | 6B13 | 6B12 | 6B11 | | | | | | | | | | | | | | | | | | | $V_{CC}$ | 2B15 | 3B15 | GND | 13 |
| 14 | GND | 7B15 | 6B15 | $V_{CC}$ | | | | | | | | | | | | | | | | | | | 2B11 | 2B12 | 2B13 | 2B14 | 14 |
| 15 | 7B14 | 7B13 | 7B12 | 7B11 | | | | | | | | | | | | | | | | | | | 2B7 | 2B8 | 2B9 | 2B10 | 15 |
| 16 | NC | 7B10 | 7B9 | 7B8 | | | | | | | | | | | | | | | | | | | 2B3 | 2B4 | 2B5 | 2B6 | 16 |
| 17 | 7B7 | 7B6 | 7B5 | 7B4 | | | | | | | | | | | | | | | | | | | $V_{CC}$ | 2B0 | 2B2 | GND | 17 |
| 18 | GND | 7B3 | 7B2 | $V_{CC}$ | | | | | | | | | | | | | | | | | | | 2A3 | 2A2 | 2A0 | 2B1 | 18 |
| 19 | 7B1 | 7B0 | 7A1 | 7A4 | | | | | | | | | | | | | | | | | | | 2A7 | 2A5 | 2A4 | 2A1 | 19 |
| 20 | 7A0 | 7A2 | 7A3 | 7A8 | | | | | | | | | | | | | | | | | | | 2A11 | 2A8 | 2A6 | GND | 20 |
| 21 | 7A5 | 7A6 | 7A7 | 7A12 | | | | | | | | | | | | | | | | | | | 2A15 | 2A10 | 2A9 | NC | 21 |
| 22 | GND | 7A9 | 7A11 | 7A15 | | | | | | | | | | | | | | | | | | | $V_{CC}$ | 2A13 | 2A12 | GND | 22 |
| 23 | 7A10 | 7A13 | 7A14 | $V_{CC}$ | 0A0 | 0A4 | $V_{CC}$ | 0A11 | $V_{CC}$ | 0D12 | 0D8 | 0D3 | $V_{CC}$ | 1D2 | 1D7 | 1D12 | $V_{CC}$ | 1A11 | $V_{CC}$ | 1A6 | 1A3 | 1A0 | TCK | NC | 2A14 | NC | 23 |
| 24 | NC | NC | TDI | 0A2 | 0A5 | 0A7 | 0A10 | 0A14 | 0D14 | 0D11 | 0D7 | 0D4 | I0/CLK0 | 1D1 | 1D5 | 1D9 | 1D14 | 1A13 | 1A10 | 1A8 | 1A7 | 1A4 | 1A1 | NC | GND | GND | 24 |
| 25 | GND | GND | 0A1 | 0A3 | 0A8 | 0A9 | 0A12 | 0A15 | 0D13 | 0D10 | 0D6 | 0D2 | 0D0 | 1D0 | 1D4 | 1D8 | 1D10 | 1D13 | 1A15 | 1A14 | 1A9 | 1A5 | 1A2 | NC | NC | NC | 25 |
| 26 | NC | NC | GND | 0A6 | NC | GND | 0A13 | 0D15 | GND | 0D9 | 0D5 | 0D1 | GND | I1/CLK1 | 1D3 | 1D6 | GND | 1D11 | 1D15 | GND | 1A12 | NC | GND | NC | NC | NC | 26 |

20446G-031

**Pin Designations**

| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| NC | = | No Connect |
| $V_{CC}$ | = | Supply Voltage |
| TDI | = | Test Data In |
| TCK | = | Test Clock |
| TMS | = | Test Mode Select |
| TDO | = | Test Data Out |

**7 D 15**

- 15 — Macrocell (0-15)
- D — PAL Block (A-D)
- 7 — Segment (0-7)

**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# 5V M5 ORDERING INFORMATION[1,2]

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

.

**M5- 512 /256 -7 SA C**

**FAMILY TYPE**

M5- = MACH 5 (5-V $V_{CC}$)

**MACROCELL DENSITY**

128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

**I/Os**

/68 = 68 I/Os in 100-pin PQFP or TQFP
/104 = 104 I/Os in 144-pin PQFP or TQFP
/120 = 120 I/Os in 160-pin PQFP
/160 = 160 I/Os in 208-pin PQFP
/192 = 192 I/Os in 256-ball BGA
/256 = 256 I/Os in 352-ball BGA

**PROGRAMMING DESIGNATOR**

Blank = Initial Algorithm
/1 = First Revision

**OPERATING CONDITIONS**

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

**PACKAGE TYPE**

Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
SA = Ball Grid Array (BGA)

**SPEED**

-5 = 5.5 ns $t_{PD}$
-6 = 6.5 ns $t_{PD}$
-7 = 7.5 ns $t_{PD}$
-10 = 10 ns $t_{PD}$
-12 = 12 ns $t_{PD}$
-15 = 15 ns $t_{PD}$
-20 = 20 ns $t_{PD}$

***Note:***

*1. See below for valid device/package combinations.*

*2. M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.*

| Valid Combinations | | |
|---|---|---|
| M5-128/68 | Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20 | YC, VC, YI, VI |
| M5-128/104 | | YC[1], YI[1] |
| M5-128/120 | | YC, YI |
| M5-192/68 | | VC, VI |
| M5-192/120 | | YC, YI |
| M5-256/68 | | VC, VI |
| M5-256/120 | | YC, YI |
| M5-256/160 | | YC, YI |

**Device Marking**

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

| Valid Combinations | | |
|---|---|---|
| M5-320/160 | Commercial: -6, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20 | YC, YI |
| M5-320/192 | | SAC, SAI |
| M5-384/160 | | YC, YI |
| M5-512/160 | | YC, YI |
| M5-512/256 | | SAC, SAI |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Select devices have been discontinued. See Ordering Information section for product status.**