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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

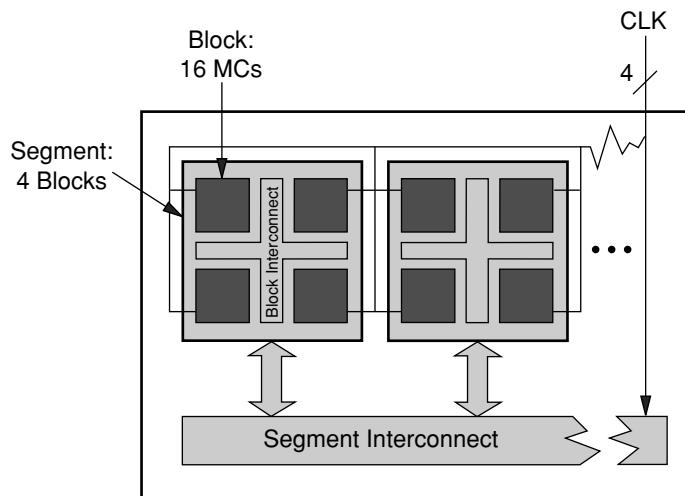
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	120
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-256-120-12yc">https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-256-120-12yc</a>

**Select devices have been discontinued.**  
See Ordering Information section for product status.

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.



20446G-001

**Figure 1. MACH 5 Block Diagram**

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- ◆ I/O cells
- ◆ Product-term array and Logic Allocator
- ◆ Macrocells
- ◆ Register control generator
- ◆ Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS<sup>1</sup>

Both the 3.3-V and 5-V V<sub>CC</sub> MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

**Note:**

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

## BUS-FRIENDLY INPUTS AND I/Os

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

## PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V<sub>CC</sub> rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

**Select devices have been discontinued.  
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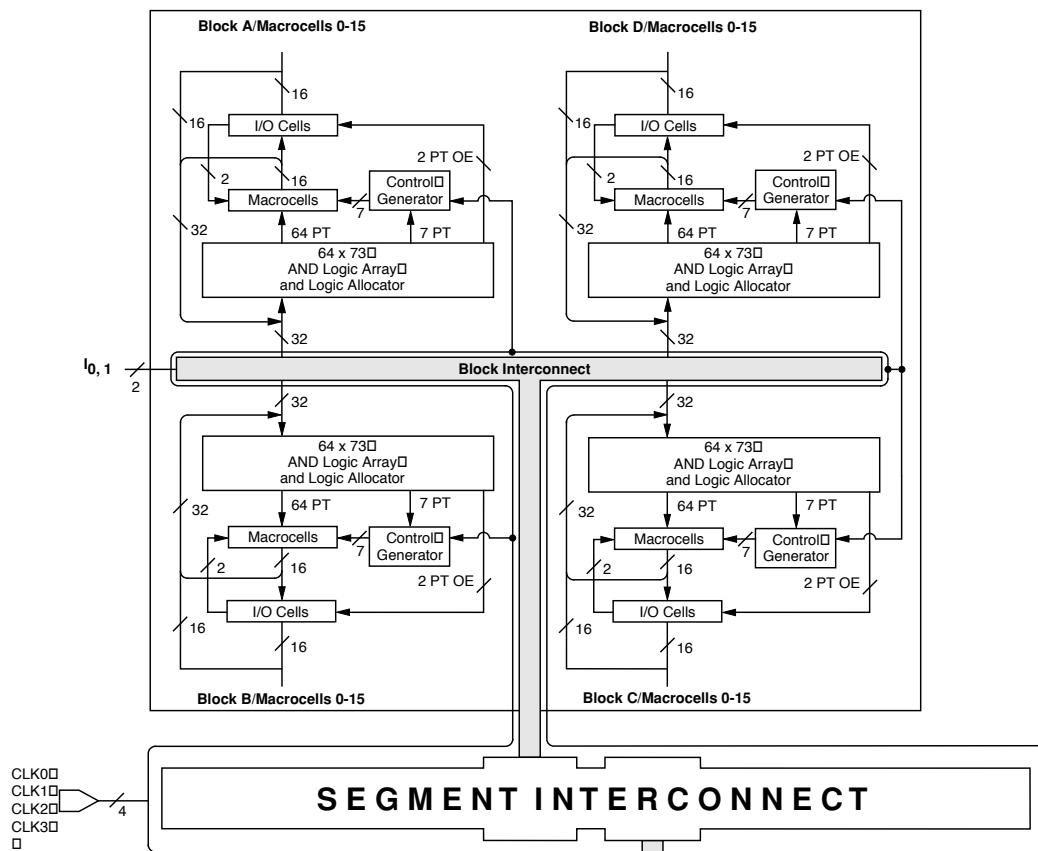
## SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

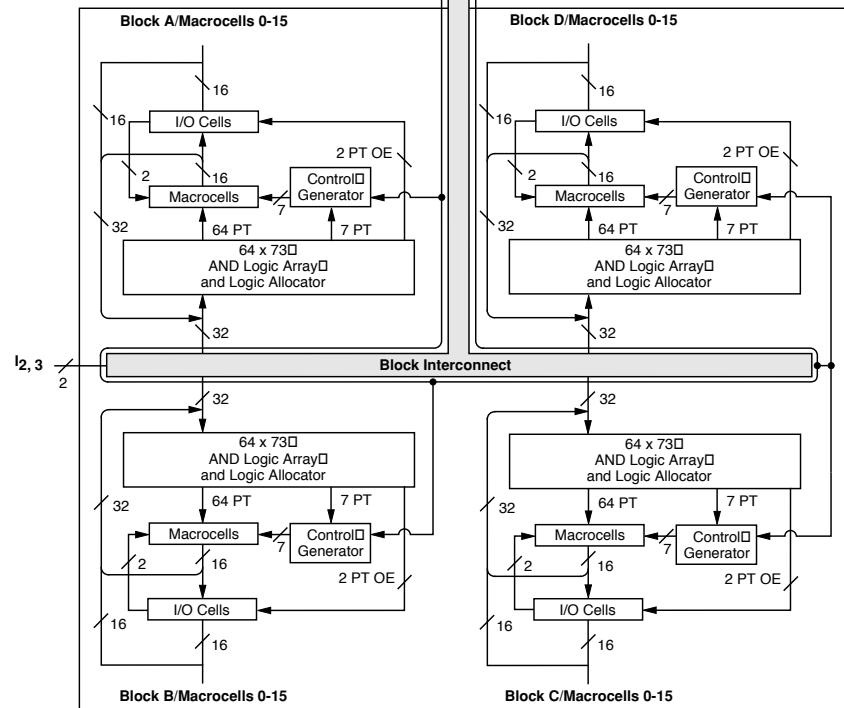
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See Ordering Information section for product status.

## BLOCK DIAGRAM — M5(LV)-128/XXX

### SEGMENT 0



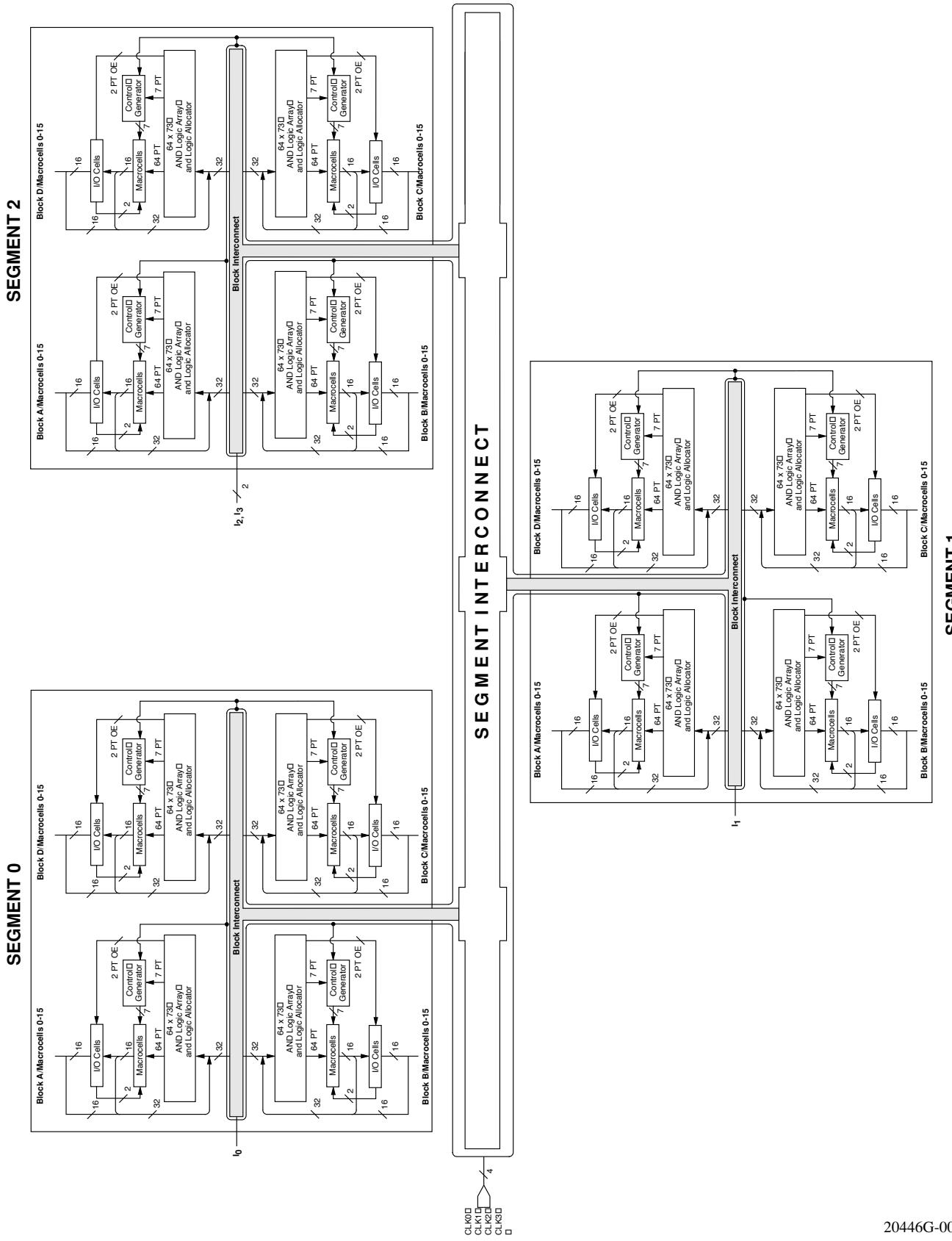
### SEGMENT INTERCONNECT



### SEGMENT 1

20446G-007

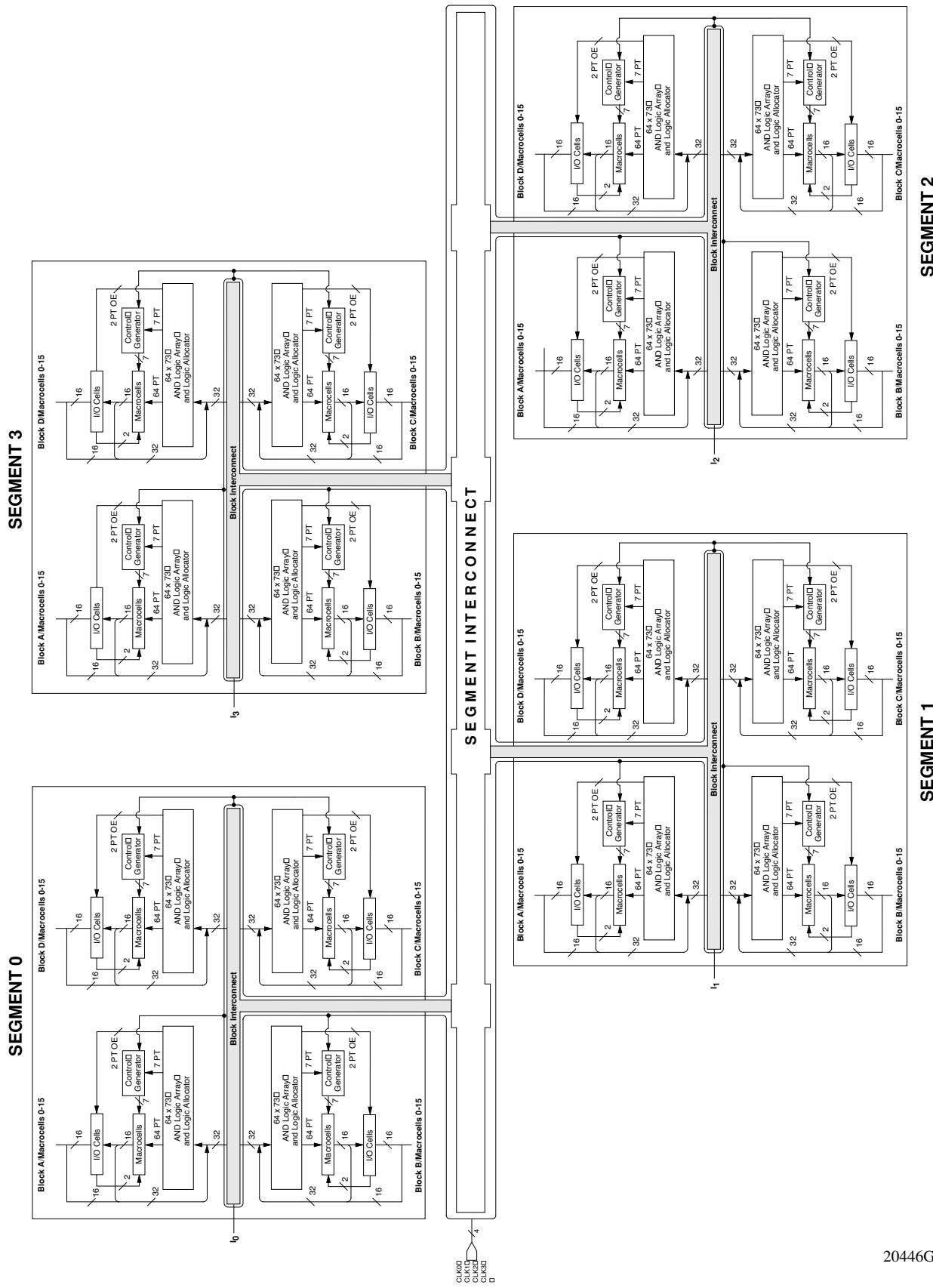
## BLOCK DIAGRAM — M5-192/XXX



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**See Ordering Information section for product status.**

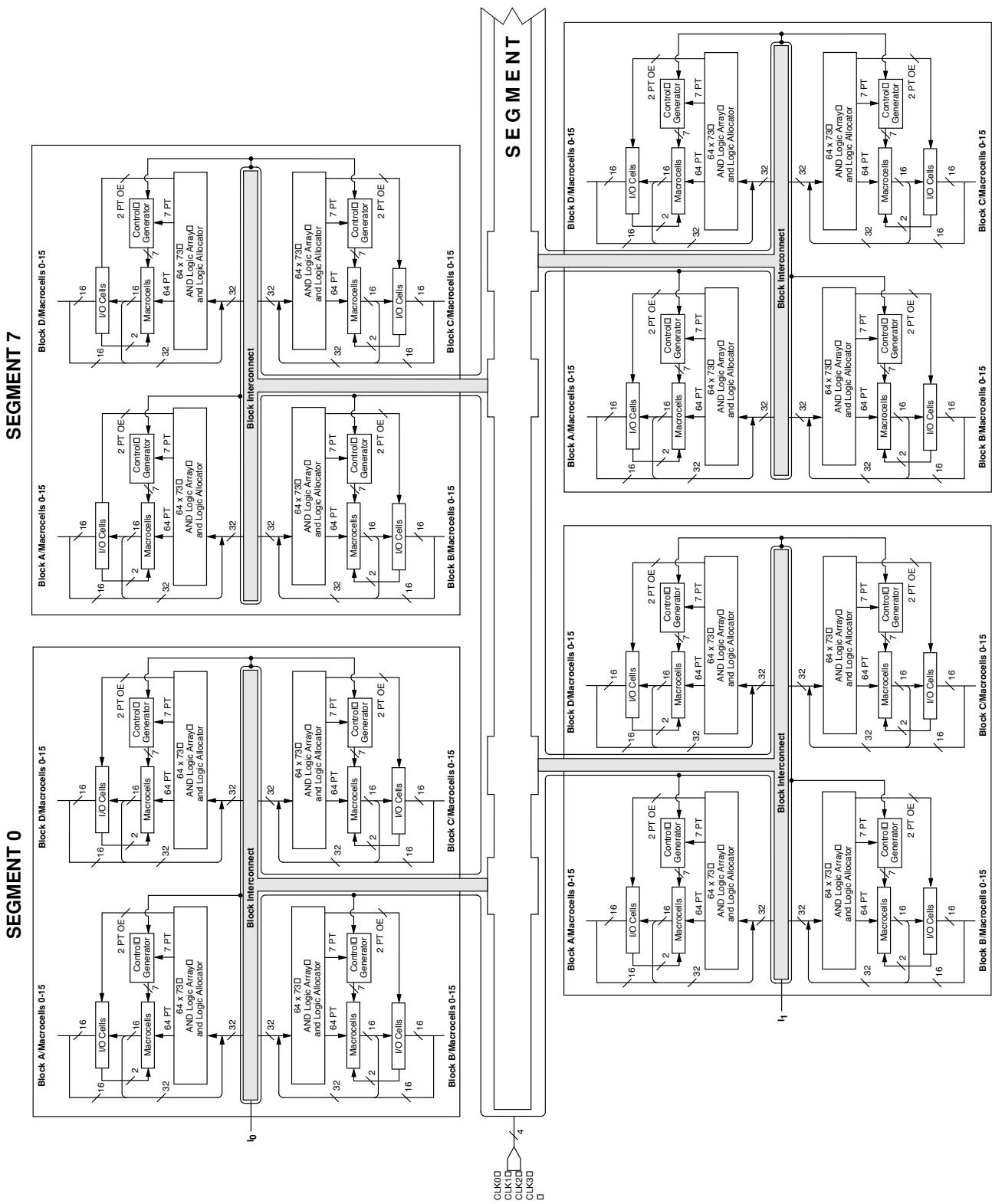
## BLOCK DIAGRAM — M5(LV)-256/XXX



20446G-009

# BLOCK DIAGRAM — M5(LV)-512/XXX

## **Continued**



**Select devices have been discontinued.  
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See Ordering Information section for product status.

## ABSOLUTE MAXIMUM RATINGS

### M5

Storage Temperature.....	-65°C to +150°C
Device Junction Temperature (Note 1).....	+130°C or +150°C
Supply Voltage with Respect to Ground .....	-0.5 V to +7.0 V
DC Input Voltage .....	-0.5 V to 5.5 V
Static Discharge Voltage.....	2000 V
Latchup Current (-40°C to +85°C) .....	200 mA
<i>Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.</i>	

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air.....	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground.....	+4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air.....	-40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground.....	+4.5 V to +5.5 V
<i>Operating ranges define those limits between which the functionality of the device is guaranteed.</i>	

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage (For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices)	$I_{OH} = -3.2 \text{ mA}, V_{CC} = \text{Min}, V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = -100 \mu\text{A}, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL}$		3.3	3.6	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	$I_{OH} = -3.2 \text{ mA}, V_{CC} = \text{Min}, V_{IN} = V_{IH} \text{ or } V_{IL}$	2.4			V
		$I_{OH} = -2.5 \text{ mA}, V_{CC} = 5.25 \text{ V}, V_{IN} = V_{IH} \text{ or } V_{IL}$			3.6	V
$V_{OL}$	Output LOW Voltage (Note 2)	$I_{OL} = +16 \text{ mA}, V_{CC} = \text{Min}, V_{IN} = V_{IH} \text{ or } V_{IL}$			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25, V_{CC} = \text{Max}$ (Note 4)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max}$ (Note 4)			-10	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 4)			-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5 \text{ V}, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 5)	-30		-180	mA

#### Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.
- Total  $I_{OL}$  between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

Select devices have been discontinued.  
See Ordering Information section for product status.

## ABSOLUTE MAXIMUM RATINGS

### M5LV

Storage Temperature.....	-65°C to +150°C
Device Junction Temperature.....	+130°C
Supply Voltage with Respect to Ground .....	-0.5 V to +4.5 V
DC Input Voltage .....	-0.5 V to 5.5 V
Static Discharge Voltage.....	2000 V
Latchup Current (-40°C to +85°C) .....	200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air.....	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground.....	+3.0 V to +3.6 V

### Industrial (I) Devices

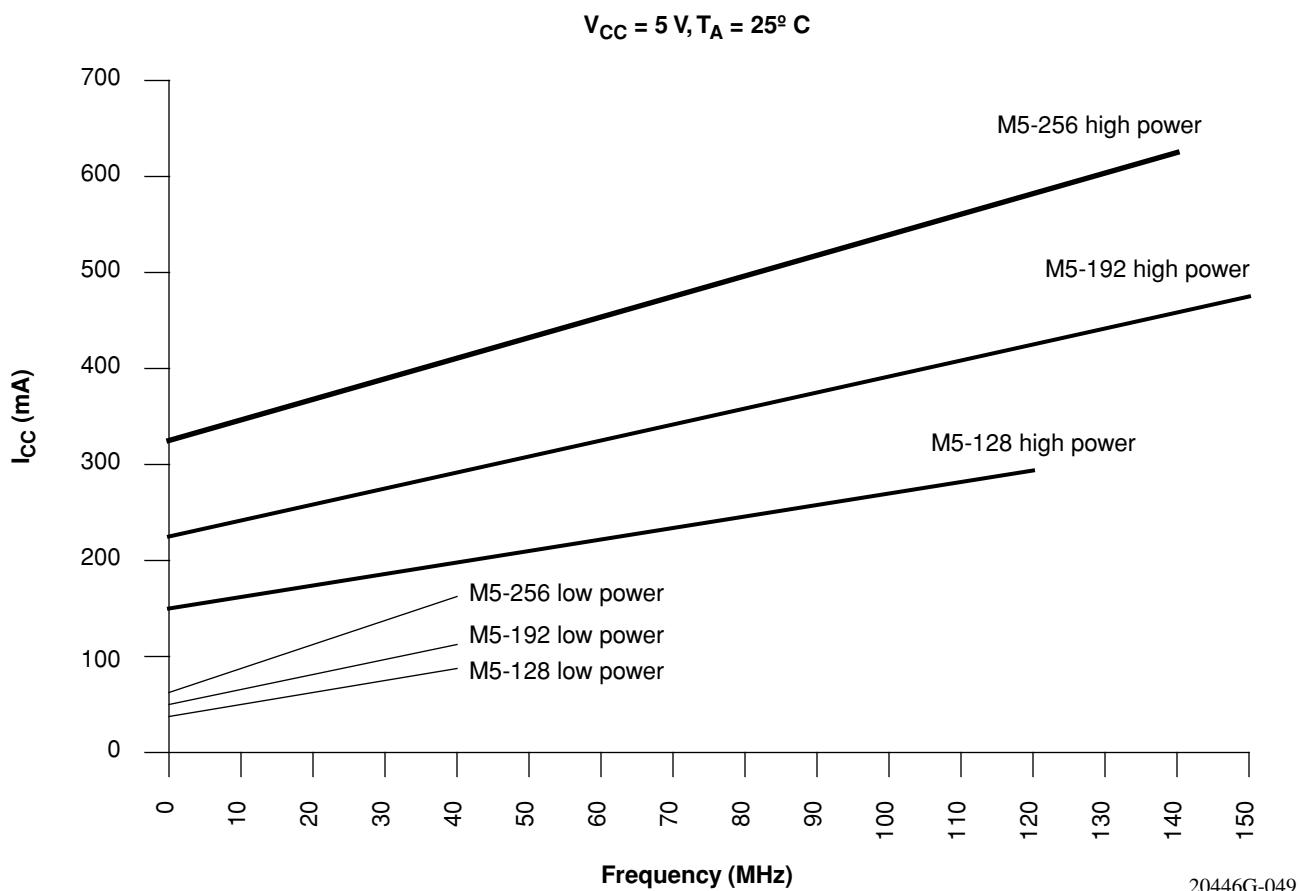
Ambient Temperature ( $T_A$ )	
Operating in Free Air.....	40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground.....	+3.0 V to +3.6 V
<i>Operating ranges define those limits between which the functionality of the device is guaranteed.</i>	

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -100 \mu\text{A}$	$V_{CC} = 0.2$		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 3.2 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 100 \mu\text{A}$		0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16 \text{ mA } (\text{Note 1})$		0.5	V
$V_{IH}$	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max } (\text{Note 2})$		2.0	5.5	V
$V_{IL}$	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max } (\text{Note 2})$		-0.3	0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max } (\text{Note 3})$			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max } (\text{Note 3})$			-10	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-15	-160	mA

#### Notes:

1. Total  $I_{OL}$  between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  or  $I_{IH}$  and  $I_{OZH}$ .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.



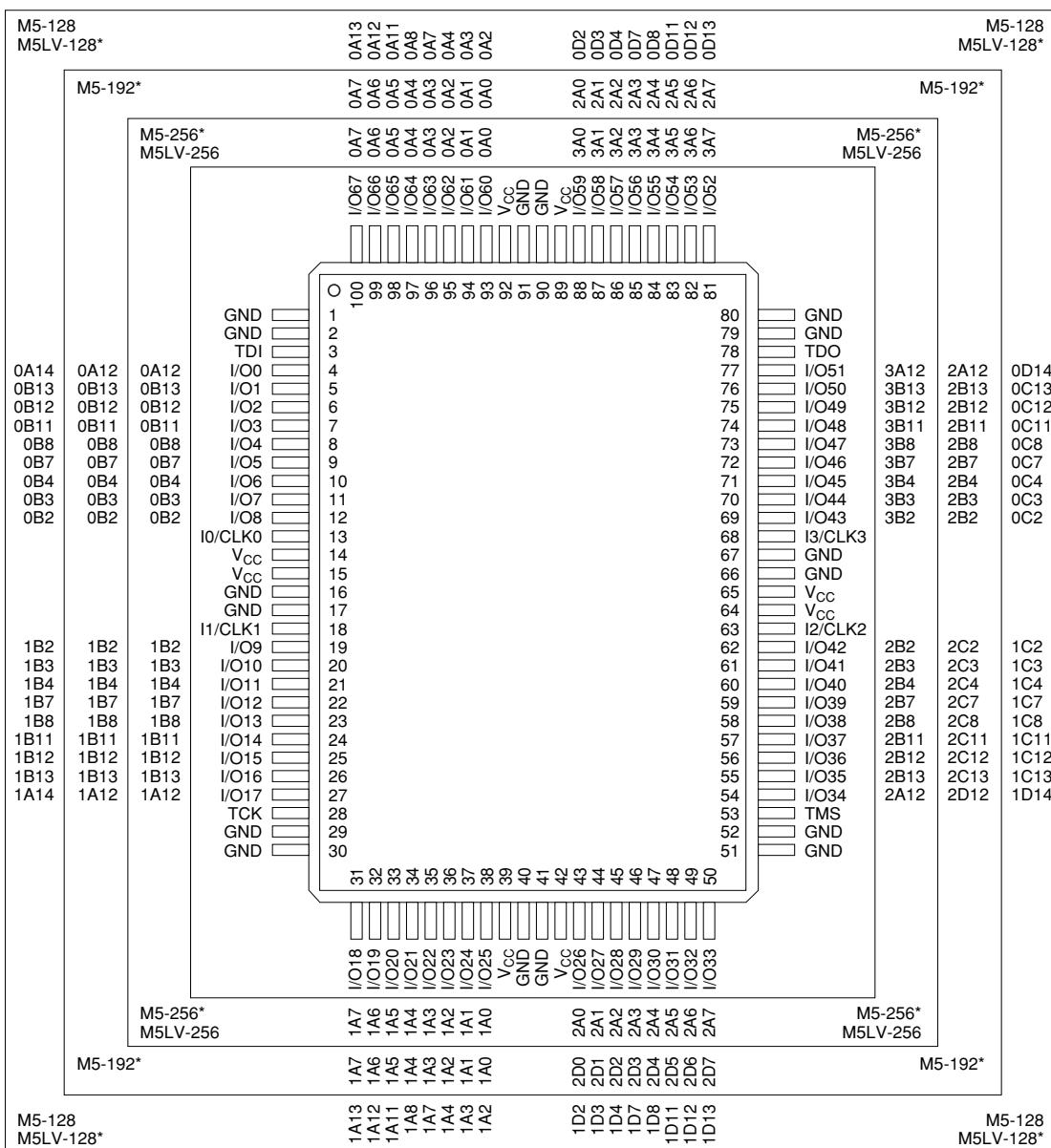
**Figure 9.  $I_{CC}$  Curves at High/Low Power Modes**

Select devices have been discontinued.  
See Ordering Information section for product status.

# 100-PIN PQFP CONNECTION DIAGRAM

## Top View

## **100-Pin PQFP (68 I/O)**

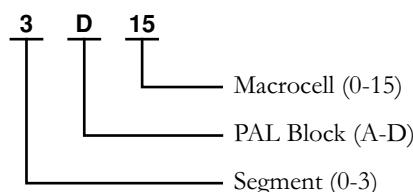


\*Package obsolete, contact factory.

20446G-016

## Pin Designations

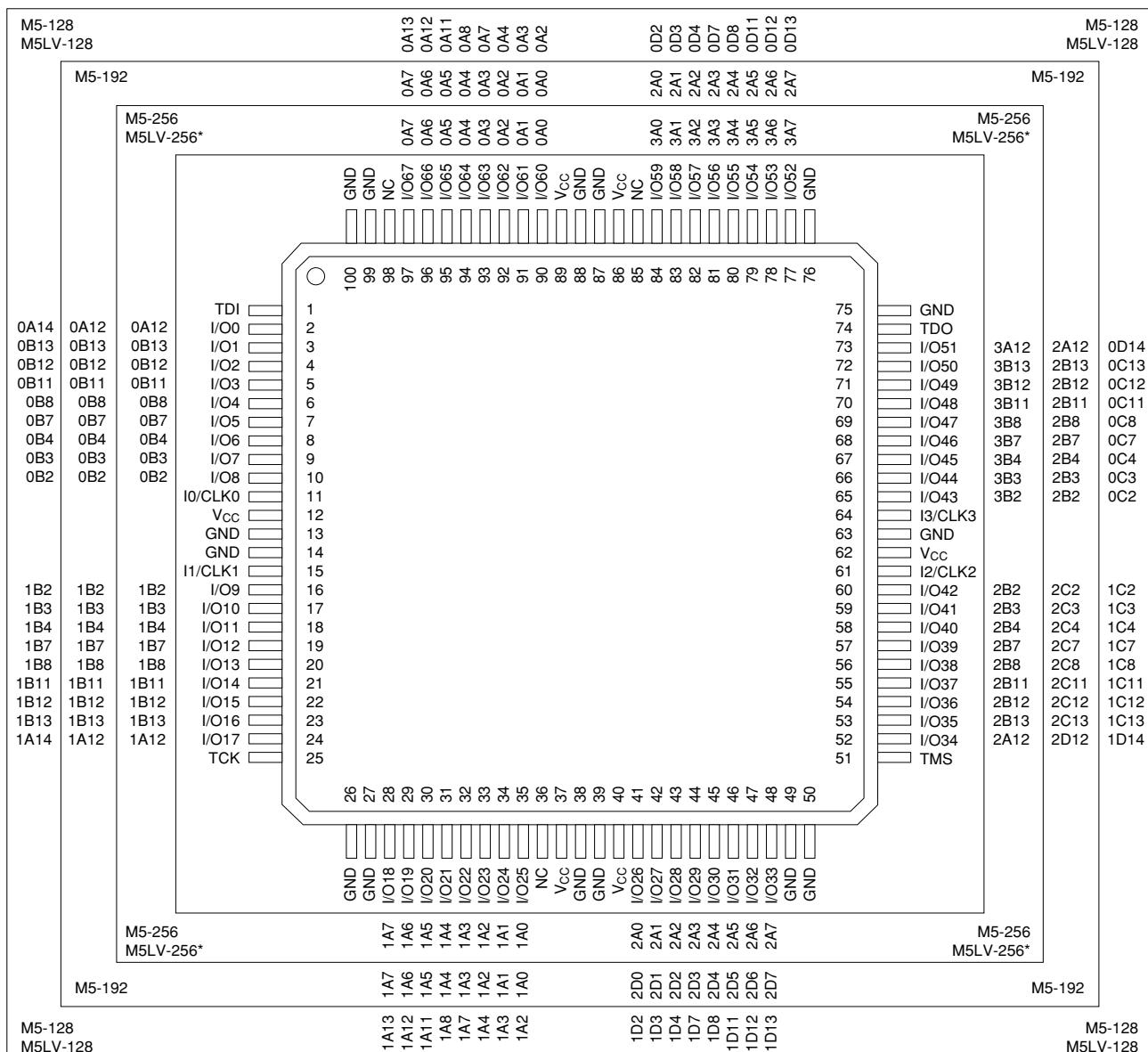
CLK	=	Clock		V <sub>CC</sub>	=	Supply Voltage
GND	=	Ground		TDI	=	Test Data In
I	=	Input		TCK	=	Test Clock
I/O	=	Input/Output		TMS	=	Test Mode Select
NC	=	No Connect		TDO	=	Test Data Out



# 100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

## Top View

## **100-Pin TQFP (68 I/O)**



\*Package obsolete, contact factory

20446G-017

## Pin Designations

CLK = Clock

GND ≡ Ground

$L = \text{Inp}$

I/O = Input/Output

NC = No Connect

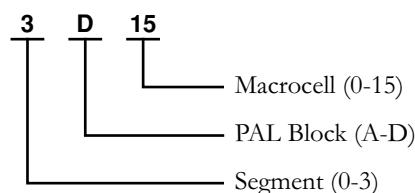
$V_{CC}$  = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TCK = Test Clock

TDO = Test Data Out

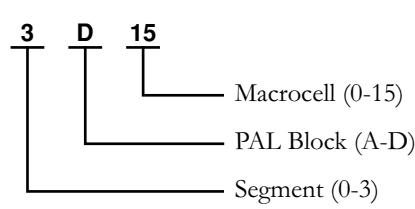
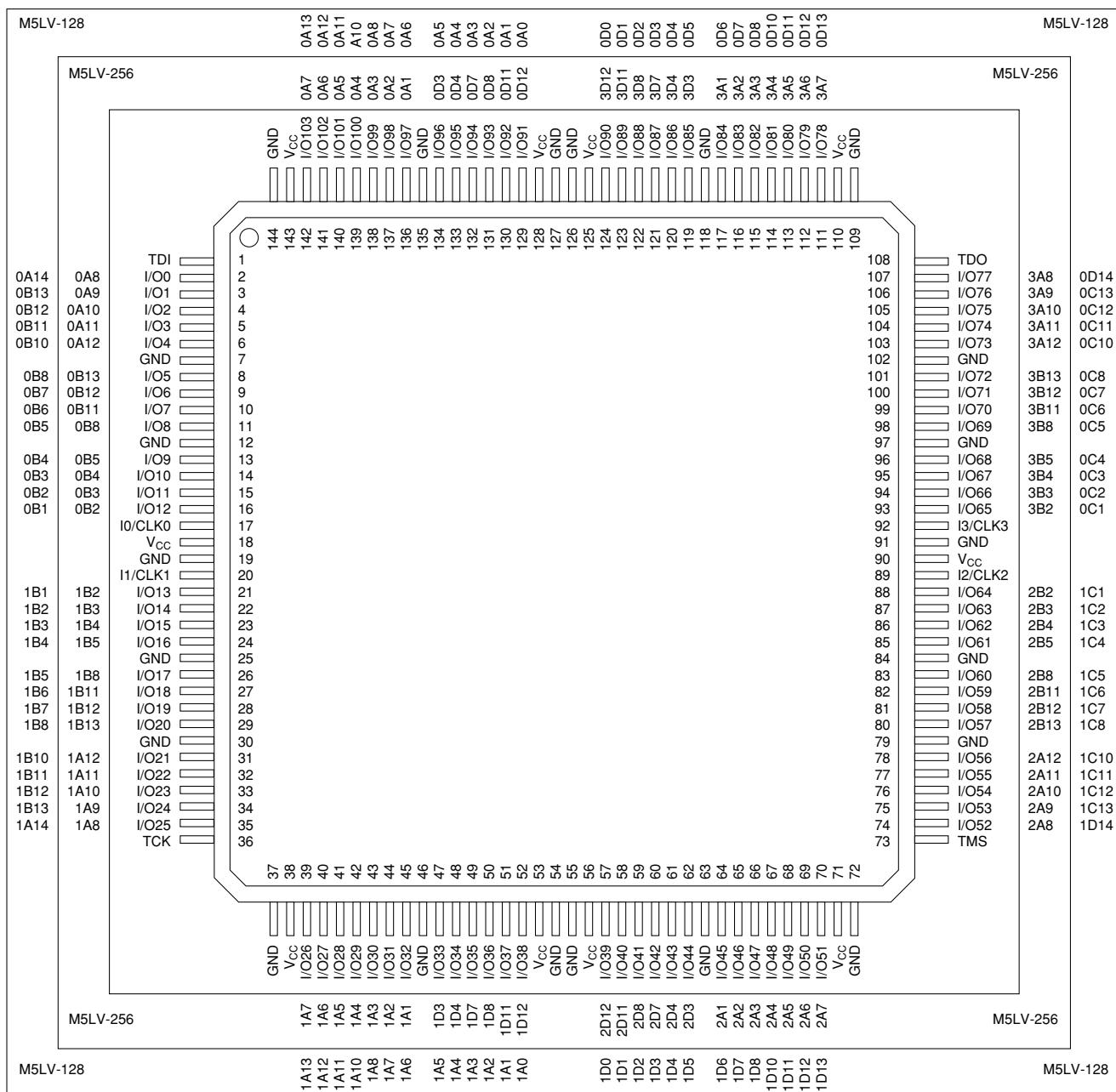


**Select devices have been discontinued.**  
**See Ordering Information section for product status.**

## 144-PIN TQFP CONNECTION DIAGRAM

### Top View

144-Pin TQFP



20446G-020

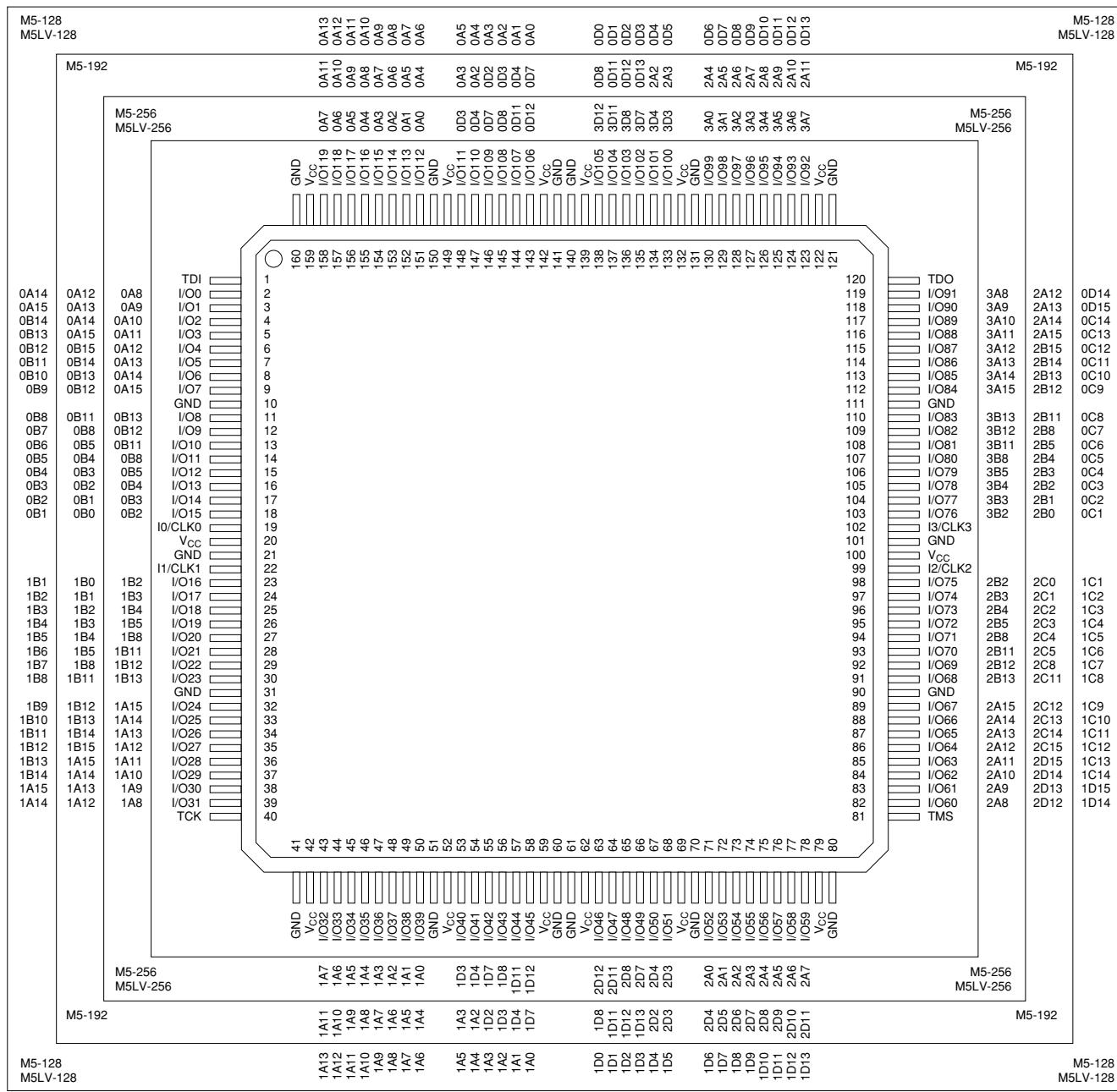
### Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V <sub>CC</sub>	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

# 160-PIN PQFP CONNECTION DIAGRAM

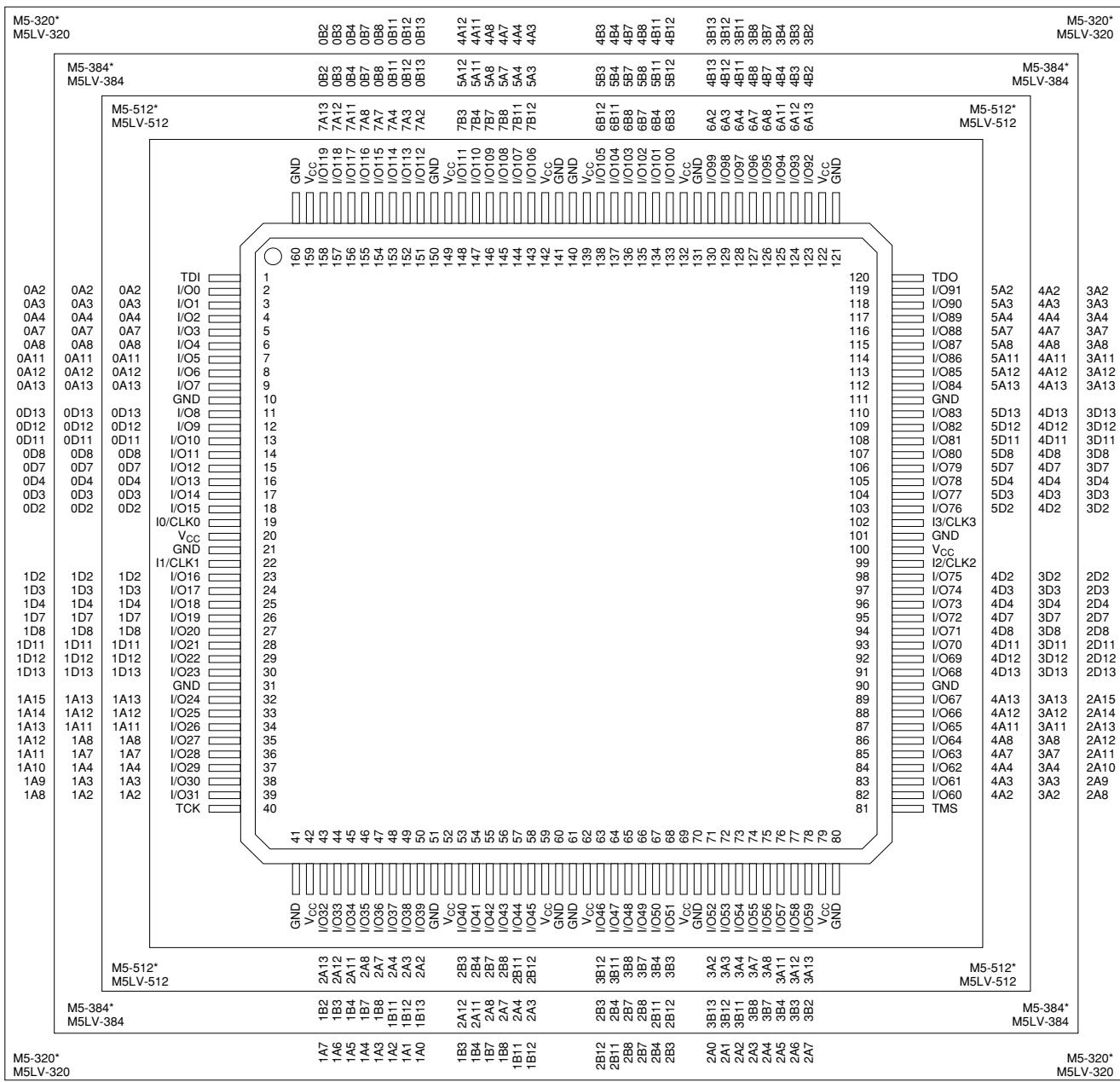
## Top View

160-Pin PQFP (128, 192, 256 Macrocells)



## **160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM**

## 160-Pin PQFP (320, 384, 512 Macrocells)



\*Package obsolete, contact factory.

20446G-022

## Pin Designations

**CLK** = Clock

GND ≡ Ground

J           ≡   Input

I/O   ≡  Input/Output

NC = No Connect

$V_{CC}$  = Supply Voltage

TDI ≡ Test Data In

TCK = Test Clock

TMS ≡ Test Mode Select

TDO = Test Data Out

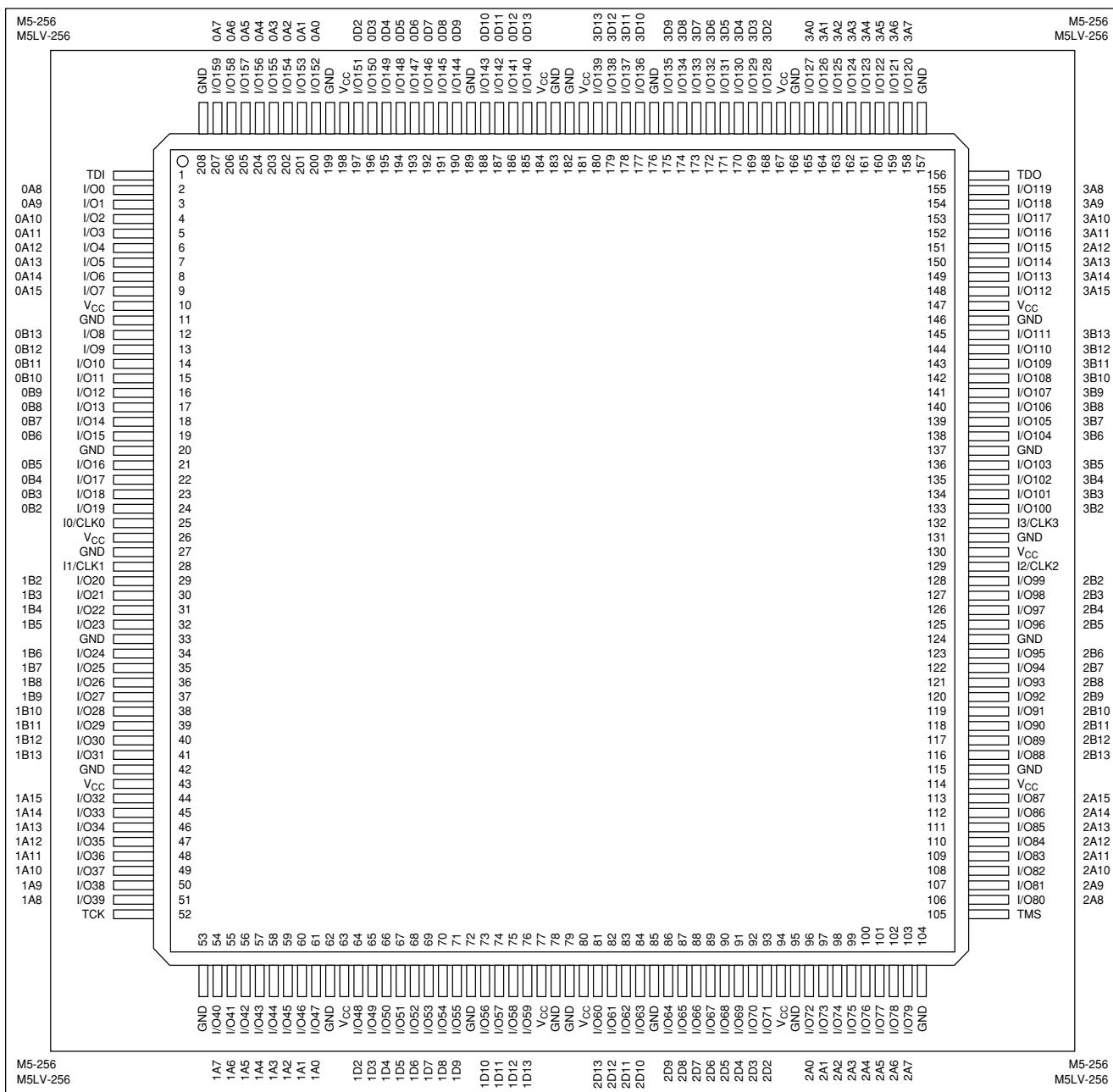
The diagram illustrates the bit mapping for a segment. It shows a sequence of 15 bits starting from bit 7. Bit 7 is mapped to a Segment (0-7). Bit D is mapped to a PAL Block (A-D). The remaining bits from bit 15 down to bit 8 are mapped to a Macrocell (0-15).

**Select devices have been discontinued.**  
**See Ordering Information section for product status**

## 208-PIN PQFP CONNECTION DIAGRAM

### Top View

208-Pin PQFP (256 Macrocells)

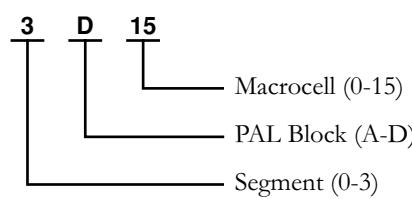


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Select devices have been discontinued.  
See Ordering Information section for product status.

### Pin Designations

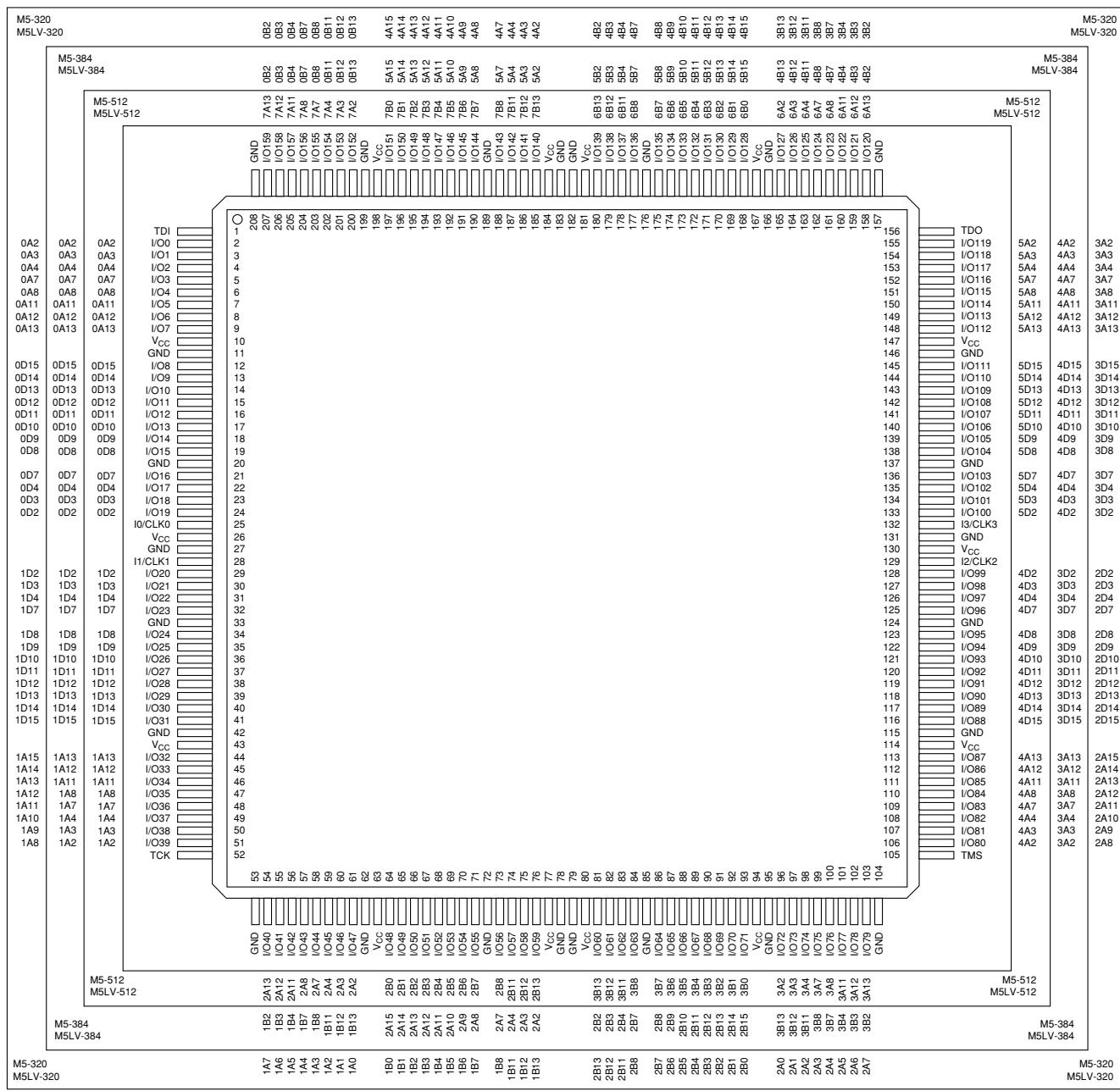
CLK	= Clock	V <sub>CC</sub>	= Supply Voltage
GND	= Ground	TDI	= Test Data In
I	= Input	TCK	= Test Clock
I/O	= Input/Output	TMS	= Test Mode Select
NC	= No Connect	TDO	= Test Data Out



Select devices have been discontinued.  
See Ordering Information section for product status.

## 208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

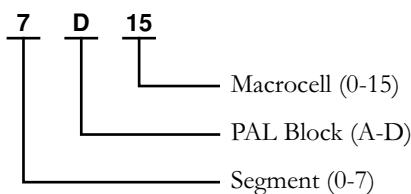
208-Pin PQFP (320, 384, 512 Macrocells)



20446G-024

### Pin Designations

CLK	= Clock	V <sub>CC</sub>	= Supply Voltage
GND	= Ground	TDI	= Test Data In
I	= Input	TCK	= Test Clock
I/O	= Input/Output	TMS	= Test Mode Select
NC	= No Connect	TDO	= Test Data Out



## 256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (I/O Pin-outs)

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	GND	I/O11	GND	I/O44	I/O58	GND	I/O70	I/O76	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	A			
B	GND	I/O12	I/O28	I/O45	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	B		
C	I/O0	I/O13	V <sub>CC</sub>	I/O46	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V <sub>CC</sub>	I/O165	I/O181	C	
D	I/O1	I/O14	I/O29	V <sub>CC</sub>	V <sub>CC</sub>	I/O66	V <sub>CC</sub>	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V <sub>CC</sub>	I/O124	V <sub>CC</sub>	V <sub>CC</sub>	I/O149	I/O166	I/O182	D	
E	I/O2	I/O15	I/O30	TDI											TDO	I/O150	I/O167	I/O183	E			
F	GND	I/O16	I/O31	I/O47											I/O137	I/O151	I/O168	GND	F			
G	I/O3	I/O17	I/O32	V <sub>CC</sub>											V <sub>CC</sub>	I/O152	I/O169	I/O184	G			
H	GND	I/O18	I/O33	I/O48											I/O138	I/O153	I/O170	GND	H			
J	I/O4	I/O19	I/O34	I/O49											I/O139	I/O154	I/O171	I/O185	J			
K	GND	I/O1CK0	I/O35	I/O50											I/O140	I/O155	I <sub>3</sub> /CLK3	I/O186	K			
L	I/O5	I <sub>1</sub> /CLK1	I/O36	I/O51											I/O141	I/O156	I <sub>2</sub> /CLK2	GND	L			
M	I/O6	I/O20	I/O37	I/O52											I/O142	I/O157	I/O172	I/O187	M			
N	GND	I/O21	I/O38	I/O53											I/O143	I/O158	I/O173	GND	N			
P	I/O7	I/O22	I/O39	V <sub>CC</sub>											V <sub>CC</sub>	I/O159	I/O174	I/O188	P			
R	GND	I/O23	I/O40	I/O54												I/O144	I/O160	I/O175	GND	R		
T	I/O8	I/O24	I/O41	TCK											TMS	I/O161	I/O176	I/O189	T			
U	I/O9	I/O25	I/O42	V <sub>CC</sub>	V <sub>CC</sub>	I/O67	V <sub>CC</sub>	I/O80	I/O87	I/O93	I/O99	I/O105	I/O112	V <sub>CC</sub>	I/O125	V <sub>CC</sub>	V <sub>CC</sub>	I/O162	I/O177	I/O190	U	
V	I/O10	I/O26	V <sub>CC</sub>	I/O55	I/O61	I/O68	I/O73	I/O81	I/O88	I/O94	I/O100	I/O106	I/O113	I/O119	I/O126	I/O131	I/O145	V <sub>CC</sub>	I/O178	I/O191	V	
W	GND	I/O27	I/O43	I/O56	I/O62	I/O69	I/O74	I/O82	I/O89	I/O95	I/O101	I/O107	I/O114	I/O120	I/O127	I/O132	I/O146	I/O163	I/O179	GND	W	
Y	GND	GND	GND	I/O57	I/O63	GND	I/O75	I/O83	GND	GND	GND	GND	GND	I/O115	I/O121	GND	I/O133	I/O147	GND	I/O180	GND	Y

### Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

**Select devices have been discontinued.**  
**See Ordering Information section for product status.**

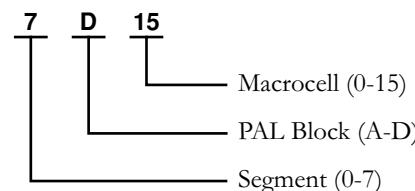
## 352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (Macrocell Association)

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A
A	NC	GND	NC	7A10	GND	7A5	7A0	7B1	GND	7B7	NC	7B14	GND	6B14	6B10	6B6	GND	6B1	6A1	GND	NC	GND	NC	GND	NC	NC	NC
B	NC	GND	NC	7A13	7A9	7A6	7A2	7B0	7B3	7B6	7B10	7B13	7B15	6B13	6B9	6B5	6B2	6A0	6A4	6A6	6A9	6A12	6A14	GND	NC	NC	B
C	GND	0A1	TDI	7A14	7A11	7A7	7A3	7A1	7B2	7B5	7B9	7B12	6B15	6B12	6B8	6B4	6B0	6A2	6A5	6A8	6A10	6A13	NC	NC	NC	NC	C
D	0A6	0A3	0A2	V <sub>CC</sub>	7A15	7A12	7A8	7A4	V <sub>CC</sub>	7B4	7B8	7B11	V <sub>CC</sub>	6B11	6B7	6B3	V <sub>CC</sub>	6A3	6A7	6A11	6A15	V <sub>CC</sub>	TDO	5A1	5A2	GND	D
E	NC	0A8	0A5	0A0																			5A0	5A4	5A5	NC	E
F	GND	0A9	0A7	0A4																			5A3	5A7	5A9	5A12	F
G	0A13	0A12	0A10	V <sub>CC</sub>																			5A6	5A8	5A14	GND	G
H	0D15	0A15	0A14	0A11																			V <sub>CC</sub>	5A10	5A15	5D15	H
J	GND	0D13	0D14	V <sub>CC</sub>																			5A11	5A13	5D13	5D11	J
K	0D9	0D10	0D11	0D12																			V <sub>CC</sub>	5D14	5D10	GND	K
L	0D5	0D6	0D7	0D8																			5D12	5D9	5D8	5D6	L
M	0D1	0D2	0D4	0D3																			5D7	5D5	5D4	5D3	M
N	GND	0D0	I <sub>O</sub> CLK0	V <sub>CC</sub>																			5D2	5D1	5D0	I <sub>3</sub> CLK3	N
P	I <sub>1</sub> CLK1	1D0	1D1	1D2																			V <sub>CC</sub>	I <sub>2</sub> CLK2	4D0	GND	P
R	1D3	1D4	1D5	1D7																			4D3	4D4	4D2	4D1	R
T	1D6	1D8	1D9	1D12																			4D8	4D7	4D6	4D5	T
U	GND	1D10	1D14	V <sub>CC</sub>																			4D12	4D11	4D10	4D9	U
V	1D11	1D13	1A13	1A11																			V <sub>CC</sub>	4D14	4D13	GND	V
W	1D15	1A15	1A10	V <sub>CC</sub>																			4A11	4A14	4A15	4D15	W
Y	GND	1A14	1A8	1A6																			V <sub>CC</sub>	4A10	4A12	4A13	Y
AA	1A12	1A9	1A7	1A3																			4A4	4A7	4A9	GND	AA
AB	NC	1A5	1A4	1A0																			4A0	4A5	4A8	NC	AB
AC	GND	1A2	1A1	TCK	V <sub>CC</sub>	2A15	2A11	2A7	2A3	V <sub>CC</sub>	2B3	2B7	2B11	V <sub>CC</sub>	3B3	3B7	3B3	V <sub>CC</sub>	3A2	3A6	3A10	3A14	V <sub>CC</sub>	4A2	4A3	4A6	AC
AD	NC	NC	NC	2A13	2A10	2A8	2A5	2A2	2B0	2B4	2B8	2B12	2B15	3B12	3B8	3B4	3B1	3A1	3A4	3A8	3A11	3A15	TMS	4A1	GND	AD	
AE	NC	NC	GND	2A14	2A12	2A9	2A6	2A4	2A0	2B2	2B5	2B9	2B13	3B15	3B9	3B5	3B2	3B0	3A3	3A7	3A9	3A13	NC	GND	NC	AE	
AF	NC	NC	GND	NC	GND	NC	GND	2A1	2B1	GND	2B6	2B10	2B14	GND	3B14	3B10	3B6	GND	NC	3A0	3A5	GND	3A12	NC	GND	NC	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

### Pin Designations

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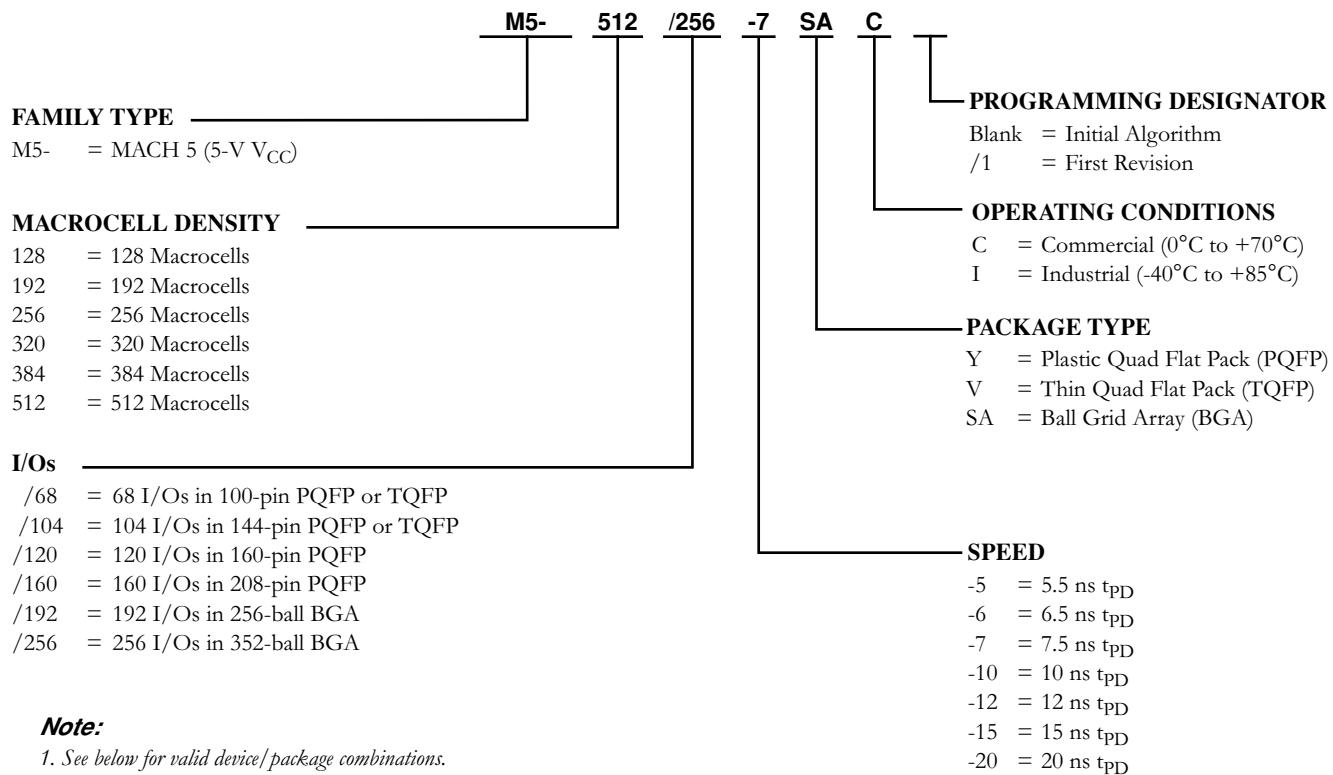
20446G-031

Select devices have been discontinued.  
See Ordering Information section for product status.

Select devices have been discontinued.  
See Ordering Information section for product status.

## 5V M5 ORDERING INFORMATION<sup>1,2</sup>

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



**Note:**

1. See below for valid device/package combinations.
2. M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68		YC, VC, YI, VI
M5-128/104		YC <sup>1</sup> , YI <sup>1</sup>
M5-128/120	Commercial:	YC, YI
M5-192/68	-5, -7, -10, -12, -15	VC, VI
M5-192/120	Industrial:	YC, YI
M5-256/68	-7, -10, -12, -15, -20	VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

### Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial:	YC, YI
M5-320/192		SAC, SAI
M5-384/160	-6, -7, -10, -12, -15	YC, YI
M5-512/160	Industrial:	YC, YI
M5-512/256	-7, -10, -12, -15, -20	SAC, SAI

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.