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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	68
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-256-68-15yi

Table 1. MACH 5 Device Features [1]

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	160	160	160	256	256
t_{PD} (ns)	5.5	5.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	6.5	6.5
t_{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t_{COS} (ns)	4.5	4.5	4.5	4.5	4.5	5.0	5.0	5.0	5.0	5.0	5.0
f_{CNT} (MHz)	182	182	182	182	182	167	167	167	167	167	167
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

GENERAL DESCRIPTION

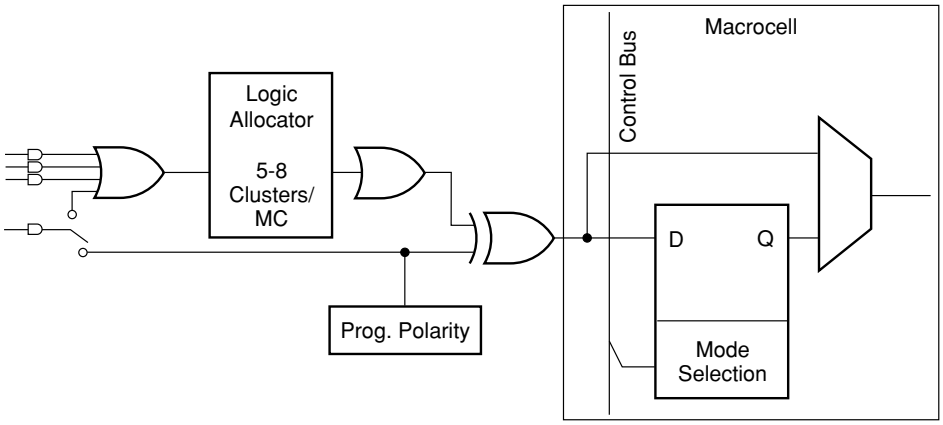
The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E^2CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The
I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as "buried" macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 1 Options

- Global clock (0, 1, 2, or 3) with positive edge clock enable
- Global clock (0, 1, 2, or 3) with negative edge clock enable

- Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- Global clock (0, 1, 2, or 3) with clock enable

Clock Line 3 Options

- Complement of clock line 2 (same clock enable)
- Product-term clock (if clock line 2 does not use clock enable

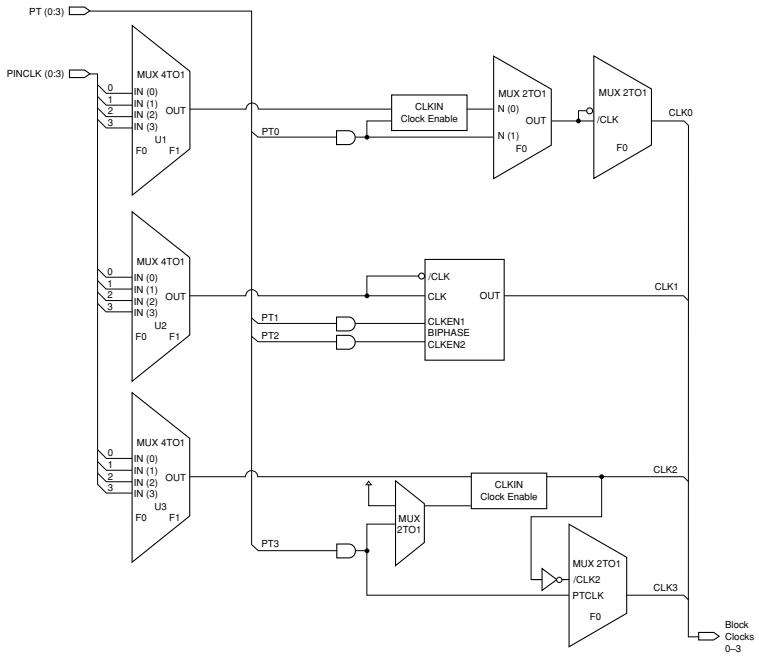


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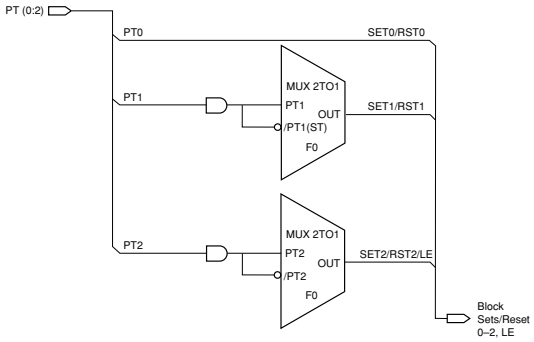
Figure 4. Clock Generator



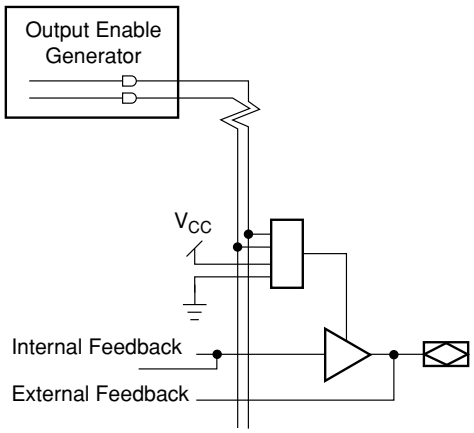
20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).



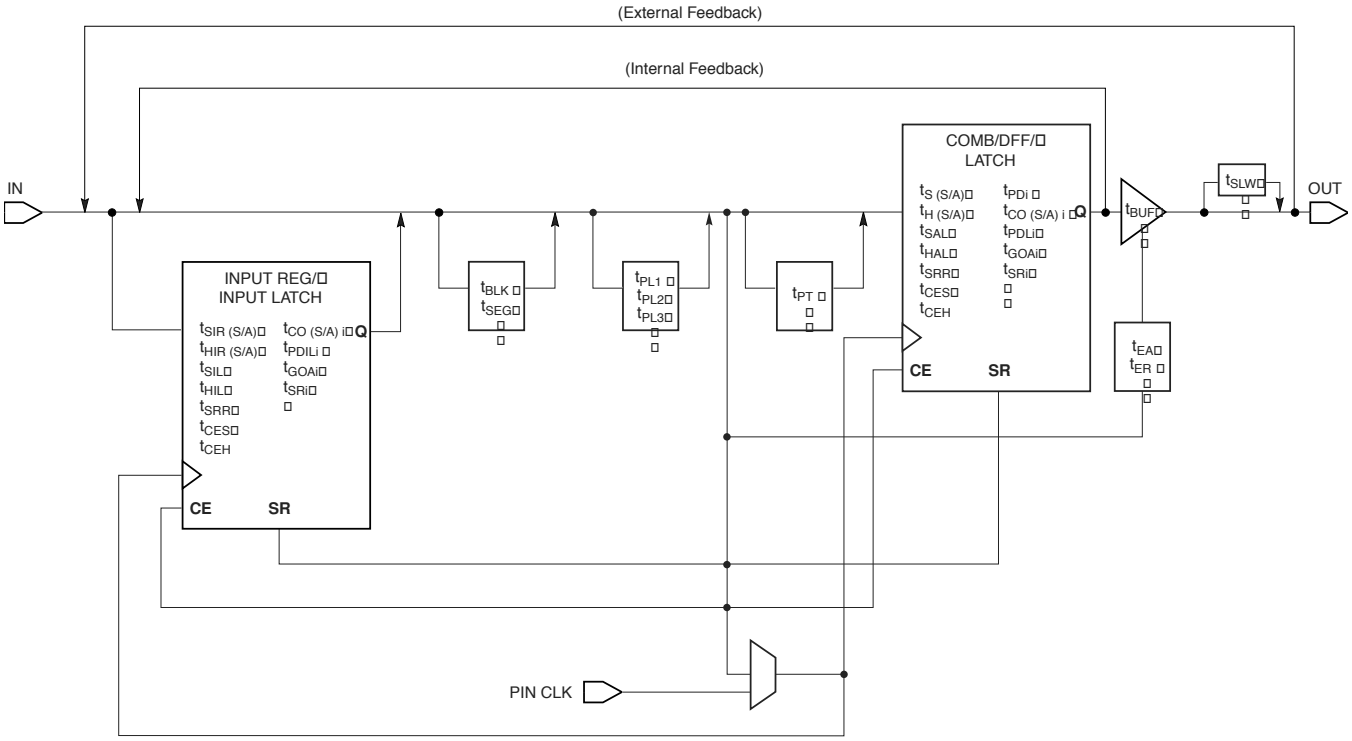
20446G-006

Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



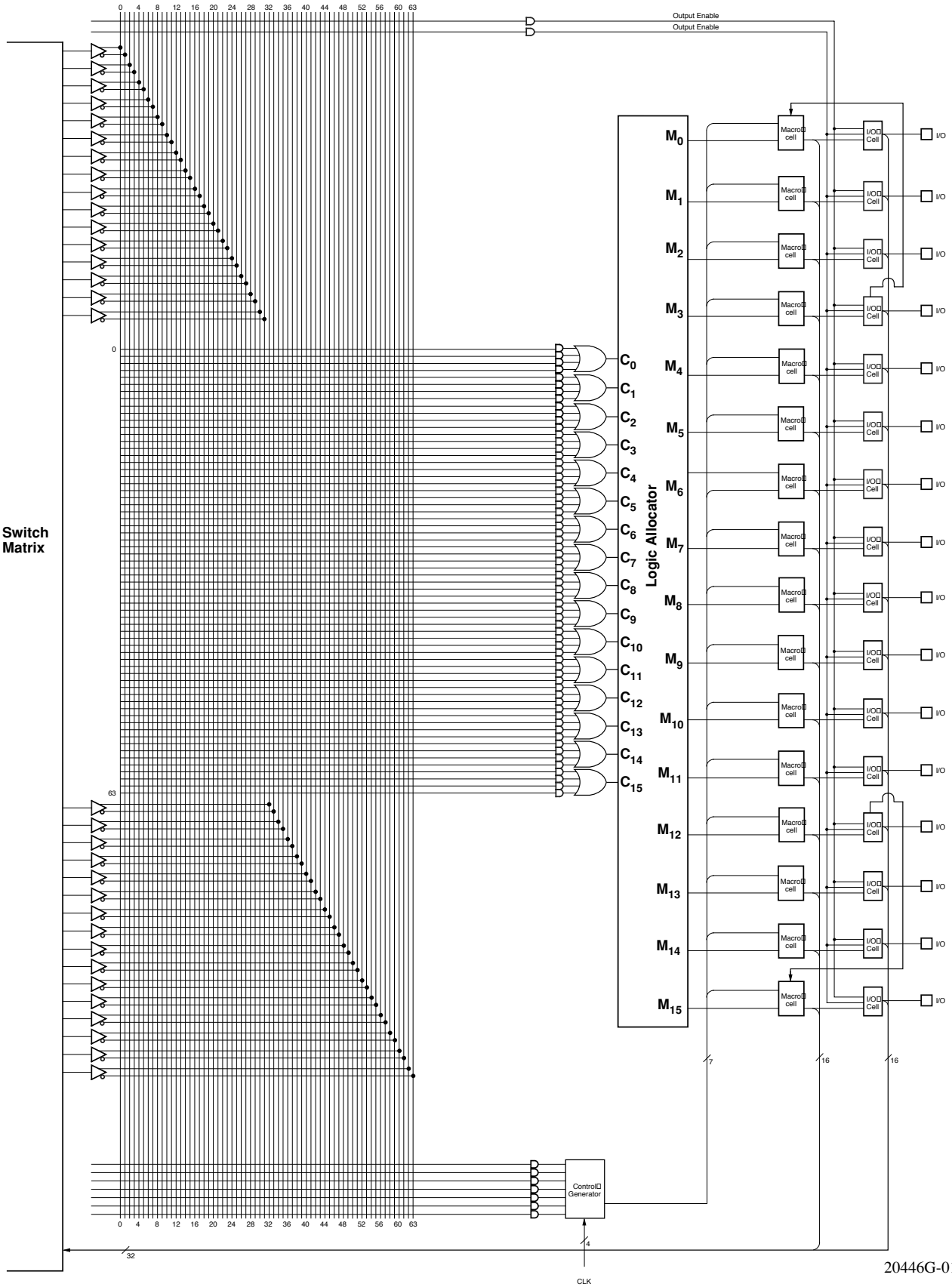
20446G-014

Figure 7. MACH 5 Timing Model

SECURITY BIT

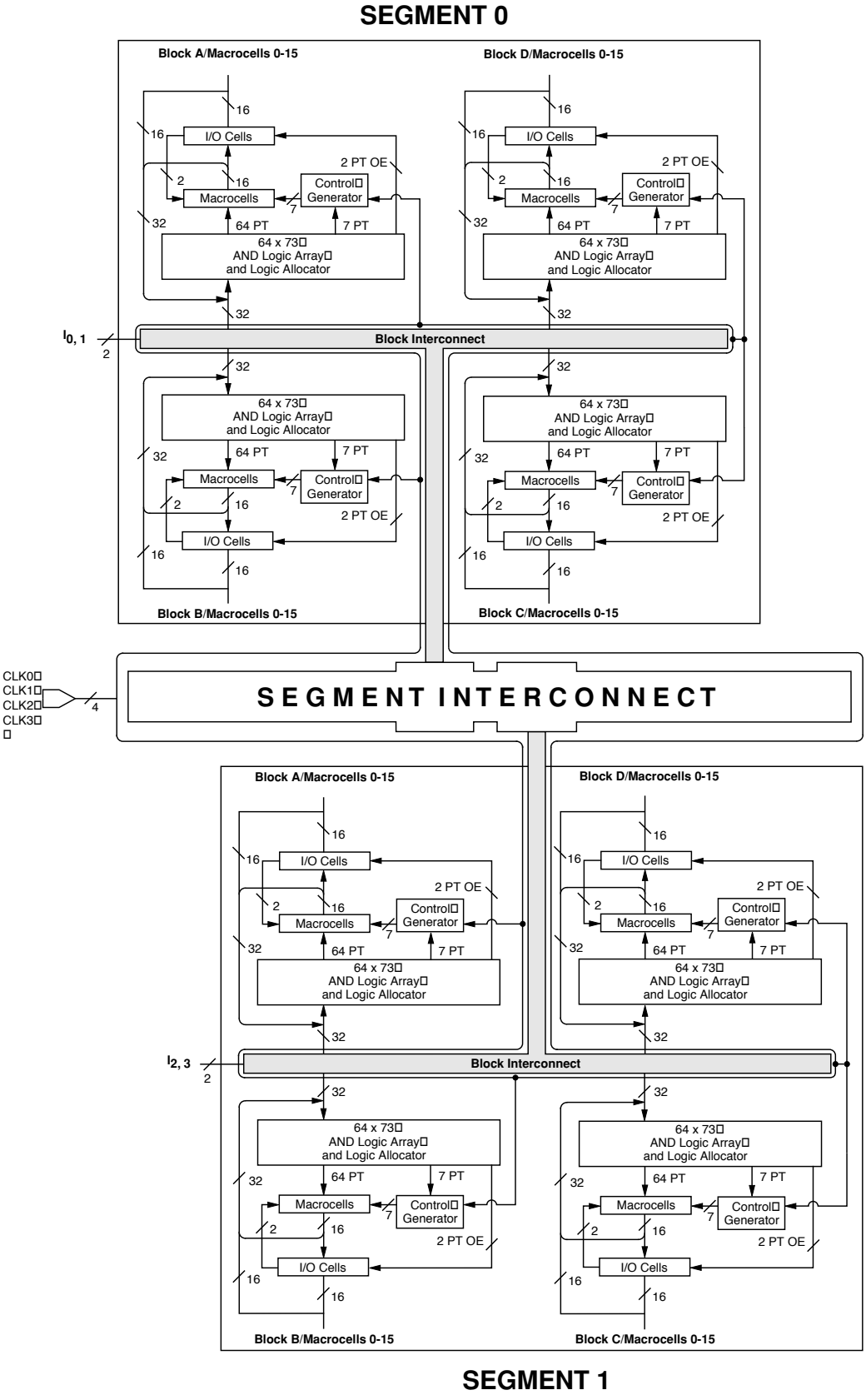
A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

MACH 5 PAL BLOCK



Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-128/XXX



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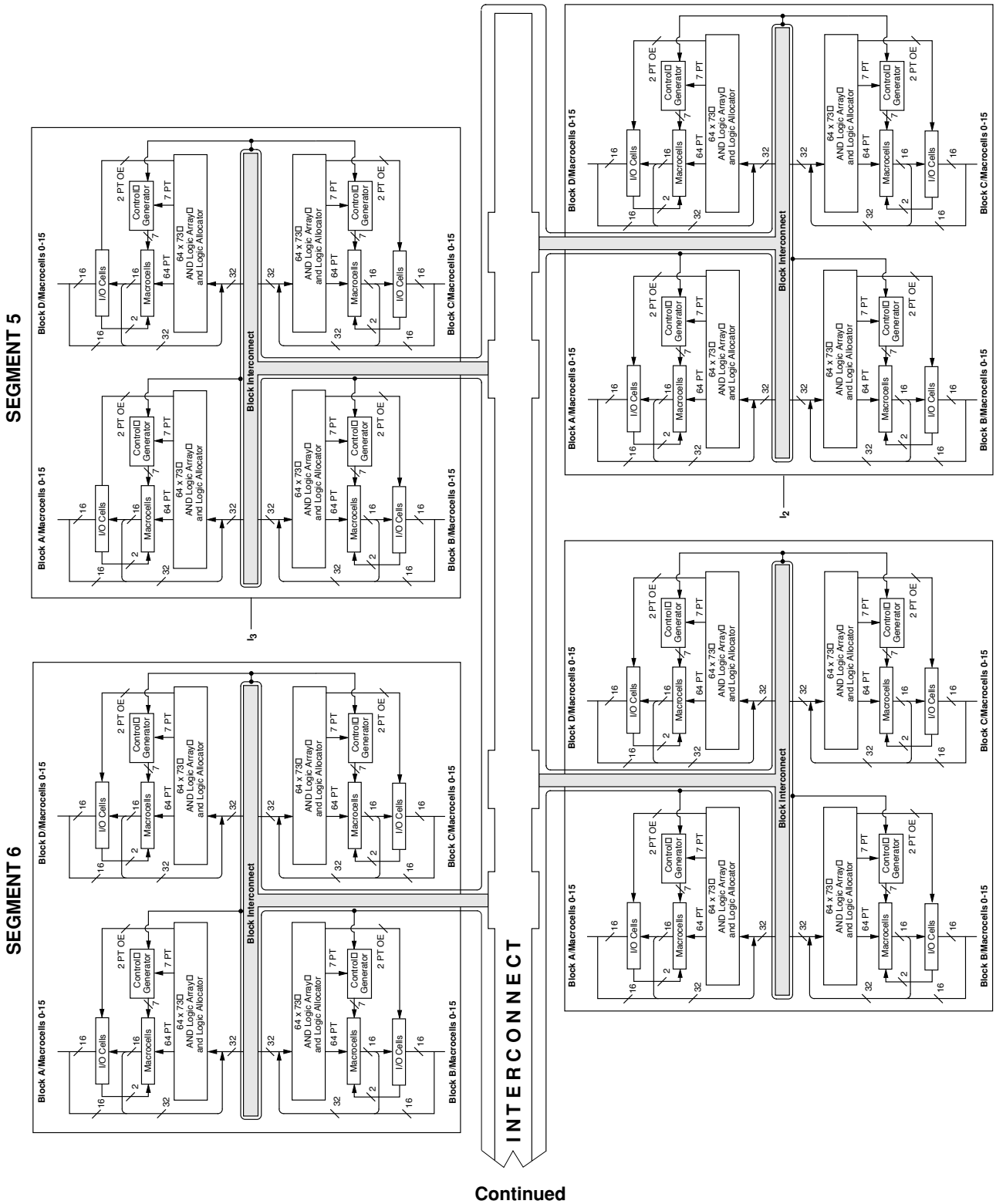
Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-512/XXX



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Select devices have been discontinued.
See Ordering Information section for product status.

ABSOLUTE MAXIMUM RATINGS

M5

Storage Temperature . . . . . -65°C to +150°C

Device Junction
Temperature (Note 1) . . . . . +130°C or +150°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = -100 µA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}		3.3	3.6	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = -2.5 mA, V_{CC} = 5.25 V, V_{IN} = V_{IH} or V_{IL}			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 4)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 5)	-30		-180	mA

Note:

1. *150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.*
2. *Total I_{OL} between ground pins should not exceed 64 mA.*
3. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
5. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*

ABSOLUTE MAXIMUM RATINGS

M5LV

Storage Temperature . . . . . -65°C to +150°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -100 µA	V_{CC} -0.2		V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = 3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 100 µA		0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA (Note 1)		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		-15	-160	mA

Notes:

1. *Total I_{OL} between ground pins should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																
t_{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0		18.0	ns
t_{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:																
t_{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		10.0		ns
t_{SA}	Asynchronous clock setup time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		6.0		6.0		8.0		10.0		13.0		15.0		18.0	ns
t_{COA}	Asynchronous clock to output		8.0		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:																
t_{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0		10.0	ns
t_{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0		12.0	ns
t_{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0		12.0	ns
t_{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:																
t_{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		4.0		ns
t_{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:																
t_{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
t_{PDILi}	Transparent input latch		5.0		5.0		5.5		6.0		6.0		6.0		6.0	ns
Output Delays:																
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns
t_{ER}	Output disable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns

Select devices have been discontinued.
See Ordering Information section for product status.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Power Delays:																
t_{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t_{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t_{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t_{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t_{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t_{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t_{SRi}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t_{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t_{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t_{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t_{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t_{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t_{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																
f_{MAX}	External feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{HS})$	200		167		167		125		100		83.3		83.3		MHz
f_{MAXA}	External feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{HA})$	167		125		125		100		83.3		71.4		62.5		MHz
f_{MAXI}	Maximum input register frequency $1/(t_{SIRS}+t_{HIRS})$ or $1/(2 \times t_{WICW})$	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

1. *See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.*
2. *Numbers in parentheses are for M5-128, M5-192, M5-256.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} =2.0 V	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} =2.0 V	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

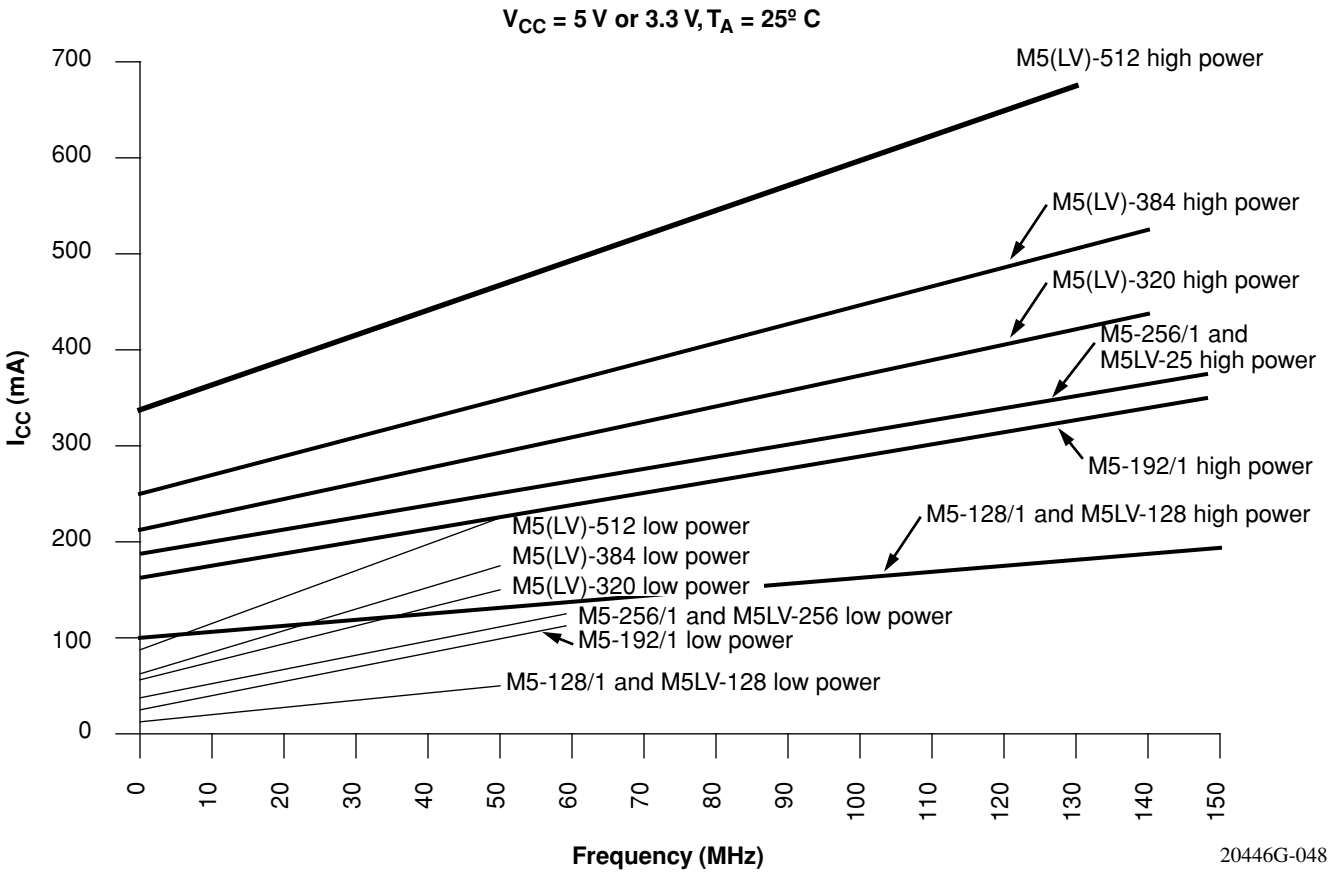


Figure 8. I_{CC} Curves at High/Low Power Modes

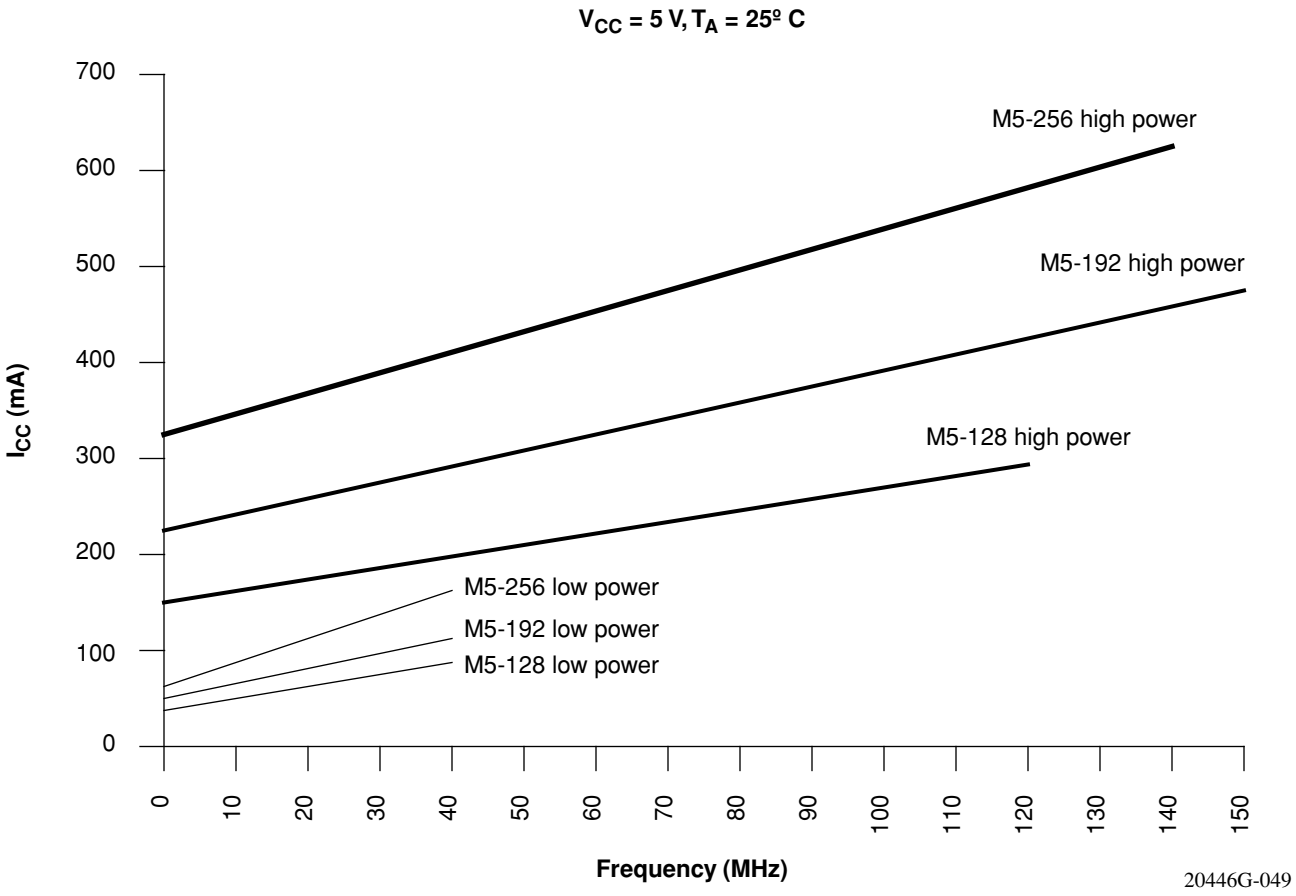
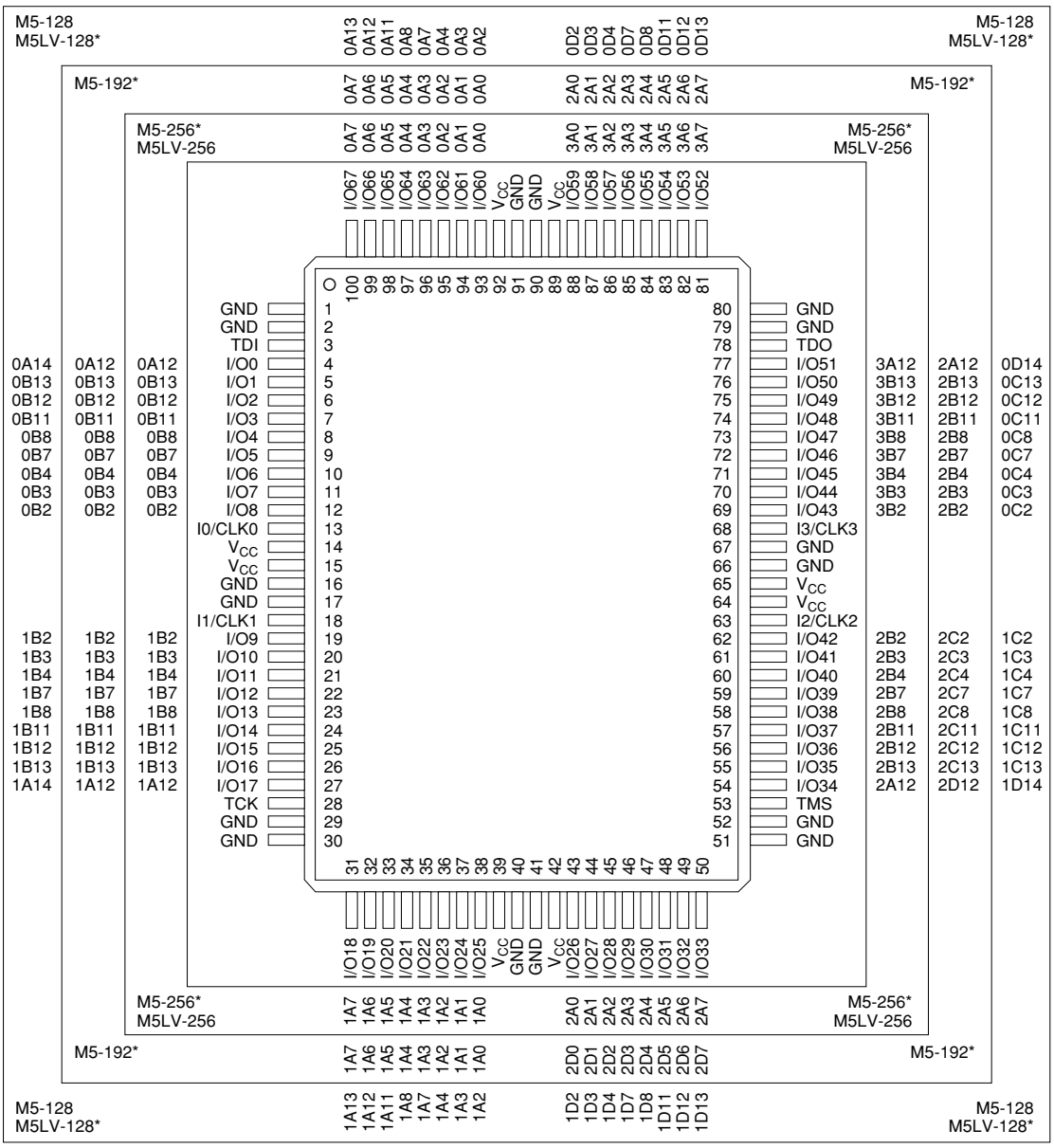


Figure 9. I_{CC} Curves at High/Low Power Modes

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)



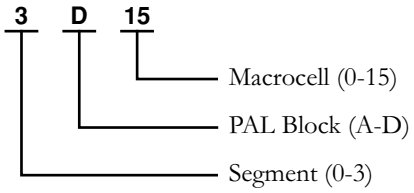
*Package obsolete, contact factory.

20446G-016

Select devices have been discontinued. See Ordering Information section for product status.

Pin Designations

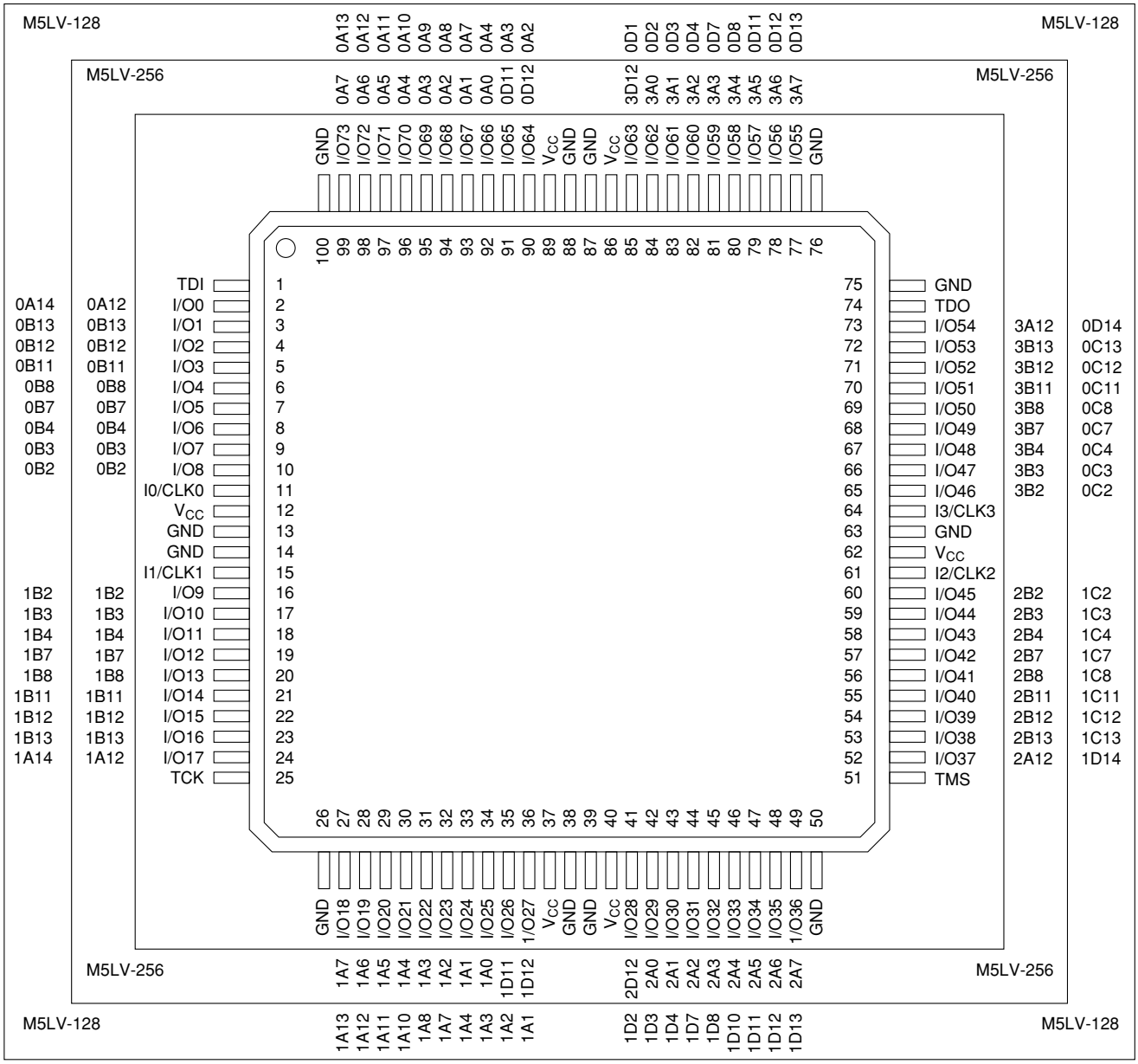
CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)

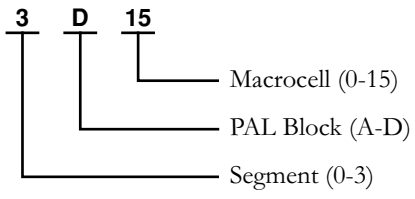


20446G-018

Select devices have been discontinued. See Ordering Information section for product status.

Pin Designations

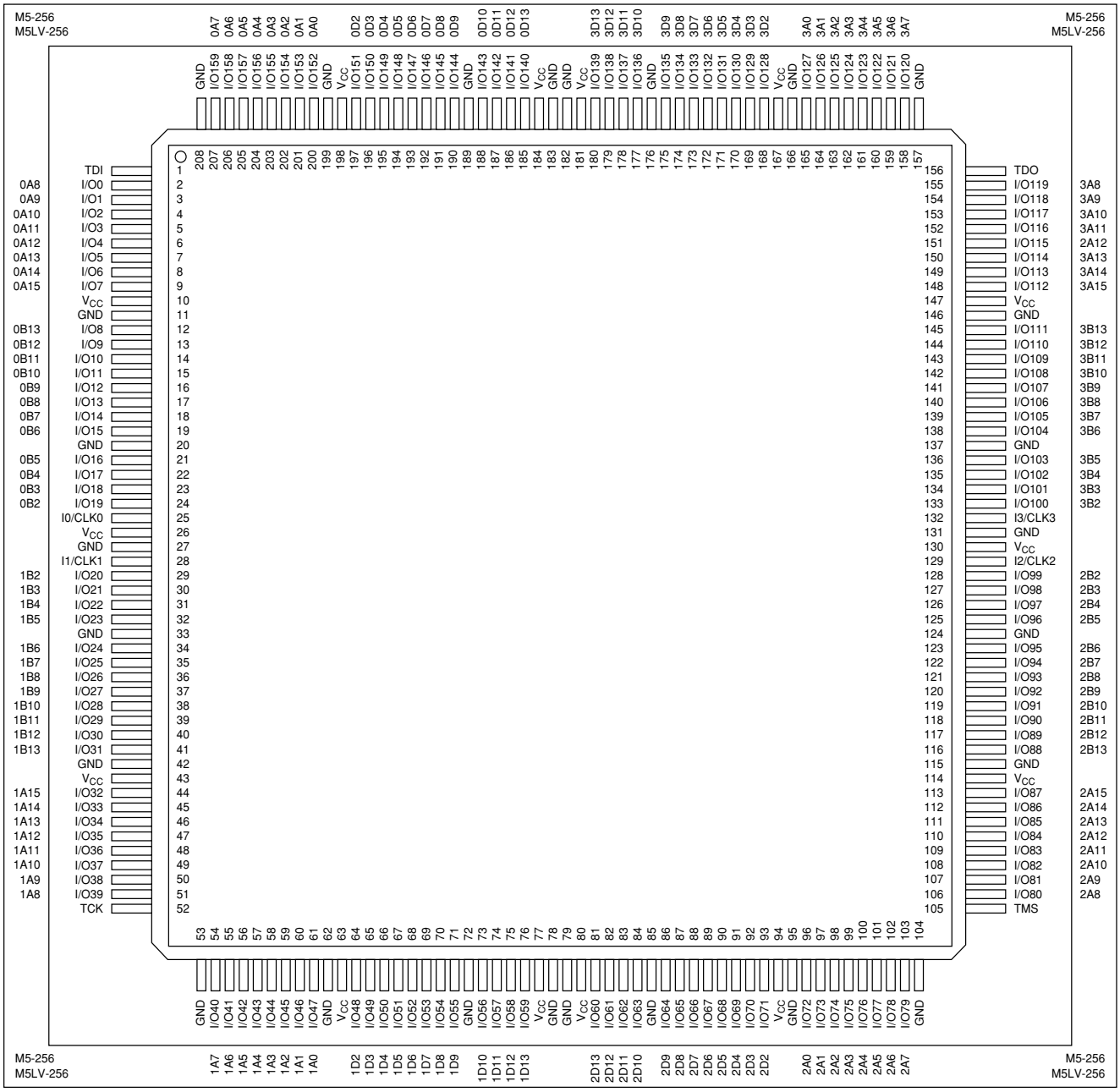
CLK	=	Clock	V_{CC}	=	Supply Voltage		
GND	=	Ground	TDI	=	Test Data In		
I	=	Input	TCK	=	Test Clock		
I/O	=	Input/Output	TMS	=	Test Mode Select		
NC	=	No Connect	TDO	=	Test Data Out		



208-PIN PQFP CONNECTION DIAGRAM

Top View

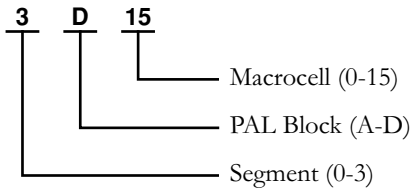
208-Pin PQFP (256 Macrocells)



20446G-023

Pin Designations

CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



Select devices have been discontinued. See Ordering Information section for product status.

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (Macrocell Association)

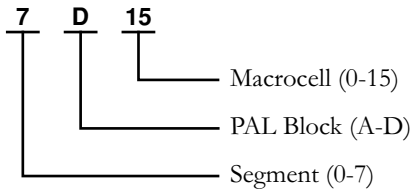
352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	I3/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	NC	1
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	GND	2
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I2/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	3
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V_{CC}	5A11	V_{CC}	5D12	5D7	5D2	V_{CC}	4D3	4D8	4D12	V_{CC}	4A11	V_{CC}	4A4	4A0	V_{CC}	3A15	3A13	3A12	4
5	GND	6A12	6A13	V_{CC}																			3A14	3A11	3A9	GND	5
6	NC	6A9	6A10	6A15																			3A10	3A8	3A7	3A5	6
7	GND	6A6	6A8	6A11																			3A6	3A4	3A3	3A0	7
8	6A1	6A4	6A5	6A7																			3A2	3A1	3B0	NC	8
9	6B1	6A0	6A2	6A3																			V_{CC}	3B1	3B2	GND	9
10	GND	6B2	6B0	V_{CC}																			3B3	3B4	3B5	3B6	10
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	3B10	11
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B14	12
13	6B14	6B13	6B12	6B11																			V_{CC}	2B15	3B15	GND	13
14	GND	7B15	6B15	V_{CC}																			2B11	2B12	2B13	2B14	14
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10	15
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6	16
17	7B7	7B6	7B5	7B4																			V_{CC}	2B0	2B2	GND	17
18	GND	7B3	7B2	V_{CC}																			2A3	2A2	2A0	2B1	18
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1	19
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND	20
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC	21
22	GND	7A9	7A11	7A15																			V_{CC}	2A13	2A12	GND	22
23	7A10	7A13	7A14	V_{CC}	0A0	0A4	V_{CC}	0A11	V_{CC}	0D12	0D8	0D3	V_{CC}	1D2	1D7	1D12	V_{CC}	1A11	V_{CC}	1A6	1A3	1A0	TCK	NC	2A14	NC	23
24	NC	NC	TDI	0A2	0A5	0A7	0A10	0A14	0D14	0D11	0D7	0D4	I0/CLK0	1D1	1D5	1D9	1D14	1A13	1A10	1A8	1A7	1A4	1A1	NC	GND	GND	24
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D13	0D10	0D6	0D2	0D0	1D0	1D4	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	25
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	I1/CLK1	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	26
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

20446G-031

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



Select devices have been discontinued.
See Ordering Information section for product status.