



Welcome to [E·XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	74
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-256-74-12vc

Table 2. MACH 5 Speed Grades

Device	Speed Grade ¹						
	-5	-6	-7	-10	-12	-15	-20
M5-128 ²			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C, I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256 ²			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	C, I	I

Note:

1. C = Commercial grade, I = Industrial grade
2. /1 version recommended for new designs

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL[®] block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options ¹

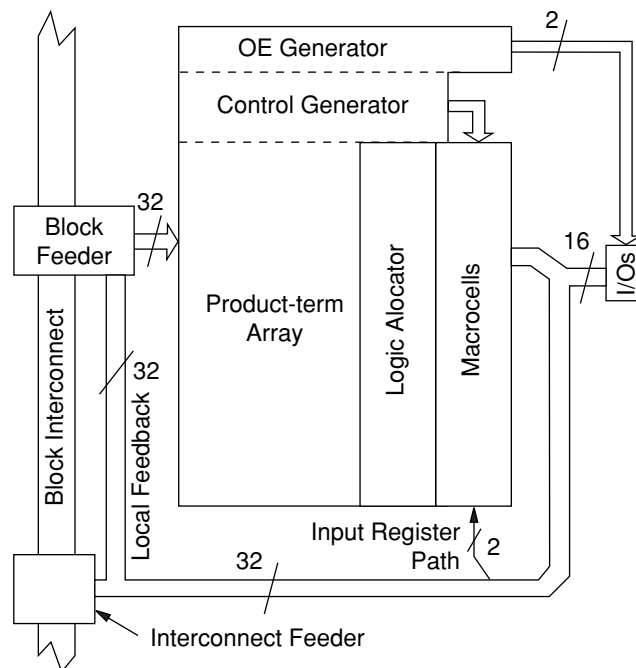
Supply Voltage	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
	5	3.3		5	3.3	5	3.3	5	3.3	5	3.3
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

Note:

1. The I/O options indicated with a "*" are obsolete, please contact factory for more information.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued.
See Ordering Information section for product status.



20446G-002

Figure 2. PAL Block Structure

Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 or 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 4. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂ , C ₃ , C ₄	M ₈	C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₁	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅	M ₉	C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₂	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆	M ₁₀	C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₃	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₁	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₄	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₂	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₅	C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈	M ₁₃	C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉	M ₁₄	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀	M ₁₅	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅

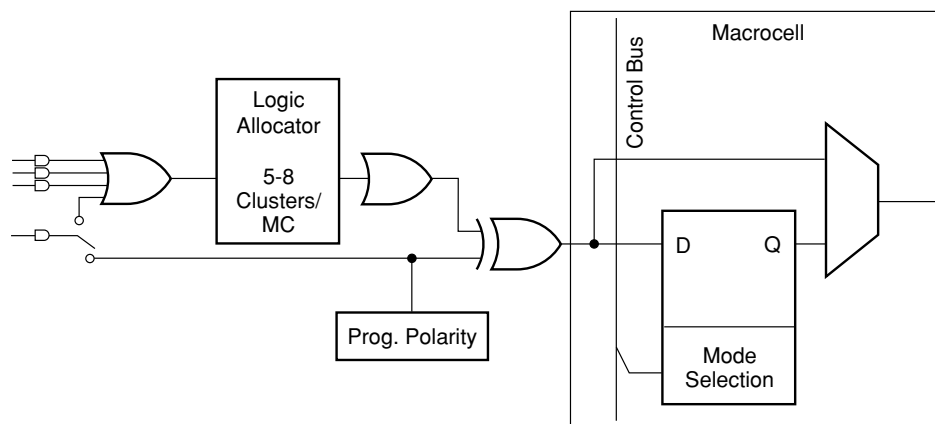
Select devices have been discontinued.
See Ordering Information section for product status.

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ($A*B*C$)
- ◆ Sum-term clock ($A+B+C$)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.
See Ordering Information section for product status.

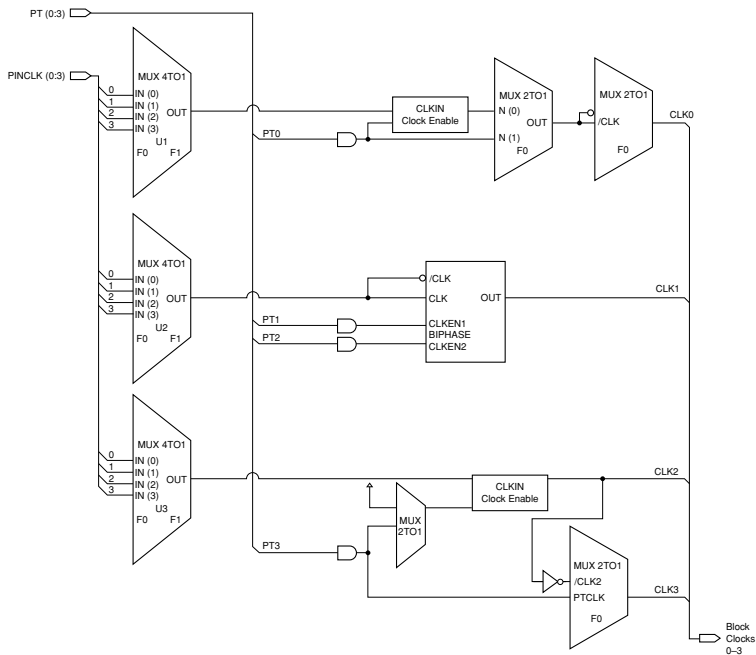
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

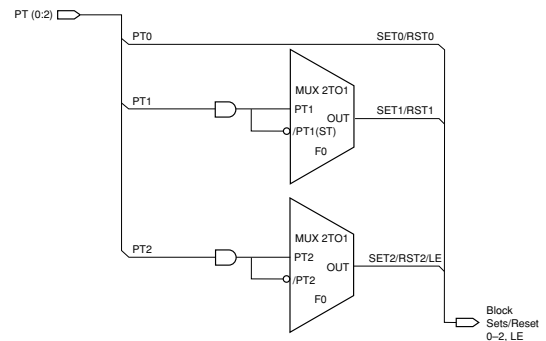
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator



20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.
See Ordering Information section for product status.**

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

Select devices have been discontinued. See Ordering Information section for product status.

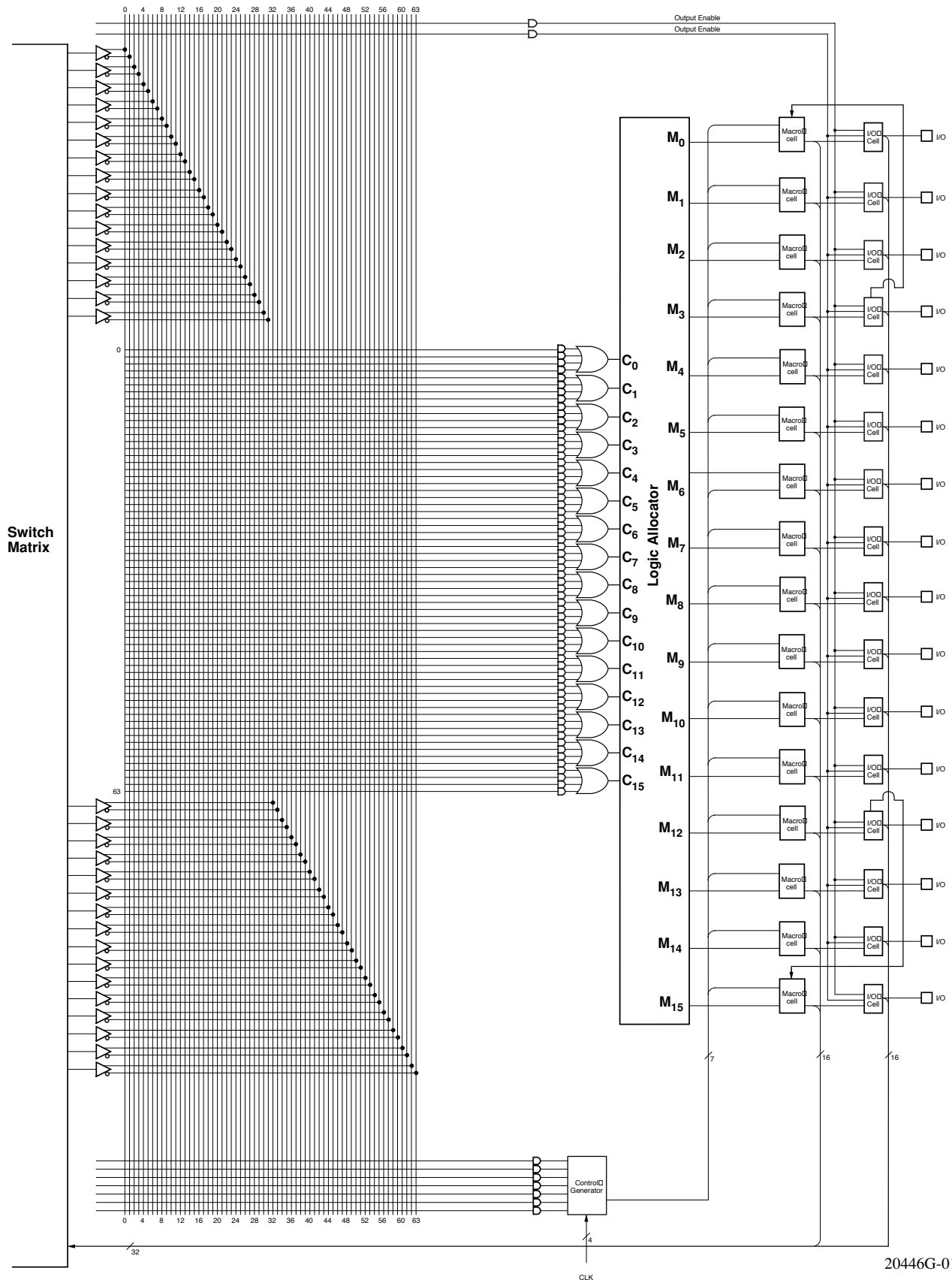


SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

**Select devices have been discontinued.
See Ordering Information section for product status.**

MACH 5 PAL BLOCK

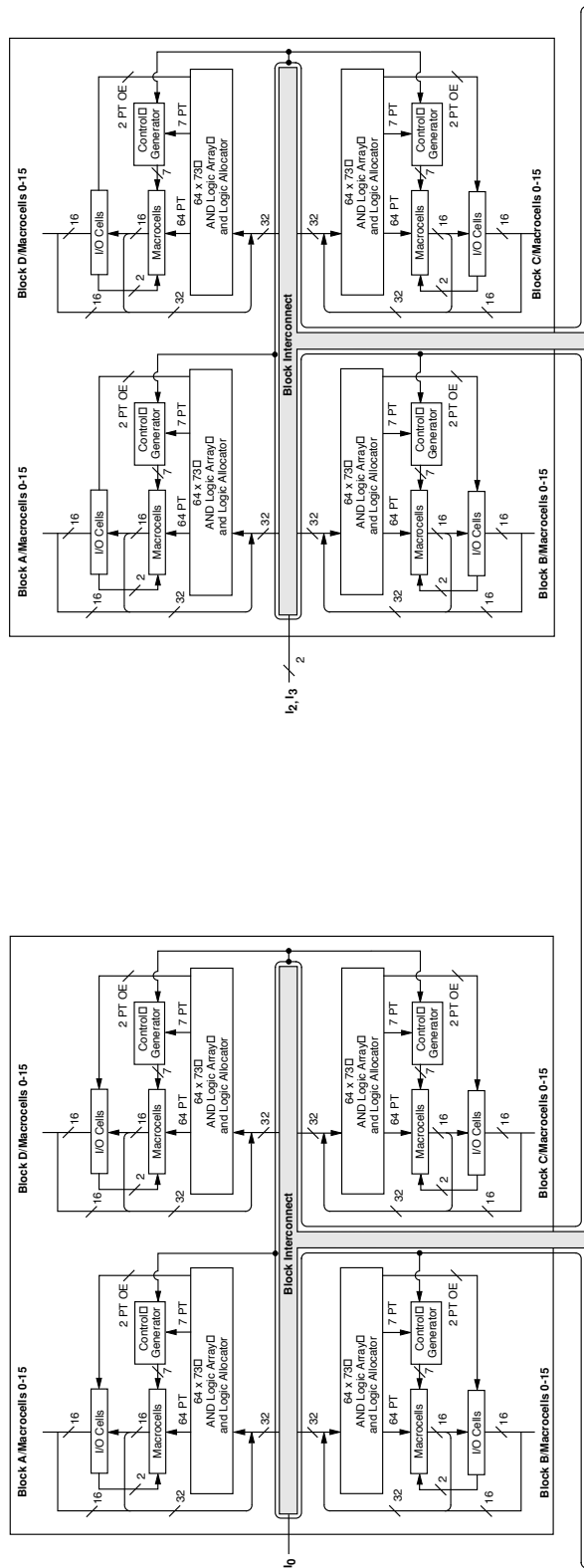


Select devices have been discontinued.
See Ordering Information section for product status.

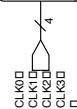
20446G-015

BLOCK DIAGRAM — M5-192/XXX

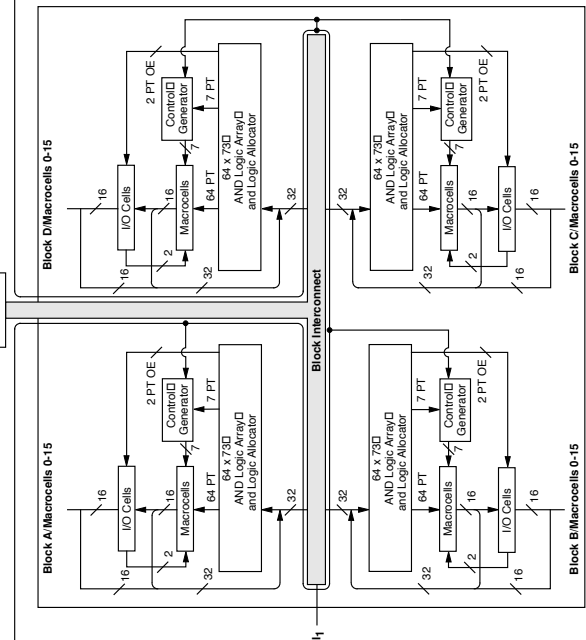
SEGMENT 2



SEGMENT INTERCONNECT



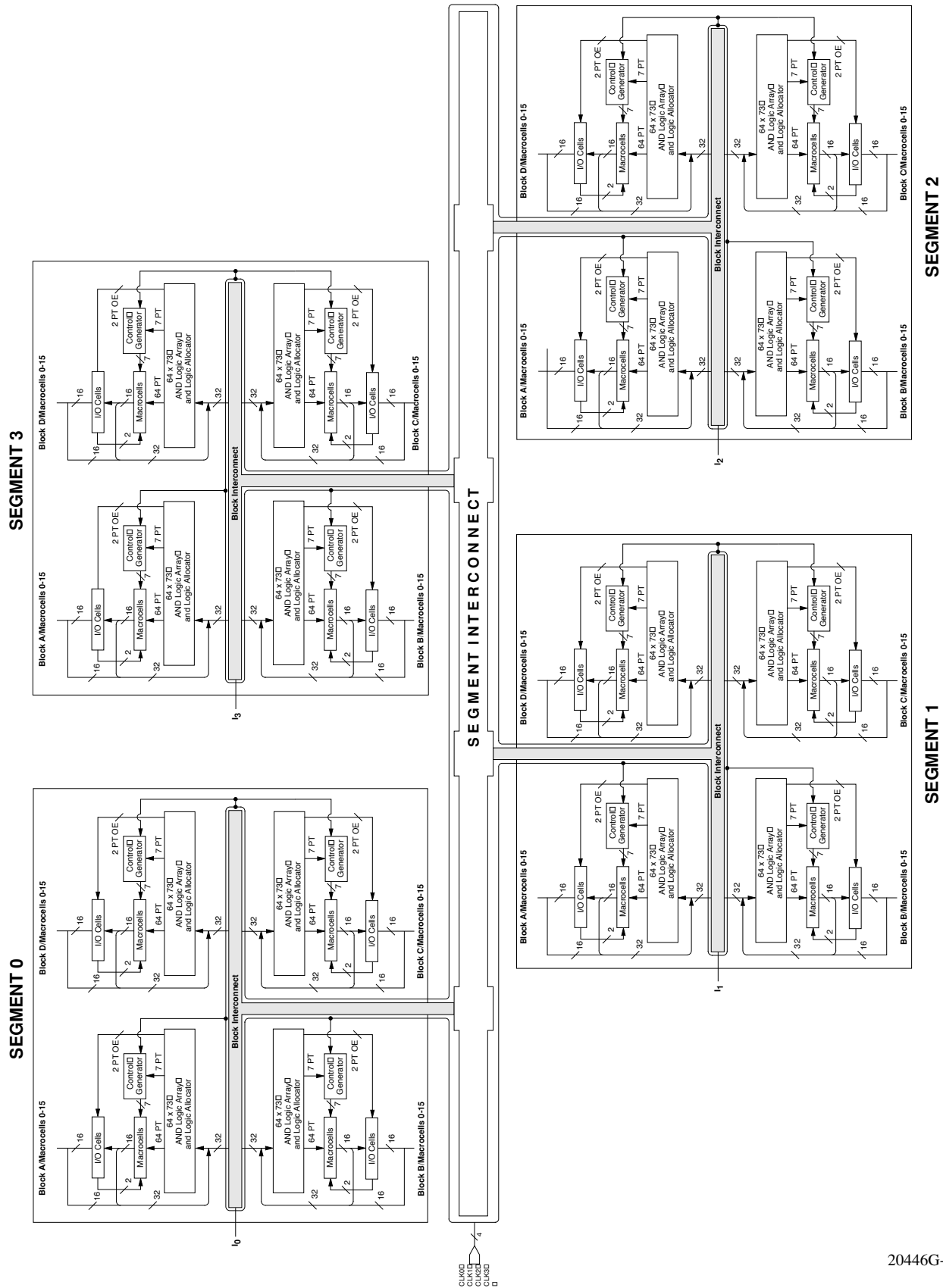
SEGMENT 1



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-008

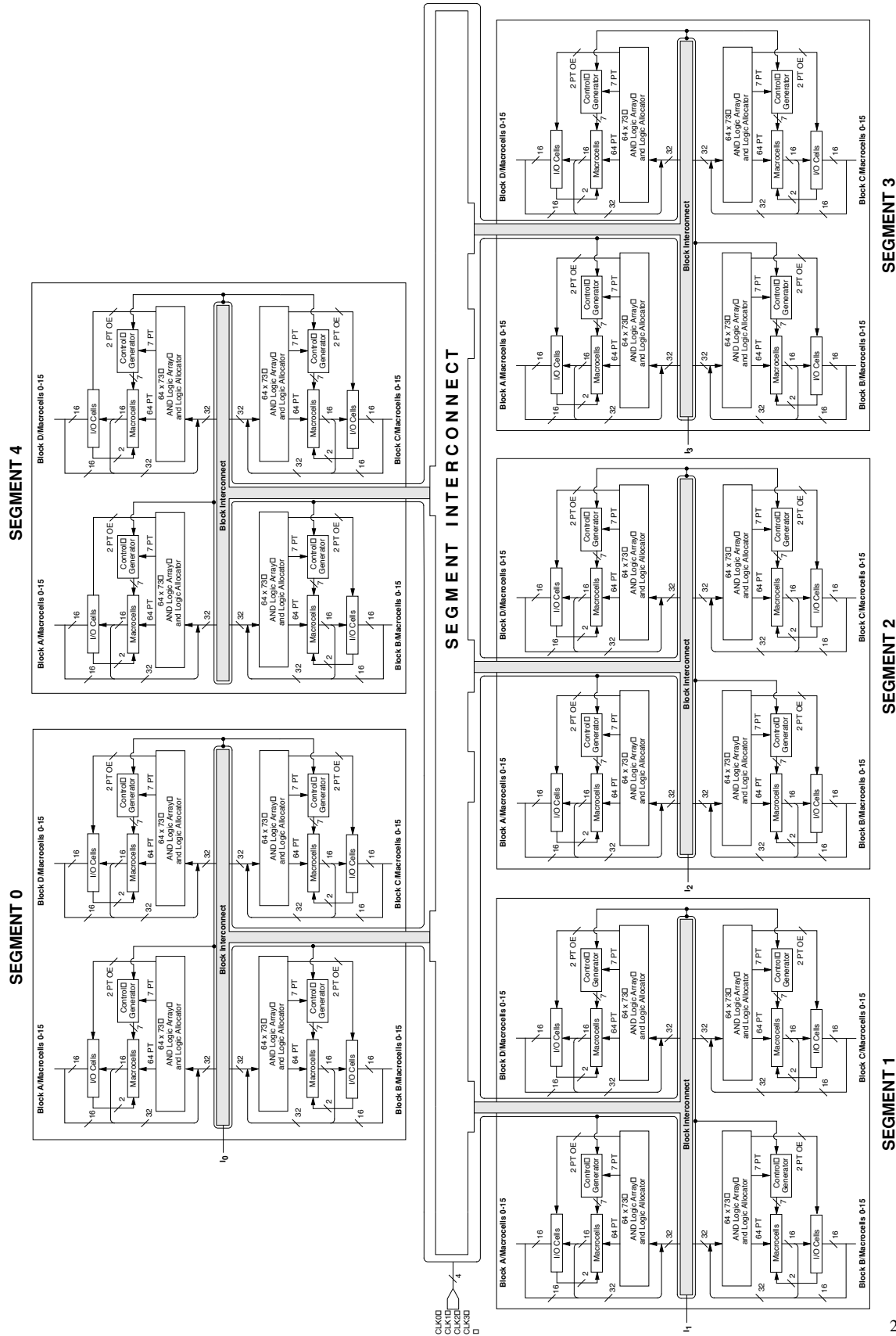
BLOCK DIAGRAM — M5(LV)-256/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-009

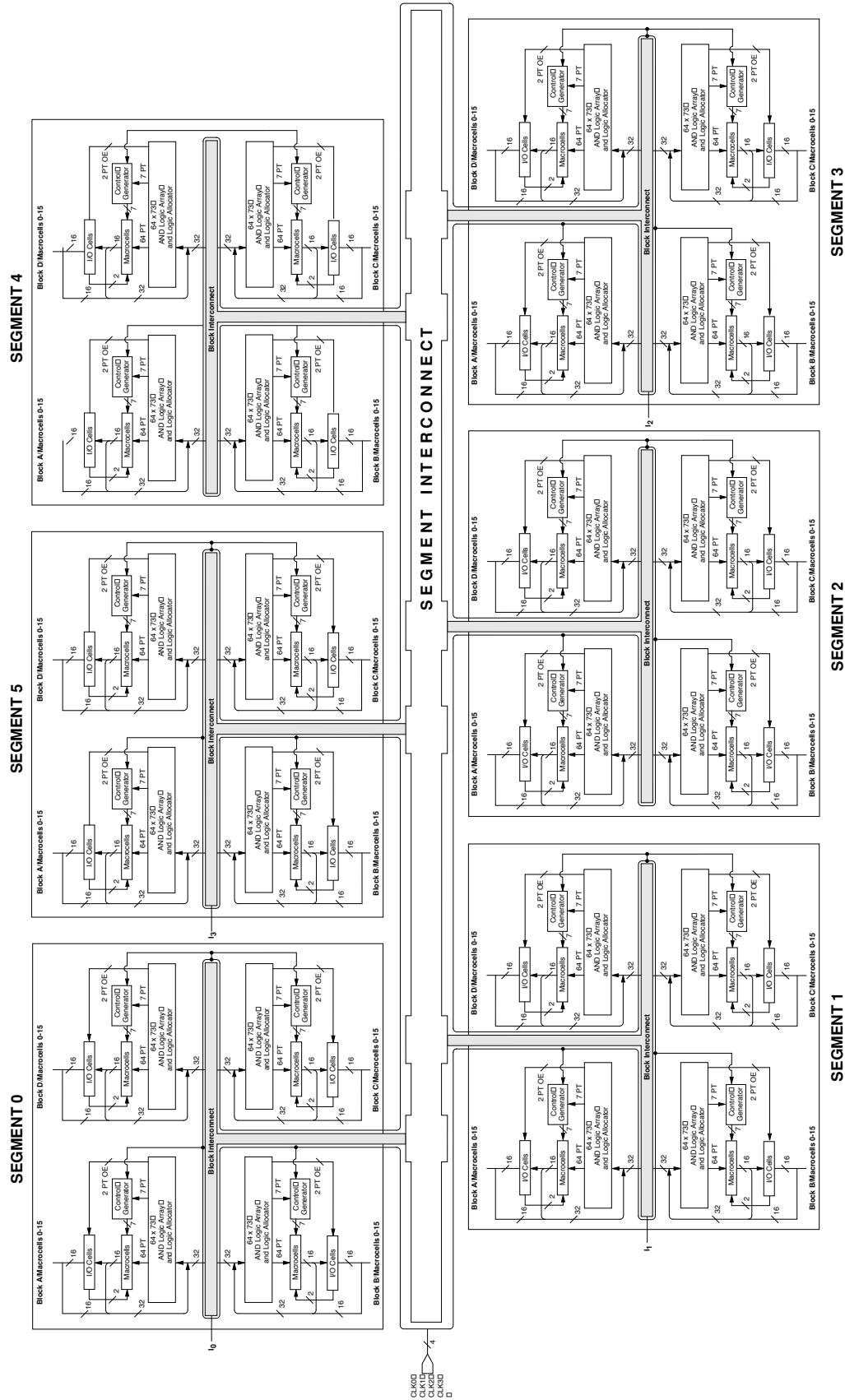
BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-010

BLOCK DIAGRAM — M5(LV)-384/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-011

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	$V_{IN} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	$V_{OUT} = 2.0 \text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

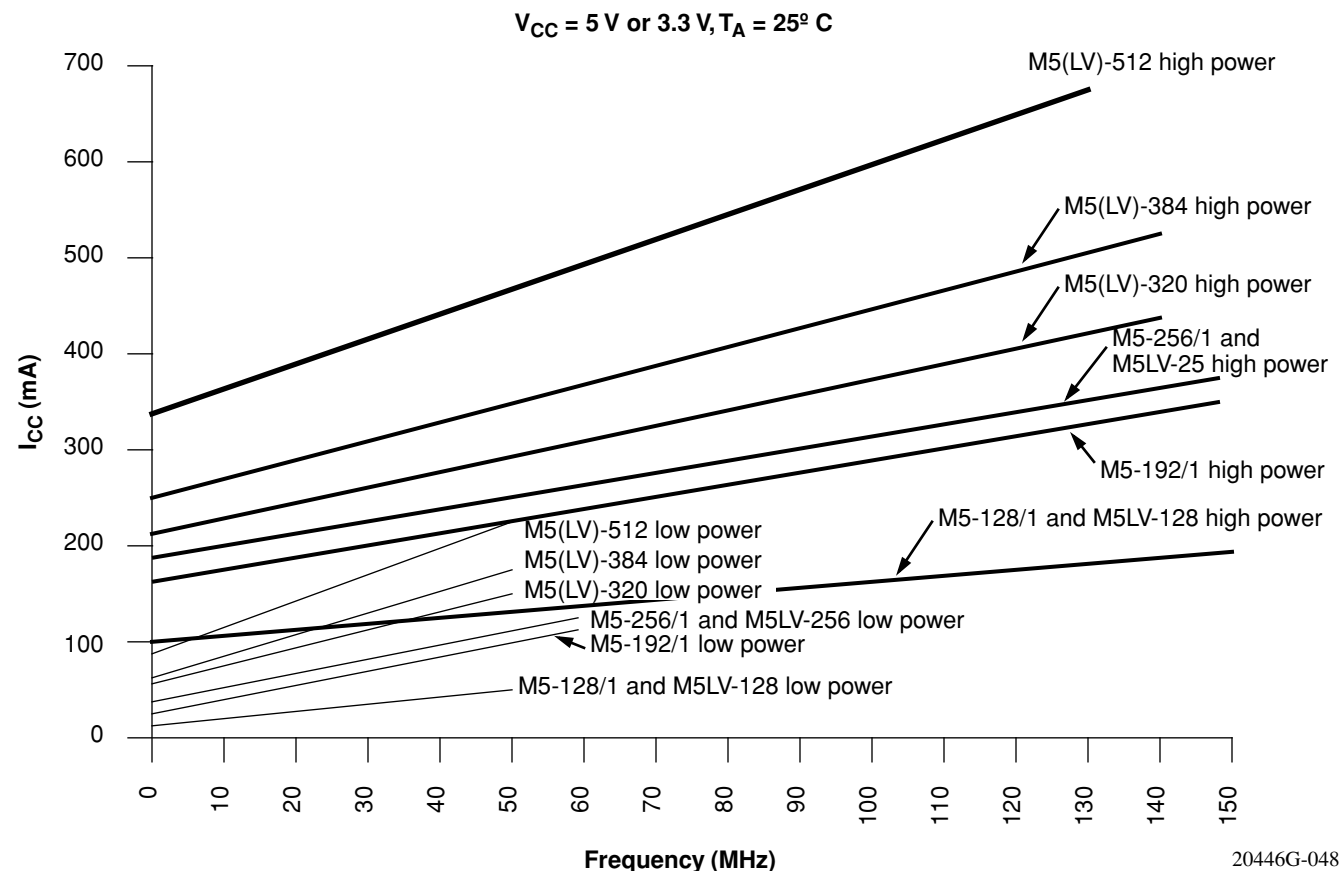


Figure 8. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

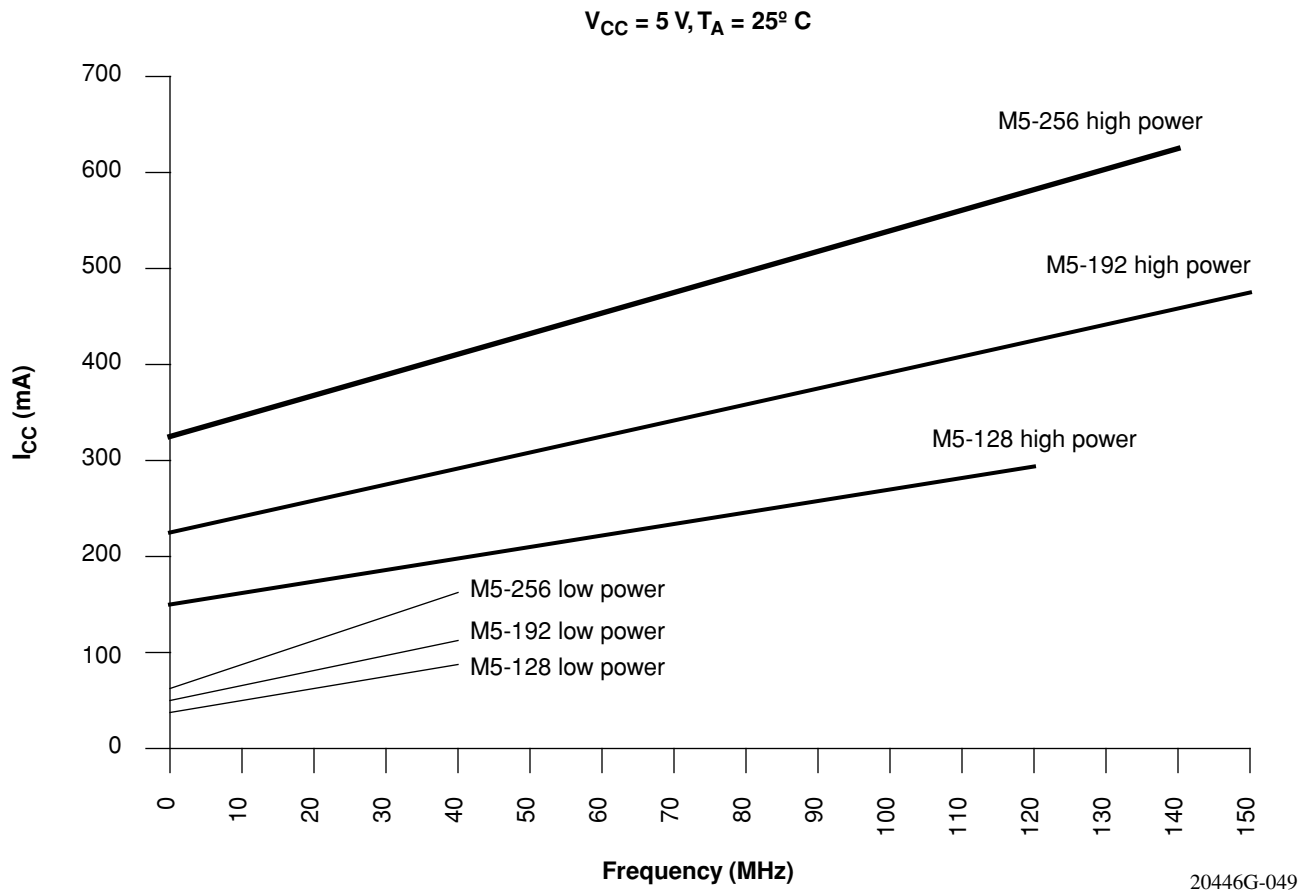


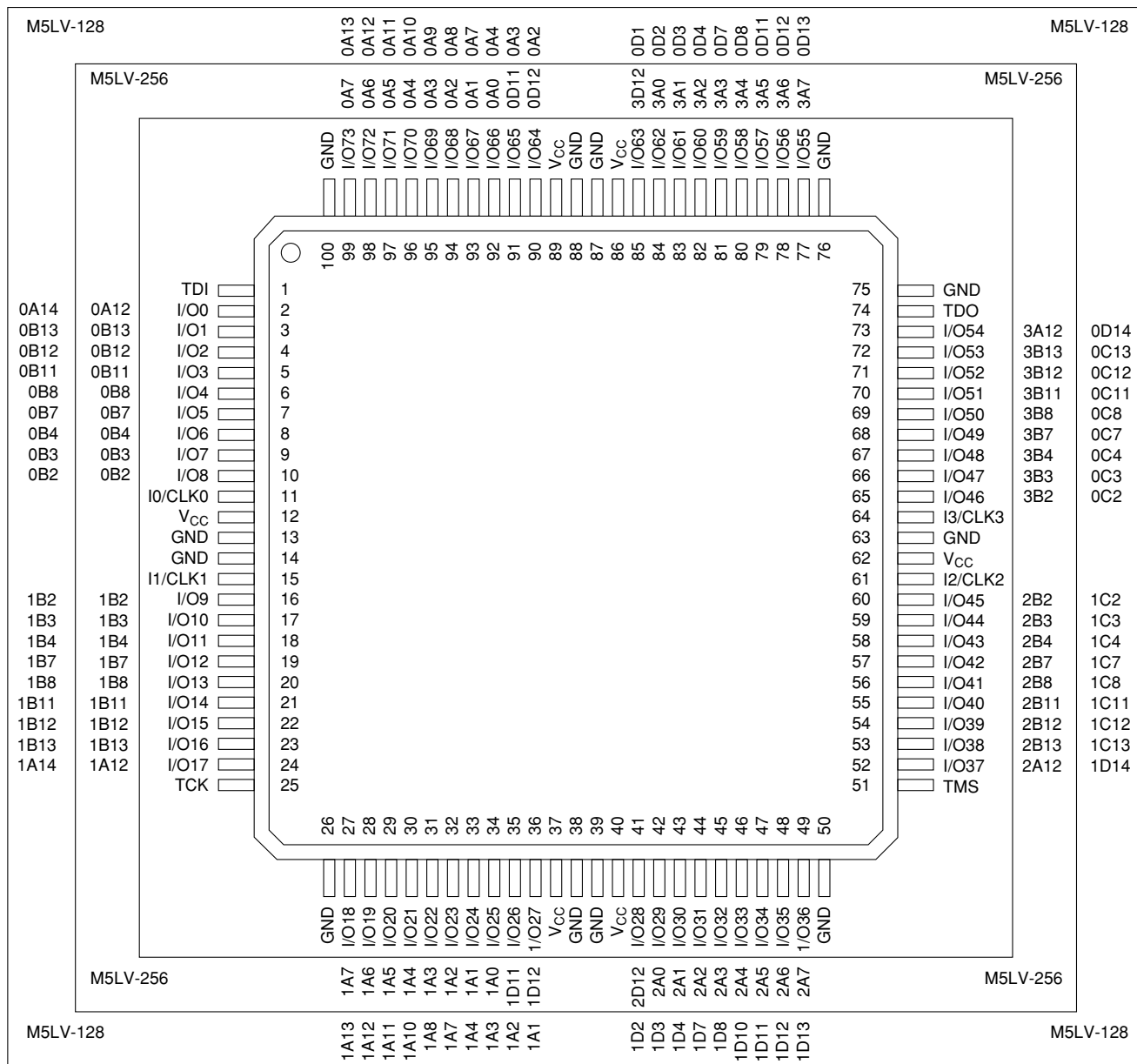
Figure 9. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued.
See Ordering Information section for product status.

100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)



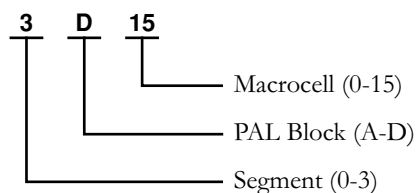
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-018

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

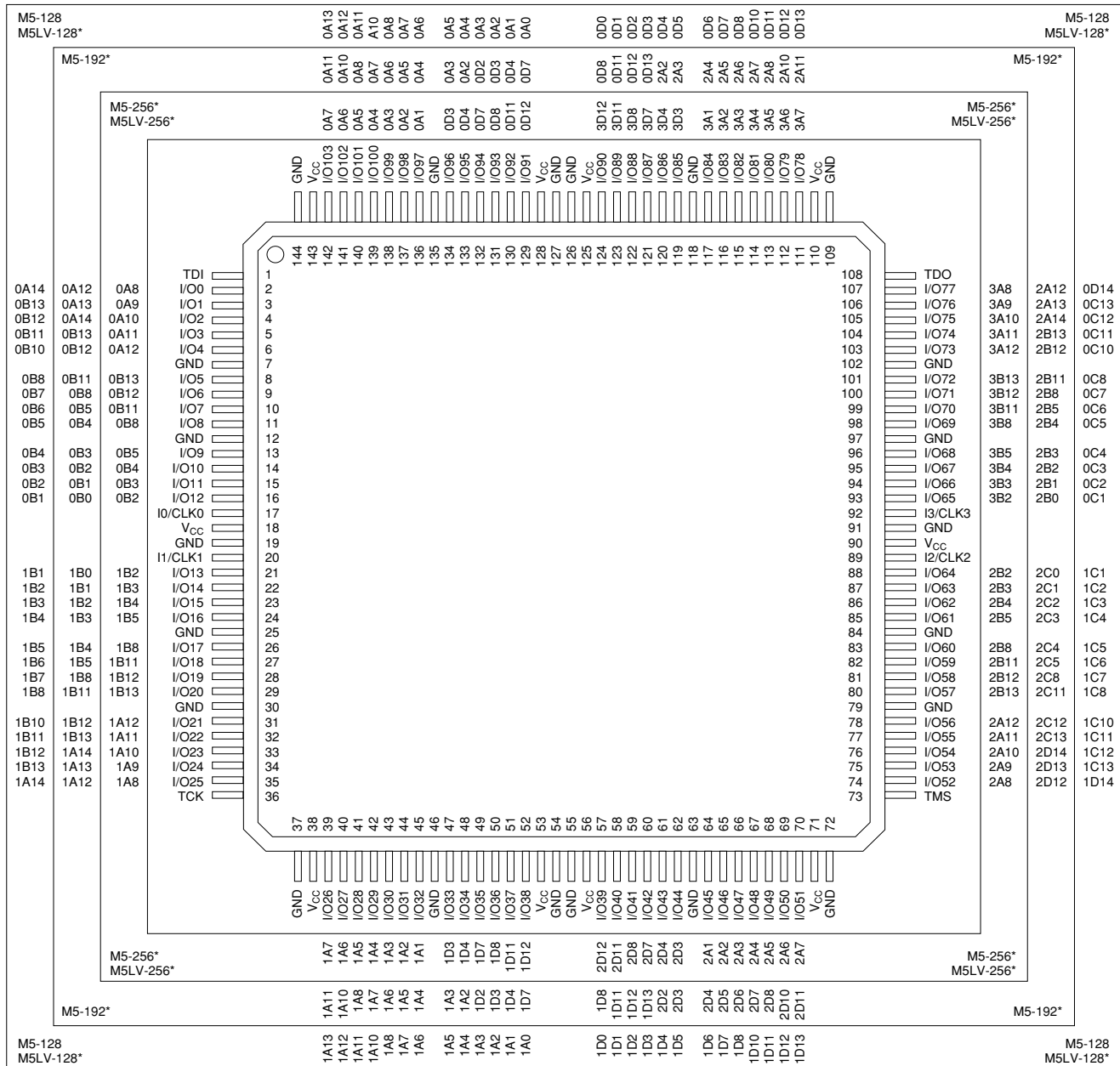
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



144-PIN PQFP CONNECTION DIAGRAM

Top View

144-Pin PQFP



**Select devices have been discontinued.
See Ordering Information section for product status.**

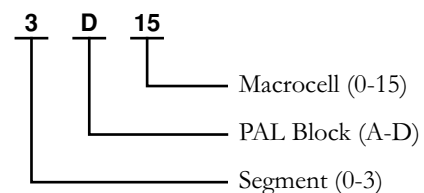
*Package obsolete, contact factory.

20446G-019

Pin Designations

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 NC = No Connect

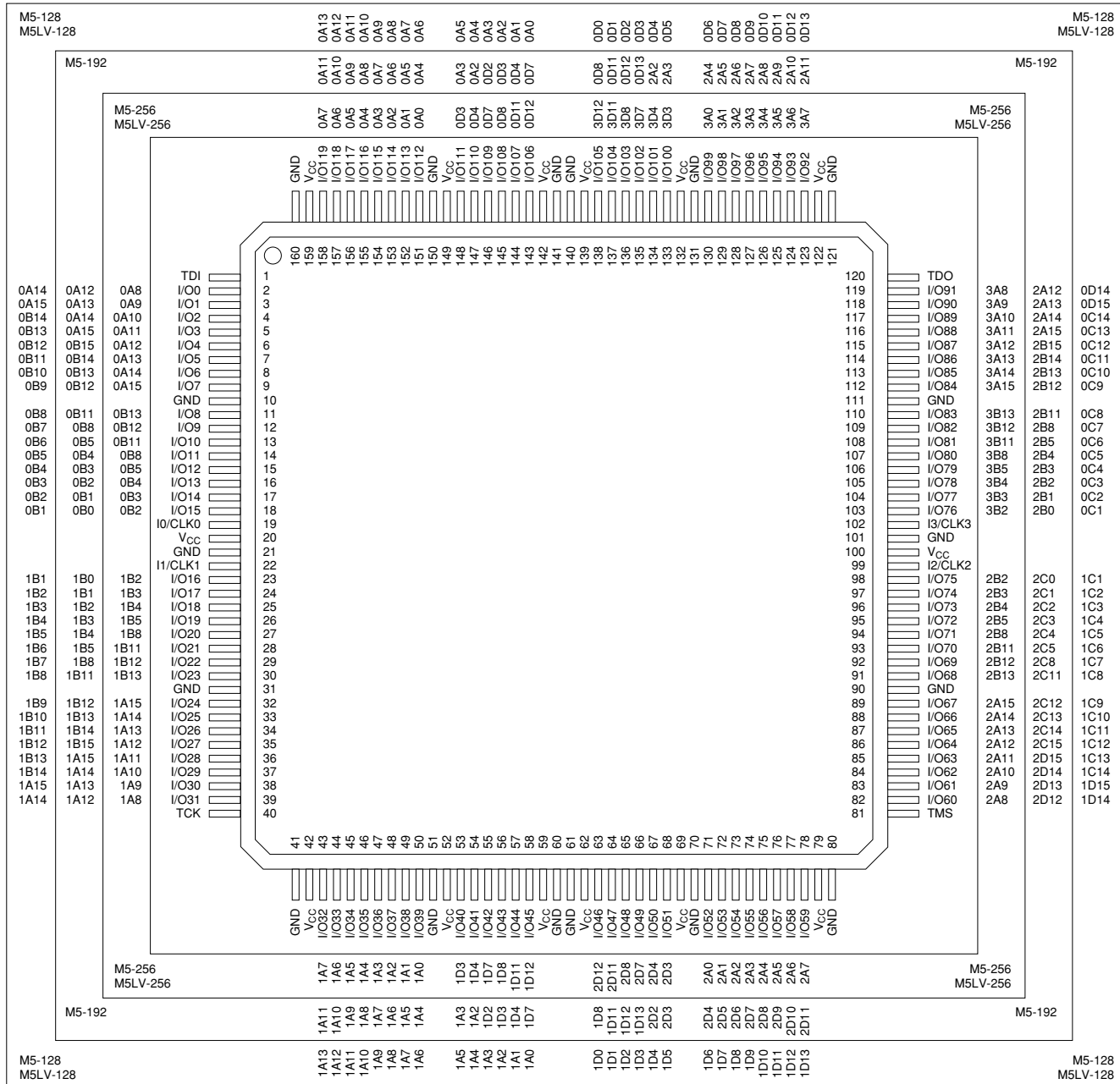
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)



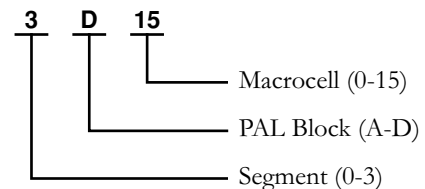
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-021

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

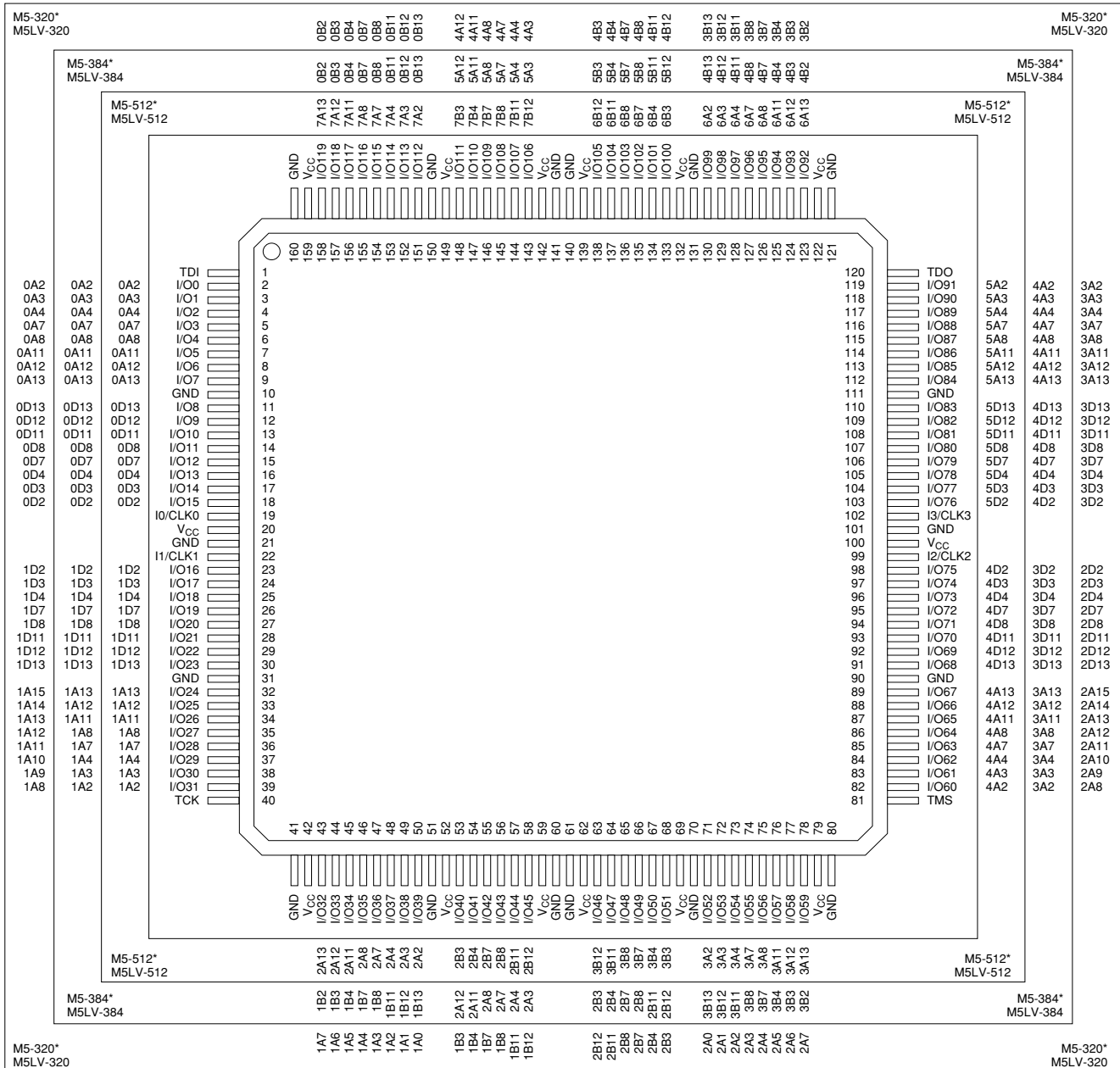
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

160-Pin PQFP (320, 384, 512 Macrocells)

Select devices have been discontinued.
See Ordering Information section for product status.



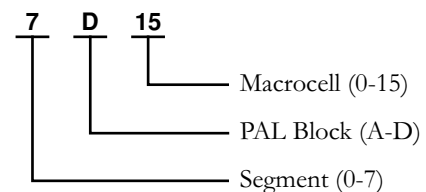
*Package obsolete, contact factory.

20446G-022

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (I/O Pin-outs)

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11	GND	I/O44	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	A
B	GND	I/O12	I/O28	I/O45	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	B
C	I/O0	I/O13	V _{CC}	I/O46	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V _{CC}	I/O165	I/O181	C
D	I/O1	I/O14	I/O29	V _{CC}	V _{CC}	I/O66	V _{CC}	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V _{CC}	I/O124	V _{CC}	V _{CC}	I/O149	I/O166	I/O182	D
E	I/O2	I/O15	I/O30	TDI													TDO	I/O150	I/O167	I/O183	E
F	GND	I/O16	I/O31	I/O47													I/O137	I/O151	I/O168	GND	F
G	I/O3	I/O17	I/O32	V _{CC}													V _{CC}	I/O152	I/O169	I/O184	G
H	GND	I/O18	I/O33	I/O48													I/O138	I/O153	I/O170	GND	H
J	I/O4	I/O19	I/O34	I/O49													I/O139	I/O154	I/O171	I/O185	J
K	GND	I/O20	I/O35	I/O50													I/O140	I/O155	I/O172	I/O186	K
L	I/O5	I/O21	I/O36	I/O51													I/O141	I/O156	I/O173	GND	L
M	I/O6	I/O22	I/O37	I/O52													I/O142	I/O157	I/O174	I/O187	M
N	GND	I/O23	I/O38	I/O53													I/O143	I/O158	I/O175	GND	N
P	I/O7	I/O24	I/O39	V _{CC}													V _{CC}	I/O159	I/O176	I/O188	P
R	GND	I/O25	I/O40	I/O54													I/O144	I/O160	I/O177	GND	R
T	I/O8	I/O26	I/O41	TCK													TMS	I/O161	I/O178	I/O189	T
U	I/O9	I/O27	I/O42	V _{CC}													V _{CC}	I/O162	I/O179	I/O190	U
V	I/O10	I/O28	V _{CC}	I/O55													I/O145	V _{CC}	I/O180	I/O191	V
W	GND	I/O29	I/O43	I/O56													I/O146	I/O163	I/O181	GND	W
Y	GND	I/O30	GND	I/O57													I/O147	GND	I/O182	I/O192	Y

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

Select devices have been discontinued.
See Ordering Information section for product status.

20446G-026

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I/O233 I ₃ /CLK ₃	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O224	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	NC
3	GND	GND	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I/O211	I/O212	I/O213	I/O214	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	TMS	NC	NC	NC
4	NC	I/O188	NC	TDO	I/O189	I/O190	I/O191	V _{CC}	I/O192	V _{CC}	I/O193	I/O194	I/O195	V _{CC}	I/O196	I/O197	I/O198	V _{CC}	I/O199	V _{CC}	I/O200	I/O201	V _{CC}	I/O202	I/O203	I/O204
5	GND	I/O183	I/O184	V _{CC}																			I/O185	I/O186	I/O187	GND
6	NC	I/O176	I/O177	I/O178																			I/O179	I/O180	I/O181	I/O182
7	GND	I/O169	I/O170	I/O171																			I/O172	I/O173	I/O174	I/O175
8	I/O162	I/O163	I/O164	I/O165																			I/O166	I/O167	I/O168	NC
9	I/O156	I/O157	I/O158	I/O159																			V _{CC}	I/O160	I/O161	GND
10	GND	I/O150	I/O151	V _{CC}																			I/O152	I/O153	I/O154	I/O155
11	I/O142	I/O143	I/O144	I/O145																			I/O146	I/O147	I/O148	I/O149
12	I/O134	I/O135	I/O136	I/O137																			I/O138	I/O139	I/O140	I/O141
13	I/O128	I/O129	I/O130	I/O131																			V _{CC}	I/O132	I/O133	GND
14	GND	I/O122	I/O123	V _{CC}																			I/O124	I/O125	I/O126	I/O127
15	I/O114	I/O115	I/O116	I/O117																			I/O118	I/O119	I/O120	I/O121
16	NC	I/O107	I/O108	I/O109																			I/O110	I/O111	I/O112	I/O113
17	I/O101	I/O102	I/O103	I/O104																			V _{CC}	I/O105	I/O106	GND
18	GND	I/O87	I/O88	V _{CC}																			I/O97	I/O98	I/O99	I/O100
19	I/O80	I/O81	I/O82	I/O83																			I/O91	I/O92	I/O93	I/O94
20	I/O73	I/O74	I/O75	I/O76																			I/O84	I/O85	I/O86	GND
21	GND	I/O68	I/O69	I/O70																			I/O77	I/O78	I/O79	NC
22																							V _{CC}	I/O71	I/O72	GND
23	I/O51	I/O52	I/O53	V _{CC}	I/O54	I/O55	V _{CC}	I/O56	V _{CC}	I/O57	I/O58	I/O59	V _{CC}	I/O60	I/O61	I/O62	V _{CC}	I/O63	V _{CC}	I/O64	I/O65	I/O66	TCK	NC	I/O67	NC
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	NC	NC	GND	GND
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	NC	NC	NC
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	NC	GND	NC	NC	NC

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

20446G-030

Select devices have been discontinued.
See Ordering Information section for product status.

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

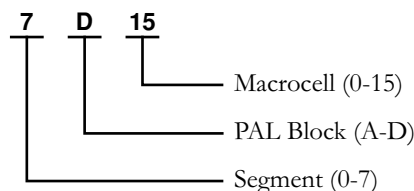
Bottom View (Macrocell Association)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF					
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	13/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	1					
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	NC	2				
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	12/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	3				
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A15	3A13	3A12	4				
5	GND	6A12	6A13	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 7 D 15 Segment (0-7) Macrocell (0-15) PAL Block (A-D)	3A14	3A10	3A6	3A2	V _{CC}	3B3	3B7	3B11	3B14	2B11	2B7	2B3	V _{CC}	2A3	2A7	2A11	2A5	2A1	GND	2A15	V _{CC}	TCK	NC	GND	NC	5
6	NC	6A9	6A10	6A15		3A10	3A8	3A4	3A1	3B1	3B4	3B8	3B12	3B15	2B12	2B8	2B4	2B0	2A8	2A5	2A1	2A15	2A13	2A10	2A12	2A14	2A6	6			
7	GND	6A6	6A8	6A11		3A6	3A4	3A3	3B0	3B2	3B5	3B9	3B13	3B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	7			
8	6A1	6A4	6A5	6A7		3A2	3A1	3B0	3B2	GND	3B6	3B10	3B14	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	8			
9	6B1	6A0	6A2	6A3		V _{CC}	3B1	3B5	3B2	GND	3B6	3B10	3B14	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	9			
10	GND	6B2	6B0	V _{CC}		3B3	3B4	3B5	3B6	GND	3B6	3B10	3B14	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	10			
11	6B6	6B5	6B4	6B3		3B7	3B8	3B9	3B10	3B6	3B10	3B14	3B14	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	11			
12	6B10	6B9	6B8	6B7		3B11	3B12	3B13	3B14	3B7	3B11	3B14	3B14	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	12			
13	6B14	6B13	6B12	6B11		V _{CC}	2B11	2B15	3B15	GND	2B11	2B15	3B15	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	13			
14	GND	7B15	7B14	V _{CC}		2B14	2B12	2B13	2B14	GND	2B14	2B12	2B13	2B14	2B13	2B9	2B5	2B2	2A6	2A4	2A1	2A15	2A13	2A10	2A12	2A14	2A6	14			
15	7B14	7B13	7B12	7B11		2B7	2B8	2B9	2B10	2B7	2B8	2B9	2B10	2B7	2B8	2B9	2B10	2B7	2B8	2B9	2B10	2B7	2B8	2B9	2B10	2B7	2B8	15			
16	NC	7B10	7B9	7B8		2B3	2B4	2B5	2B6	2B3	2B4	2B5	2B6	2B3	2B4	2B5	2B6	2B3	2B4	2B5	2B6	2B3	2B4	2B5	2B6	2B3	2B4	16			
17	7B7	7B6	7B5	7B4		V _{CC}	2B0	2B2	GND	V _{CC}	2B0	2B2	GND	V _{CC}	2B0	2B2	GND	V _{CC}	2B0	2B2	GND	V _{CC}	2B0	2B2	GND	V _{CC}	2B0	17			
18	GND	7B3	7B2	V _{CC}		2A3	2A2	2A0	2B1	2A3	2A2	2A0	2B1	2A3	2A2	2A0	2B1	2A3	2A2	2A0	2B1	2A3	2A2	2A0	2B1	2A3	2A2	18			
19	7B1	7B0	7A1	7A4		2A7	2A5	2A4	2A1	2A7	2A5	2A4	2A1	2A7	2A5	2A4	2A1	2A7	2A5	2A4	2A1	2A7	2A5	2A4	2A1	2A7	2A5	19			
20	7A0	7A2	7A3	7A8		2A11	2A8	2A6	GND	2A11	2A8	2A6	GND	2A11	2A8	2A6	GND	2A11	2A8	2A6	GND	2A11	2A8	2A6	GND	2A11	2A8	20			
21	7A5	7A6	7A7	7A12	2A15	2A10	2A9	NC	2A15	2A10	2A9	NC	2A15	2A10	2A9	NC	2A15	2A10	2A9	NC	2A15	2A10	2A9	NC	2A15	2A10	21				
22	GND	7A9	7A11	7A15	V _{CC}	2A13	2A12	GND	V _{CC}	2A13	2A12	GND	V _{CC}	2A13	2A12	GND	V _{CC}	2A13	2A12	GND	V _{CC}	2A13	2A12	GND	V _{CC}	2A13	22				
23	7A10	7A13	7A14	V _{CC}	TCK	NC	2A14	NC	TCK	NC	2A14	NC	TCK	NC	2A14	NC	TCK	NC	2A14	NC	TCK	NC	2A14	NC	TCK	NC	23				
24	NC	NC	TDI	0A2	1A1	NC	GND	GND	1A1	NC	0D2	0D4	1D1	1D4	1D5	1D9	1D14	1A13	1A10	1A8	1A7	1A4	1A2	NC	GND	GND	24				
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D13	0D10	0D6	0D2	0D0	1D0	1D3	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	25				
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	11/CLK1	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	26				

Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



20446G-031

Select devices have been discontinued.
See Ordering Information section for product status.