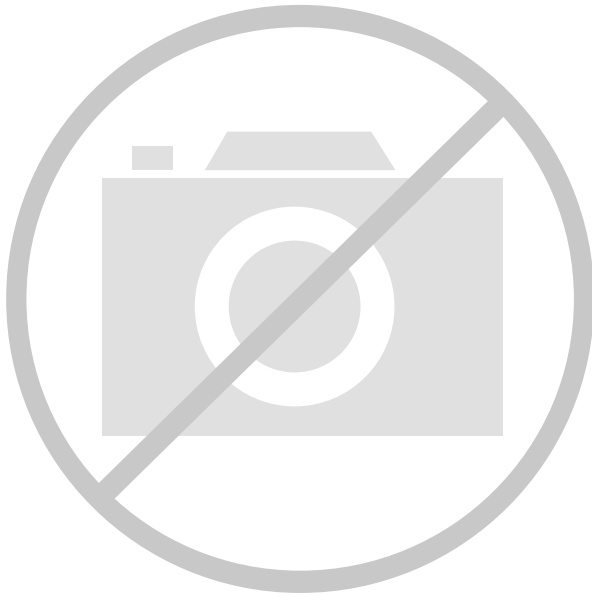




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	320
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-320-160-15yc

Table 2. MACH 5 Speed Grades

Device	Speed Grade ¹						
	-5	-6	-7	-10	-12	-15	-20
M5-128 ²			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C, I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256 ²			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C	C, I	C, I	C, I	C, I	I
M5LV-384		C	C, I	C, I	C, I	C, I	I
M5-512		C	C, I	C, I	C, I	C, I	I
M5LV-512		C	C, I	C, I	C, I	C, I	I

Note:

1. C = Commercial grade, I = Industrial grade
2. /1 version recommended for new designs

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL[®] block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options ¹

Supply Voltage	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
	5	3.3		5	3.3	5	3.3	5	3.3	5	3.3
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

Note:

1. The I/O options indicated with a "*" are obsolete, please contact factory for more information.

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued.
See Ordering Information section for product status.

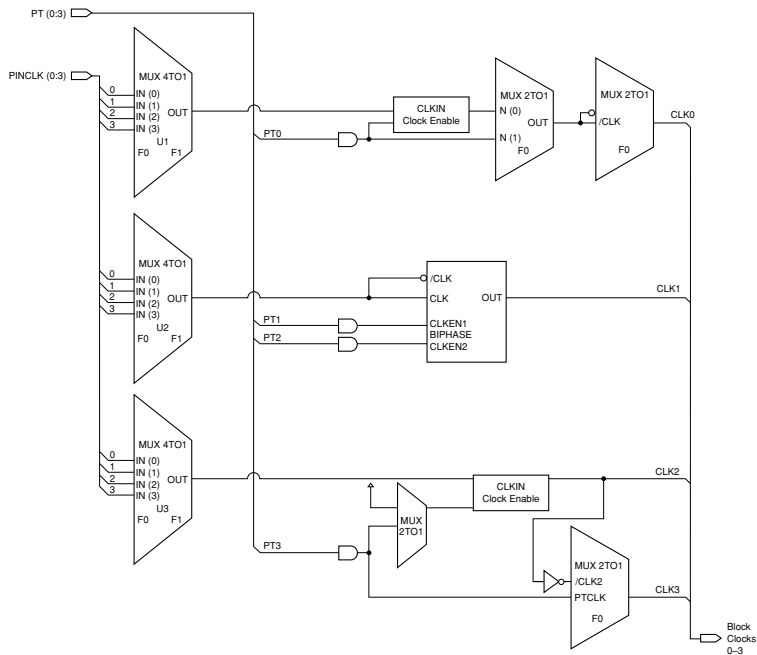
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

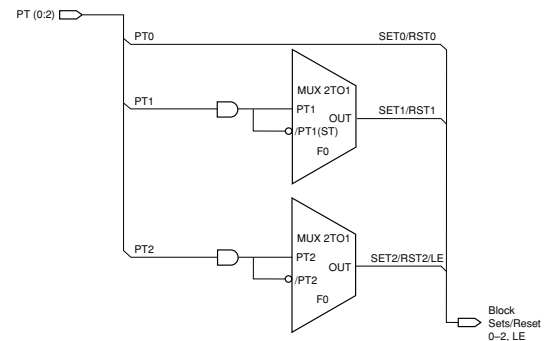
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator



20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.
See Ordering Information section for product status.**

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

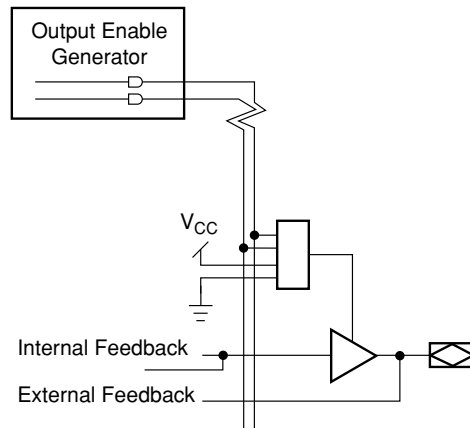
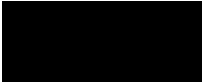


Figure 6. Output Enable Generator and I/O Cell

20446G-006

Select devices have been discontinued.
See Ordering Information section for product status.



MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.
See Ordering Information section for product status.



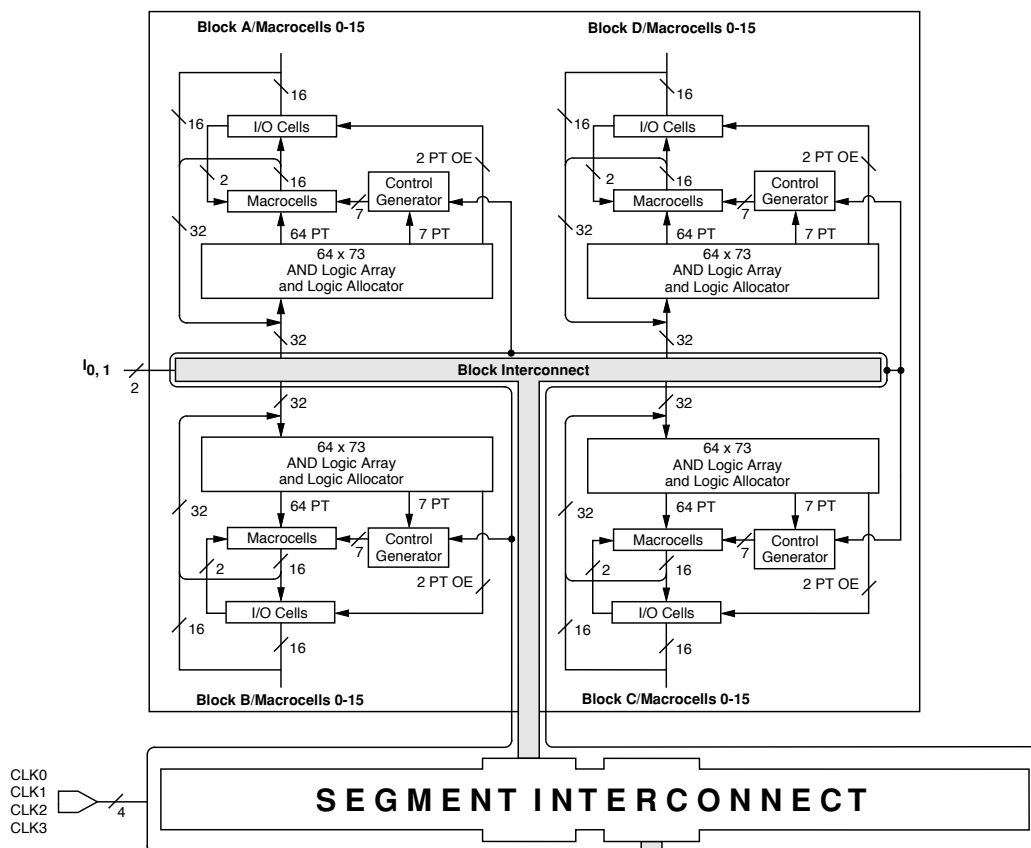
SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

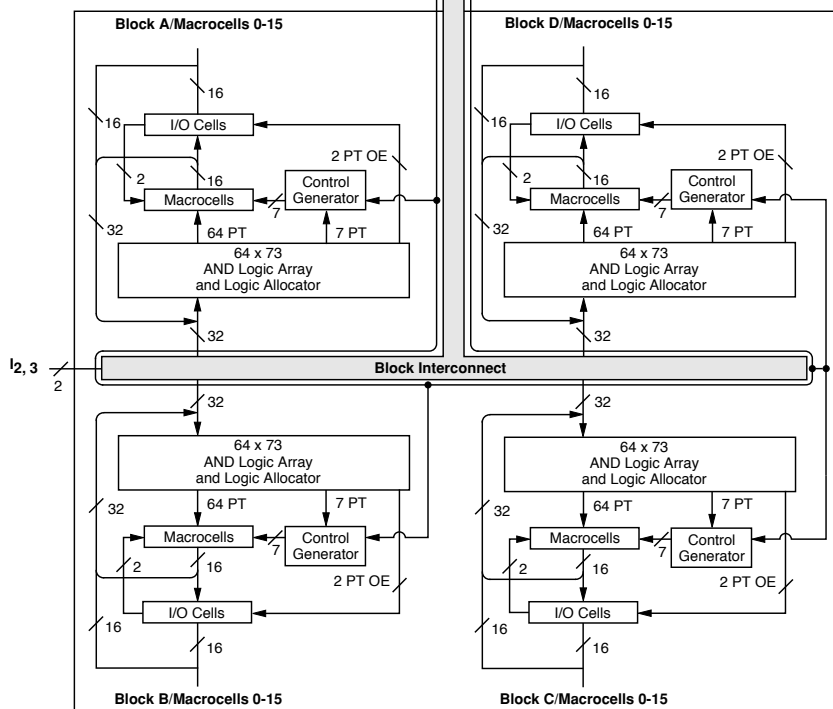
**Select devices have been discontinued.
See Ordering Information section for product status.**

BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0



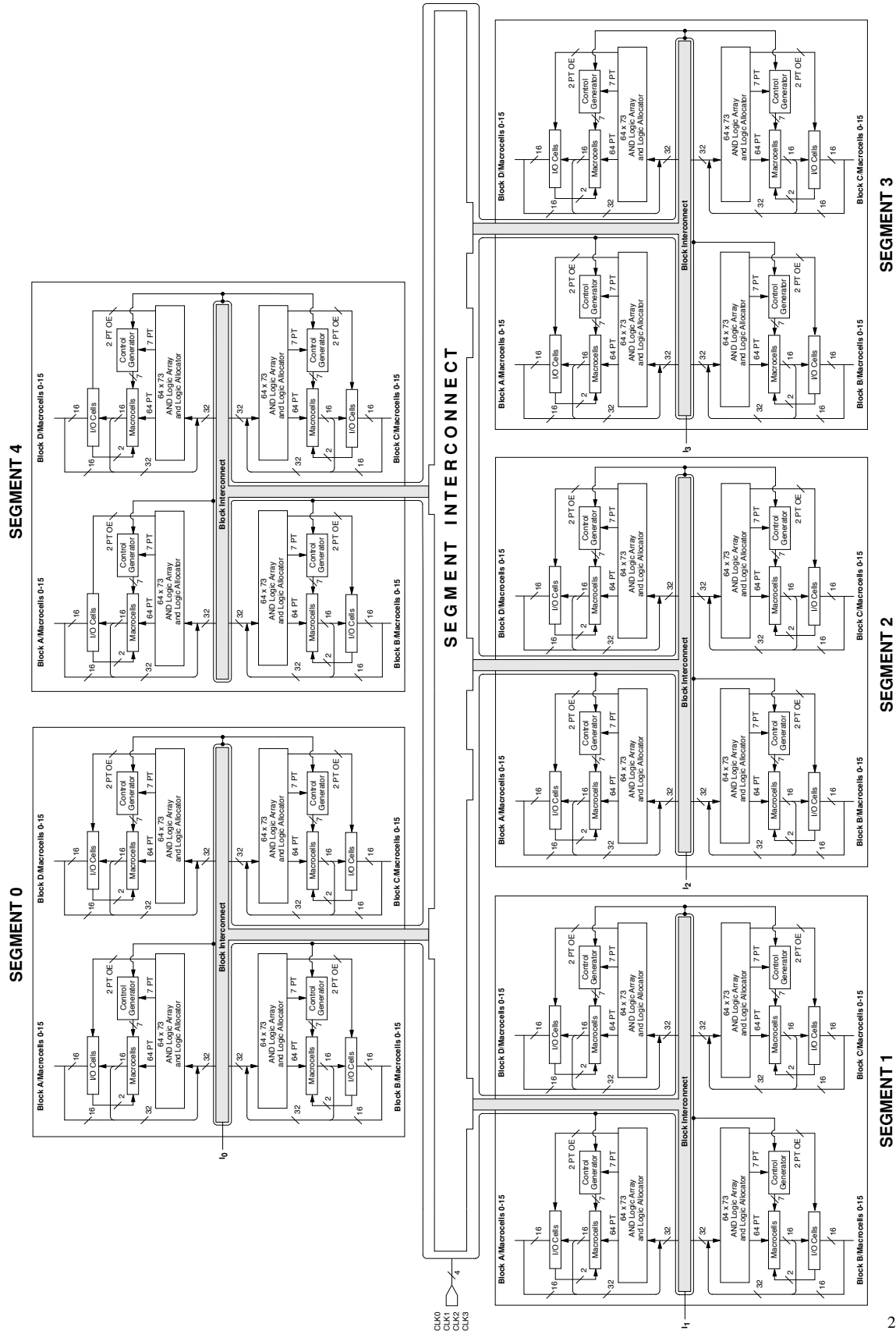
SEGMENT 1



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-007

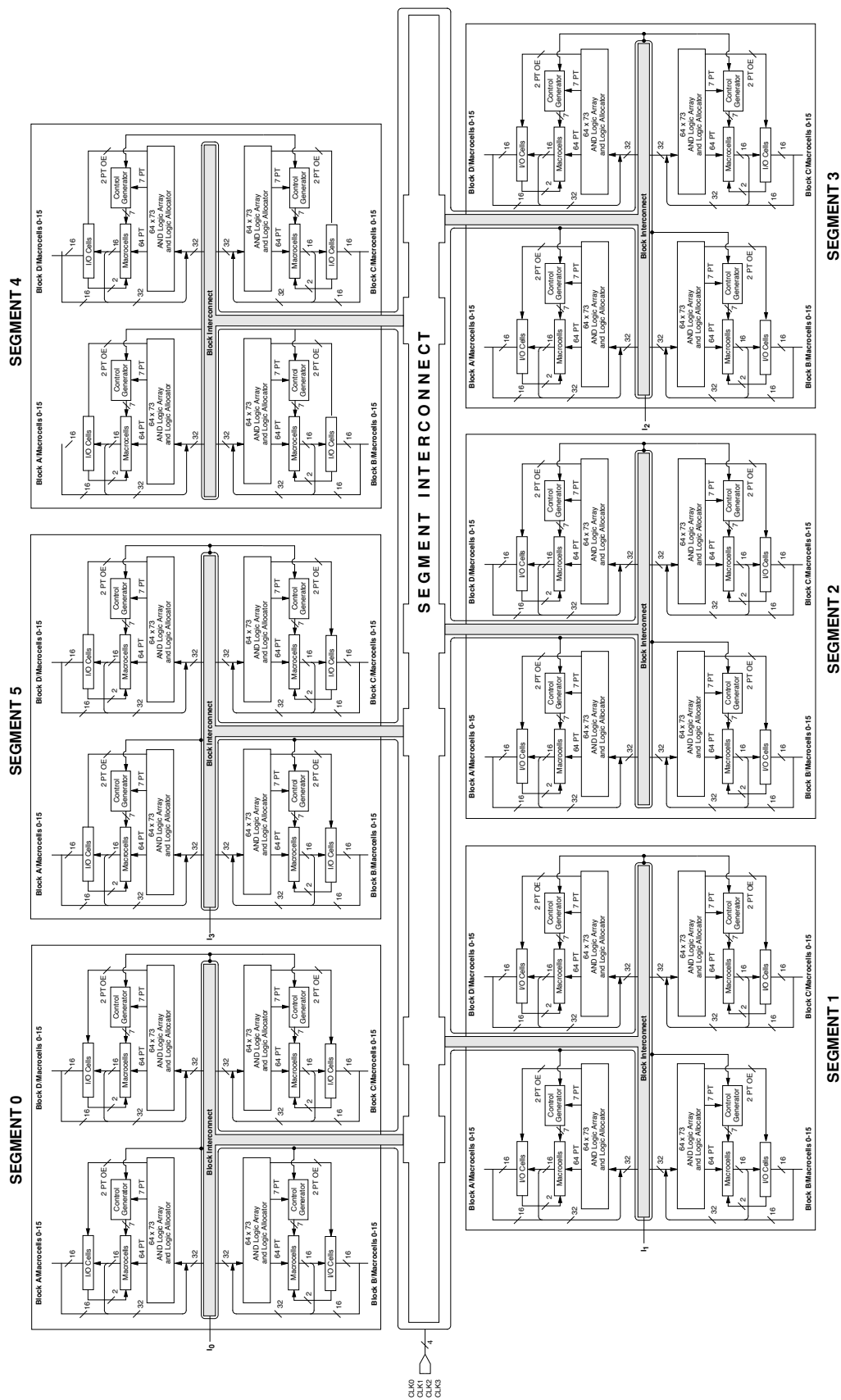
BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-010

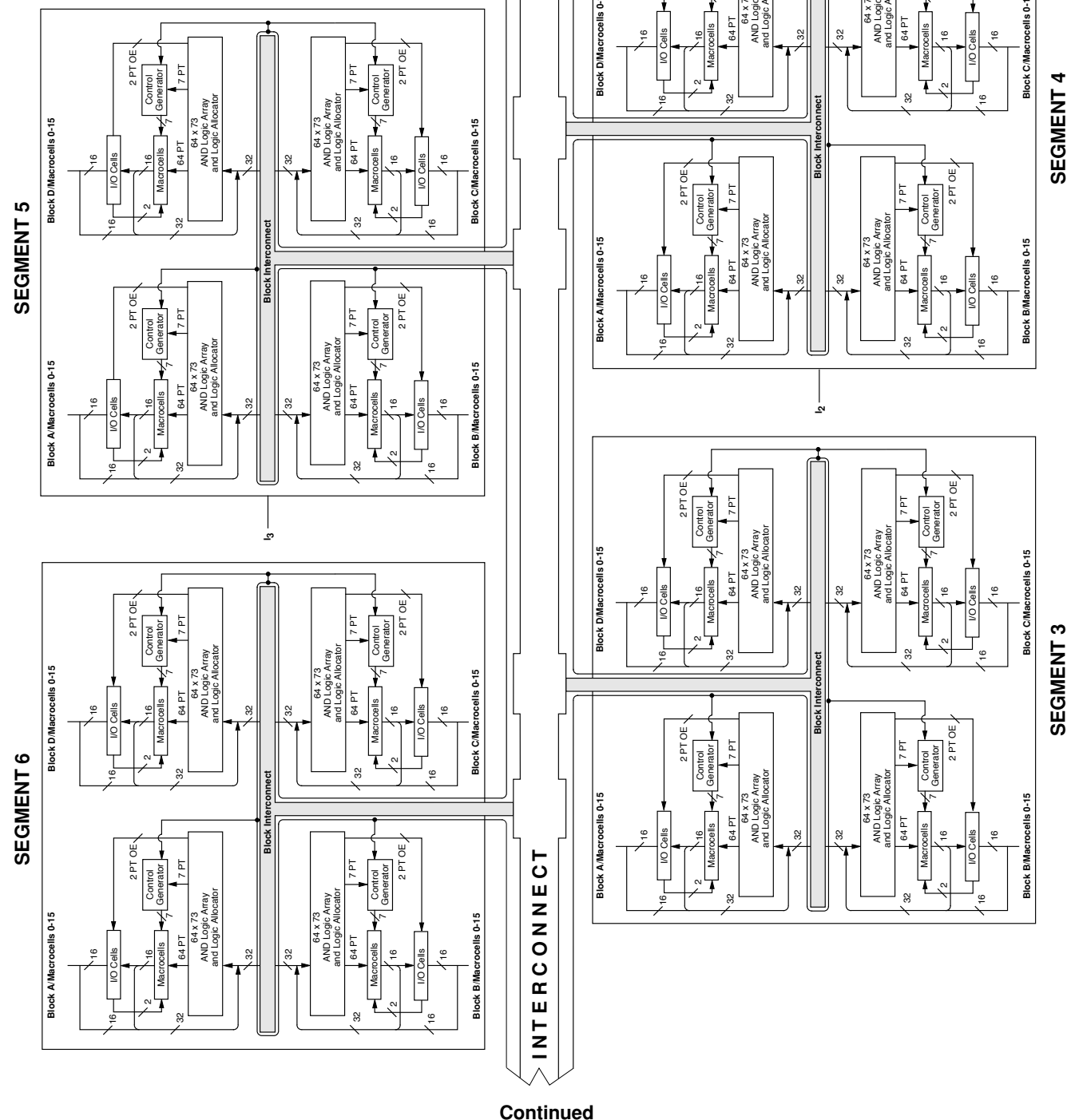
BLOCK DIAGRAM — M5(LV)-384/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-011

BLOCK DIAGRAM — M5(LV)-512/XXX



Continued

Select devices have been discontinued.
See Ordering Information section for product status.

ABSOLUTE MAXIMUM RATINGS

M5LV

Storage Temperature. -65°C to +150°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +4.5 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued.
See Ordering Information section for product status.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 3.2 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 100 \mu A$		0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16 \text{ mA (Note 1)}$		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-15	-160	mA

Notes:

1. Total I_{OL} between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																
t _{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0		18.0	ns
t _{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:																
t _{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		10.0		ns
t _{SA}	Asynchronous clock setup time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{COsi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0		10.0	ns
t _{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0		12.0	ns
t _{COAi}	Asynchronous clock to internal output		6.0		6.0		8.0		10.0		13.0		15.0		18.0	ns
t _{COA}	Asynchronous clock to output		8.0		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:																
t _{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t _{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0		10.0	ns
t _{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0		12.0	ns
t _{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0		12.0	ns
t _{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:																
t _{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		4.0		ns
t _{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:																
t _{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t _{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
t _{PDILi}	Transparent input latch		5.0		5.0		5.5		6.0		6.0		6.0		6.0	ns
Output Delays:																
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns
t _{ER}	Output disable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns

Select devices have been discontinued.
See Ordering Information section for product status.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Delays:																
t _{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t _{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t _{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t _{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t _{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t _{SRI}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t _{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t _{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

Select devices have been discontinued.
See Ordering Information section for product status.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																
f _{MAX}	External feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{HS})	200		167		167		125		100		83.3		83.3		MHz
f _{MAXA}	External feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{HA})	167		125		125		100		83.3		71.4		62.5		MHz
f _{MAXI}	Maximum input register frequency 1/(t _{SIRS} +t _{HIRS}) or 1/(2 x t _{WICW})	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

- See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.
- Numbers in parentheses are for M5-128, M5-192, M5-256.
- If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).

Select devices have been discontinued.
See Ordering Information section for product status.

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	$V_{IN} = 2.0\text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	$V_{OUT} = 2.0\text{ V}$	3.3 V or 5 V, 25° C, 1 MHz	10	pF

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

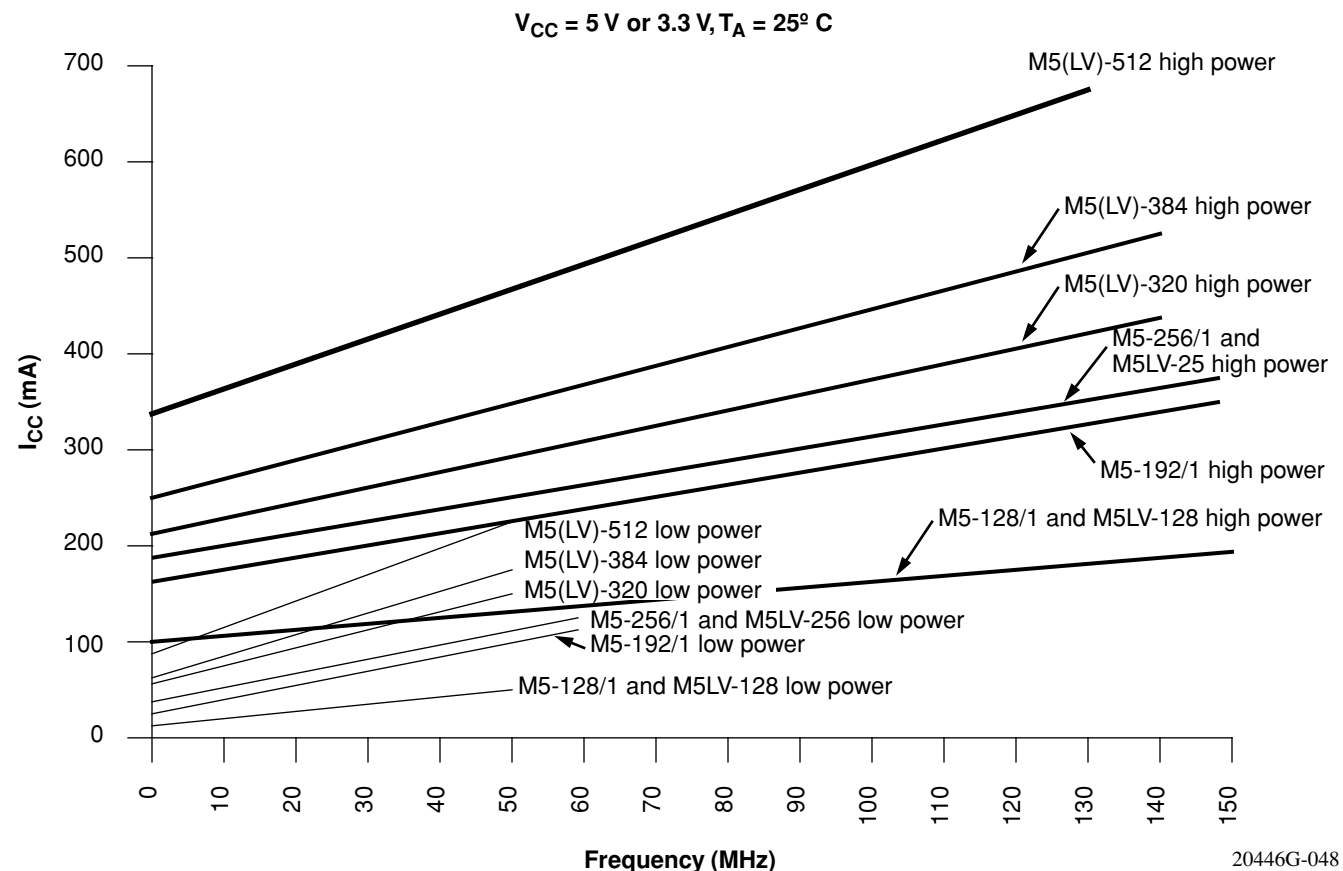


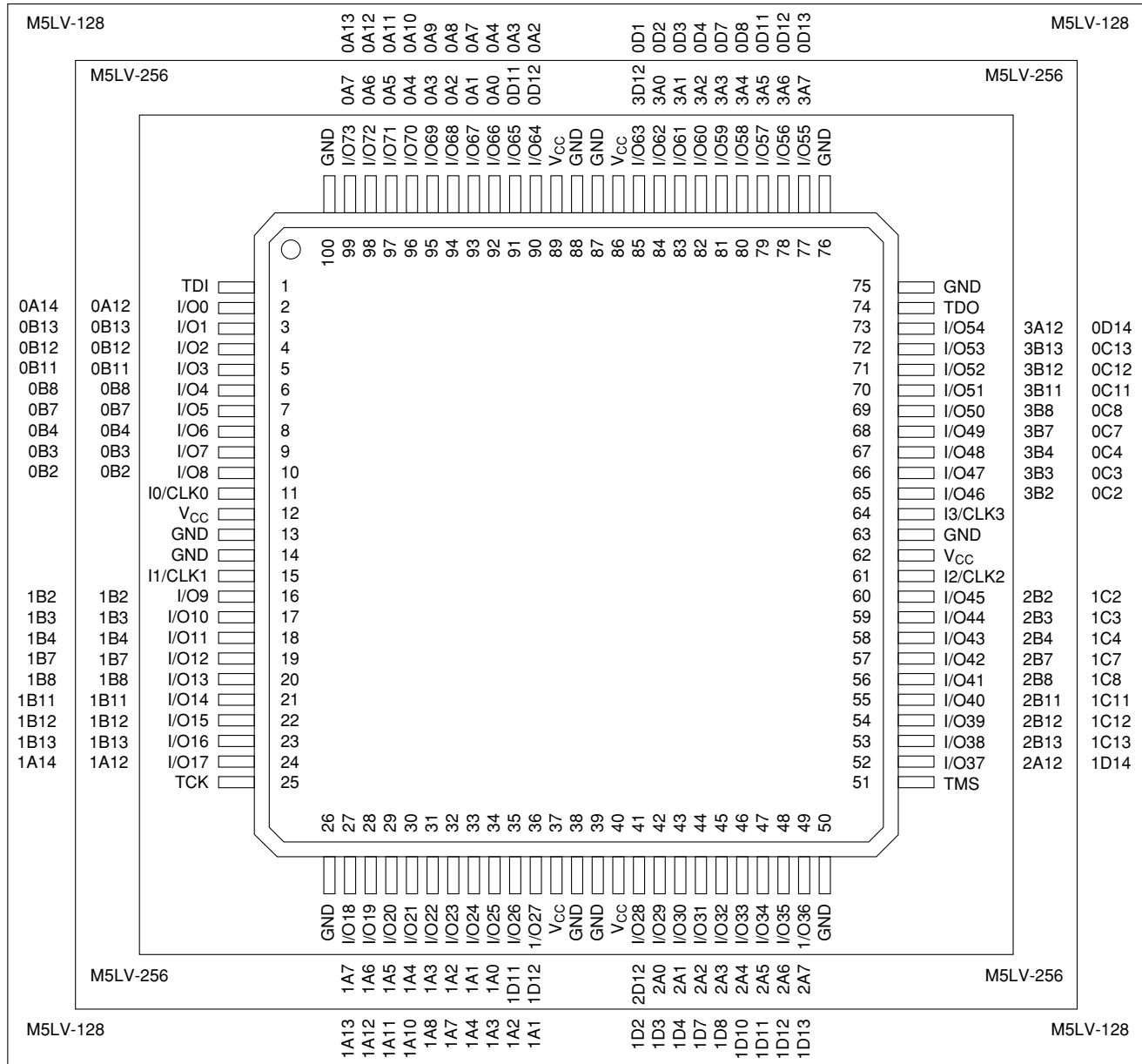
Figure 8. I_{CC} Curves at High/Low Power Modes

Select devices have been discontinued. See Ordering Information section for product status.

100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

100-Pin TQFP (74 I/O)

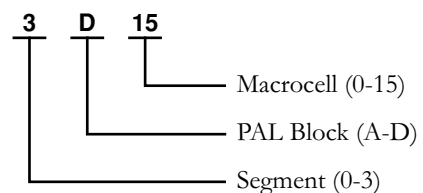


Select devices have been discontinued.
See Ordering Information section for product status.

20446G-018

Pin Designations

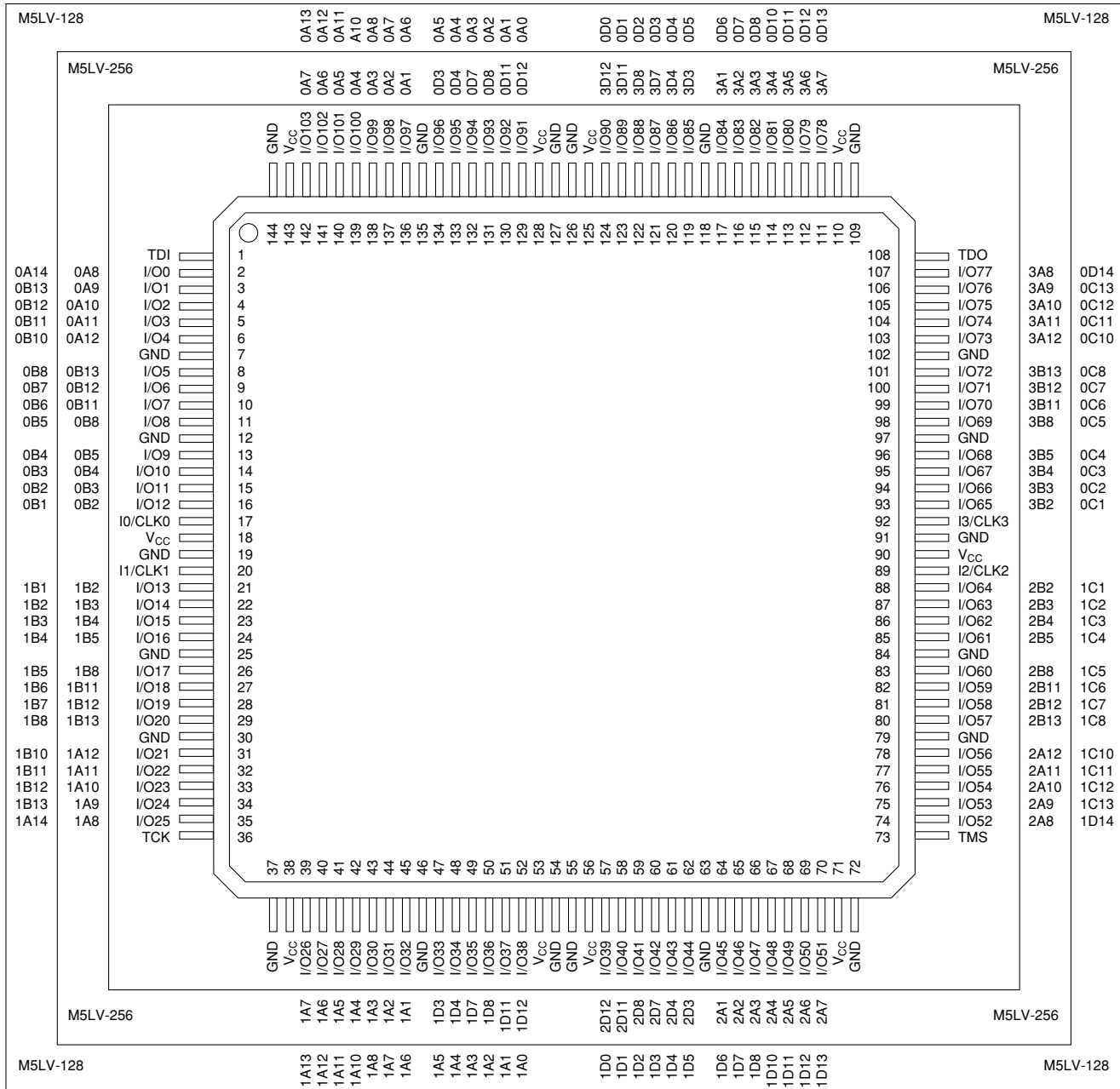
CLK = Clock	V _{CC} = Supply Voltage
GND = Ground	TDI = Test Data In
I = Input	TCK = Test Clock
I/O = Input/Output	TMS = Test Mode Select
NC = No Connect	TDO = Test Data Out



144-PIN TQFP CONNECTION DIAGRAM

Top View

144-Pin TQFP



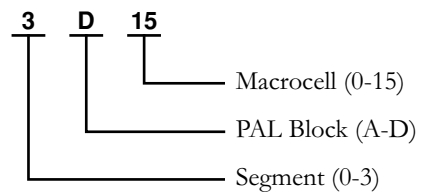
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-020

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

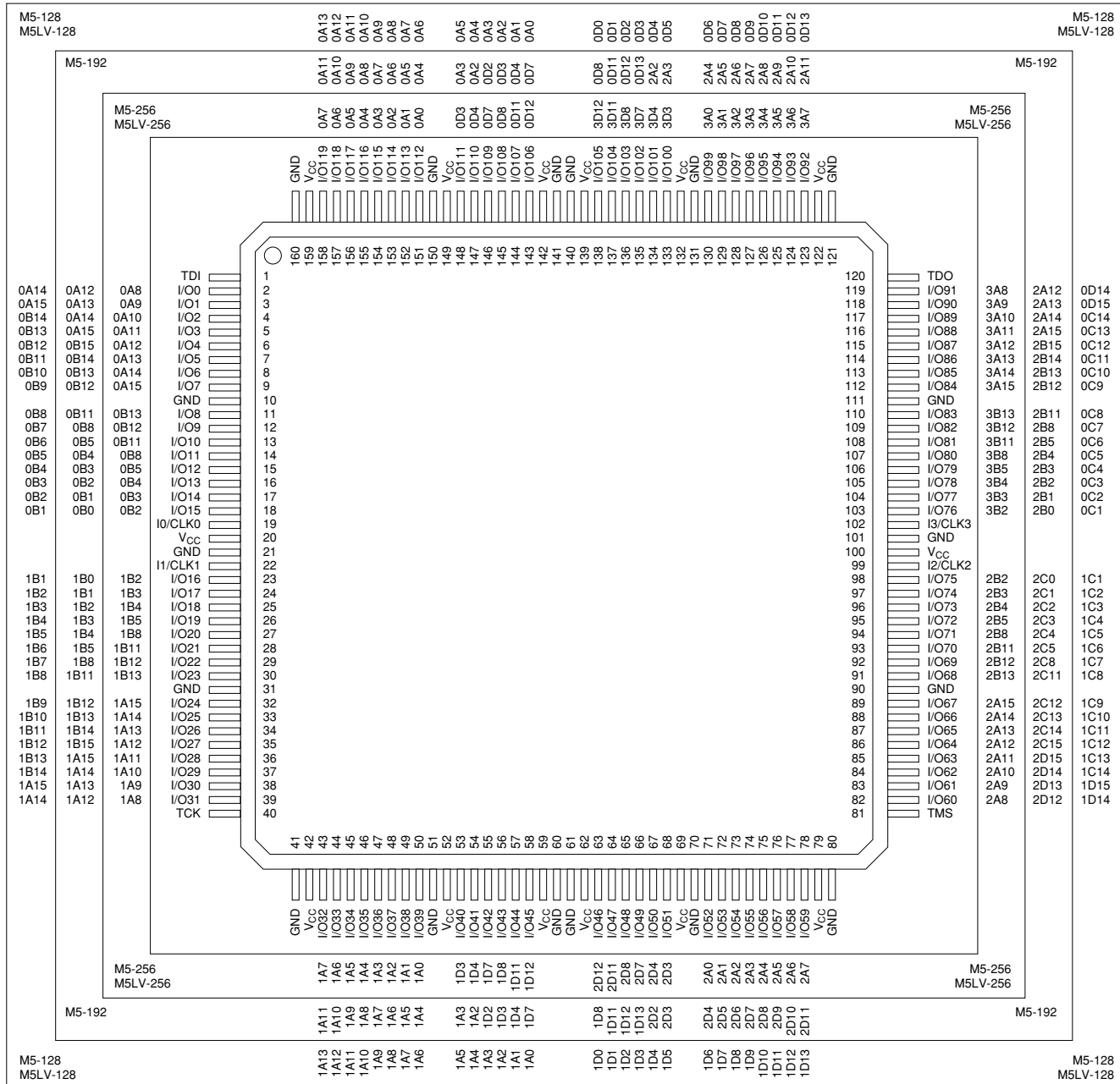
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)



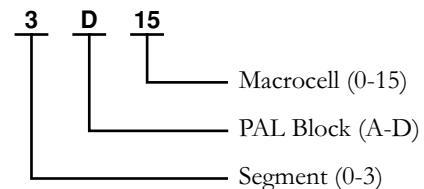
**Select devices have been discontinued.
See Ordering Information section for product status.**

20446G-021

Pin Designations

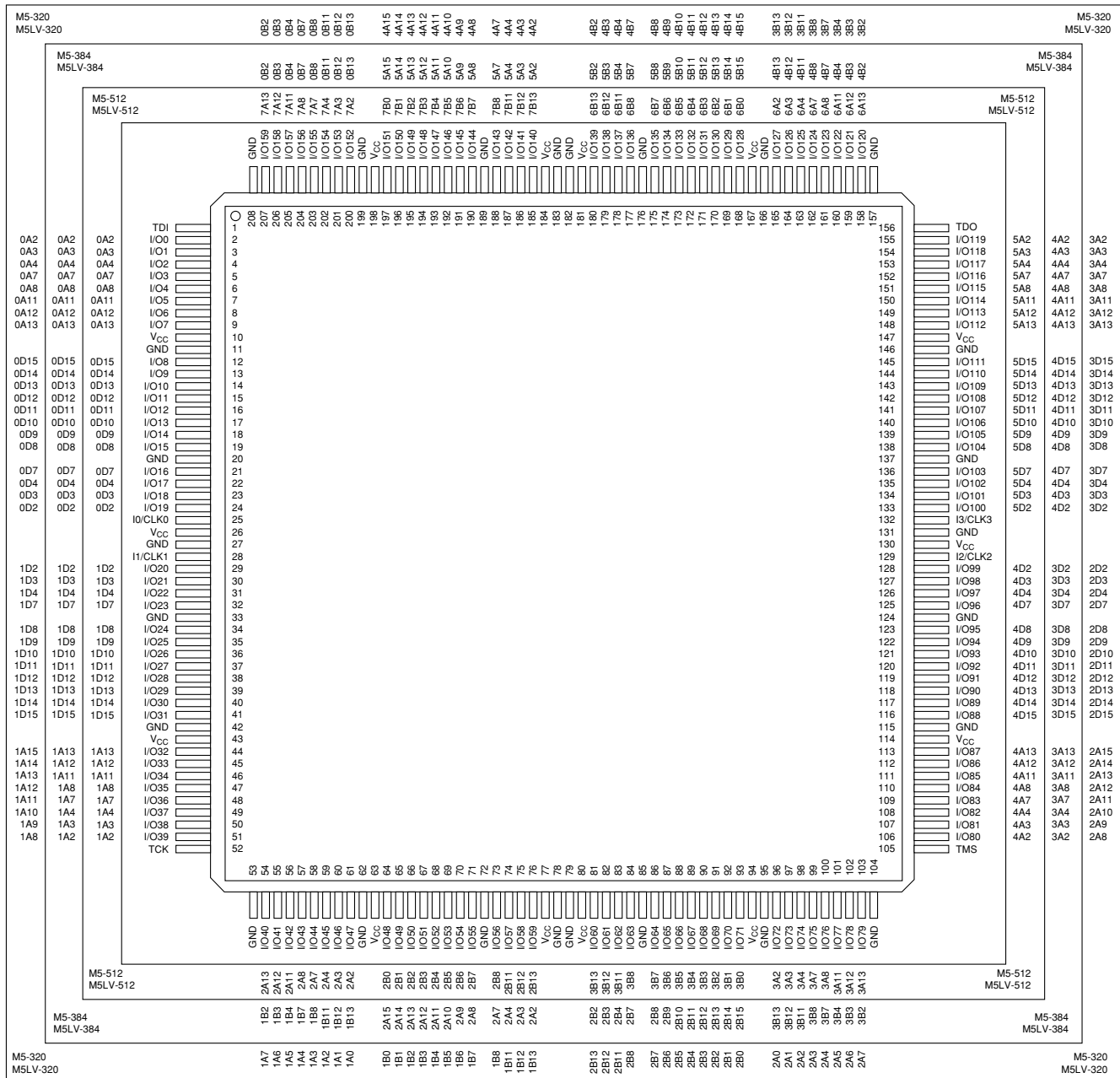
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

208-Pin PQFP (320, 384, 512 Macrocells)



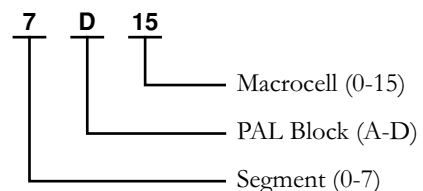
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-024

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (I/O Pin-outs)

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11	GND	I/O44	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	A
B	GND	I/O12	I/O28	I/O45	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	B
C	I/O0	I/O13	V _{CC}	I/O46	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V _{CC}	I/O165	I/O181	C
D	I/O1	I/O14	I/O29	V _{CC}	V _{CC}	I/O66	V _{CC}	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V _{CC}	I/O124	V _{CC}	V _{CC}	I/O149	I/O166	I/O182	D
E	I/O2	I/O15	I/O30	TDI													TDI	I/O150	I/O167	I/O183	E
F	GND	I/O16	I/O31	I/O47													I/O137	I/O151	I/O168	GND	F
G	I/O3	I/O17	I/O32	V _{CC}													V _{CC}	I/O152	I/O169	I/O184	G
H	GND	I/O18	I/O33	I/O48													I/O138	I/O153	I/O170	GND	H
J	I/O4	I/O19	I/O34	I/O49													I/O139	I/O154	I/O171	I/O185	J
K	GND	I/O20	I/O35	I/O50													I/O140	I/O155	I/O172	I/O186	K
L	I/O5	I/O21	I/O36	I/O51													I/O141	I/O156	I/O173	GND	L
M	I/O6	I/O22	I/O37	I/O52													I/O142	I/O157	I/O174	I/O187	M
N	GND	I/O23	I/O38	I/O53													I/O143	I/O158	I/O175	GND	N
P	I/O7	I/O24	I/O39	V _{CC}													V _{CC}	I/O159	I/O176	I/O188	P
R	GND	I/O25	I/O40	I/O54													I/O144	I/O160	I/O177	GND	R
T	I/O8	I/O26	I/O41	TCK													TMS	I/O161	I/O178	I/O189	T
U	I/O9	I/O27	I/O42	V _{CC}													V _{CC}	I/O162	I/O179	I/O190	U
V	I/O10	I/O28	V _{CC}	I/O55													I/O145	V _{CC}	I/O180	I/O191	V
W	GND	I/O29	I/O43	I/O56													I/O146	I/O163	I/O181	GND	W
Y	GND	I/O30	GND	I/O57													I/O147	GND	I/O182	I/O192	Y

Pin Designations

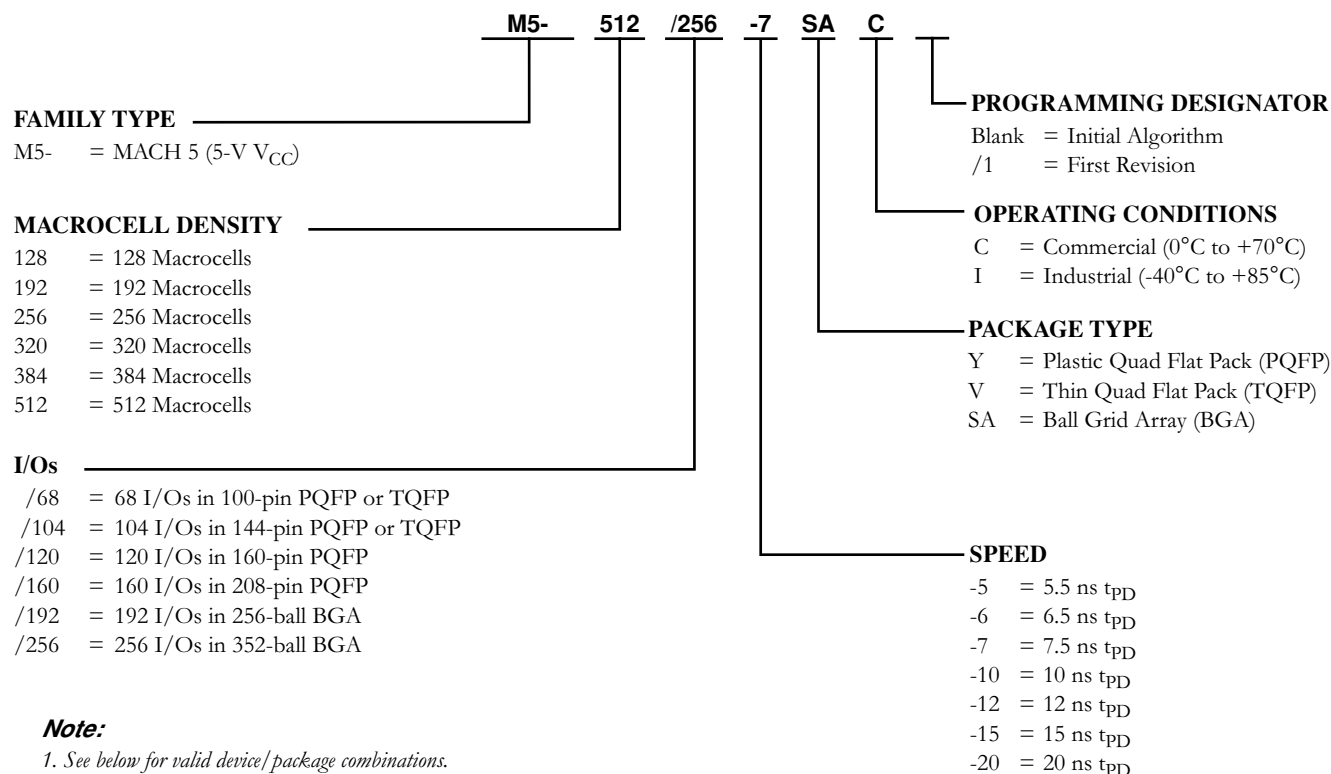
CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

Select devices have been discontinued.
See Ordering Information section for product status.

20446G-026

5V M5 ORDERING INFORMATION^{1,2}

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC ¹ , YI ¹
M5-128/120		YC, YI
M5-192/68		VC, VI
M5-192/120		YC, YI
M5-256/68		VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial: -6, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, YI
M5-320/192		SAC, SAI
M5-384/160		YC, YI
M5-512/160		YC, YI
M5-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.