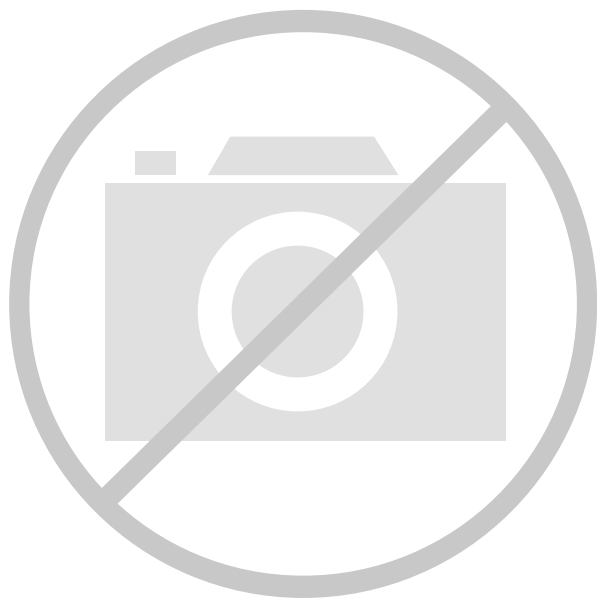




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	512
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-512-160-15yc



Table 1. MACH 5 Device Features ¹

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	160	160	160	256	256
t _{PD} (ns)	5.5	5.5	5.5	5.5	5.5	6.5	6.5	6.5	6.5	6.5	6.5
t _{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
t _{COS} (ns)	4.5	4.5	4.5	4.5	4.5	5.0	5.0	5.0	5.0	5.0	5.0
f _{CNT} (MHz)	182	182	182	182	182	167	167	167	167	167	167
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

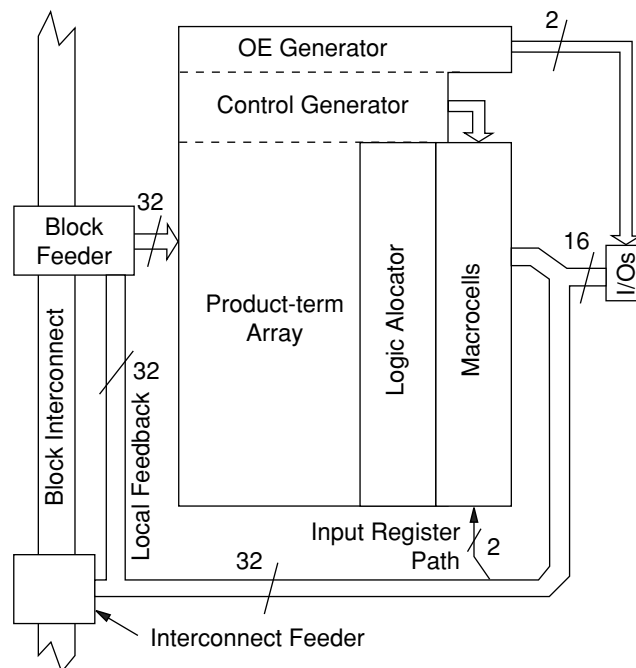
1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.

GENERAL DESCRIPTION

The MACH[®] 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E²CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.
See Ordering Information section for product status.



20446G-002

Figure 2. PAL Block Structure

Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 or 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 4. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂ , C ₃ , C ₄	M ₈	C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₁	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅	M ₉	C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₂	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆	M ₁₀	C ₇ , C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₃	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₁	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₄	C ₀ , C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇	M ₁₂	C ₈ , C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₅	C ₁ , C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈	M ₁₃	C ₉ , C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₂ , C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉	M ₁₄	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₃ , C ₄ , C ₅ , C ₆ , C ₇ , C ₈ , C ₉ , C ₁₀	M ₁₅	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅

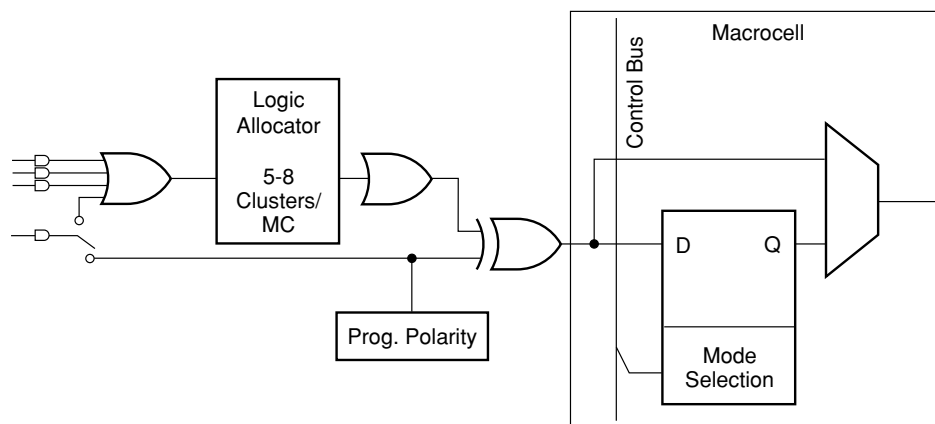
Select devices have been discontinued.
See Ordering Information section for product status.

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ($A*B*C$)
- ◆ Sum-term clock ($A+B+C$)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.
See Ordering Information section for product status.

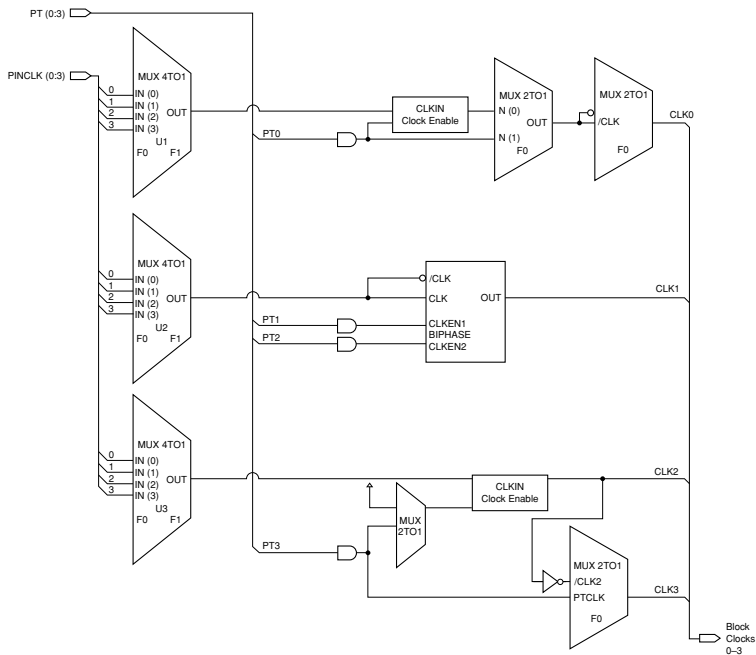
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

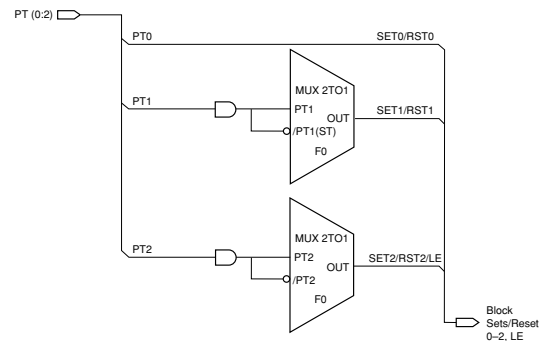
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator

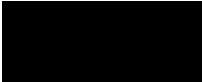


20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.
See Ordering Information section for product status.**



MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.
See Ordering Information section for product status.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

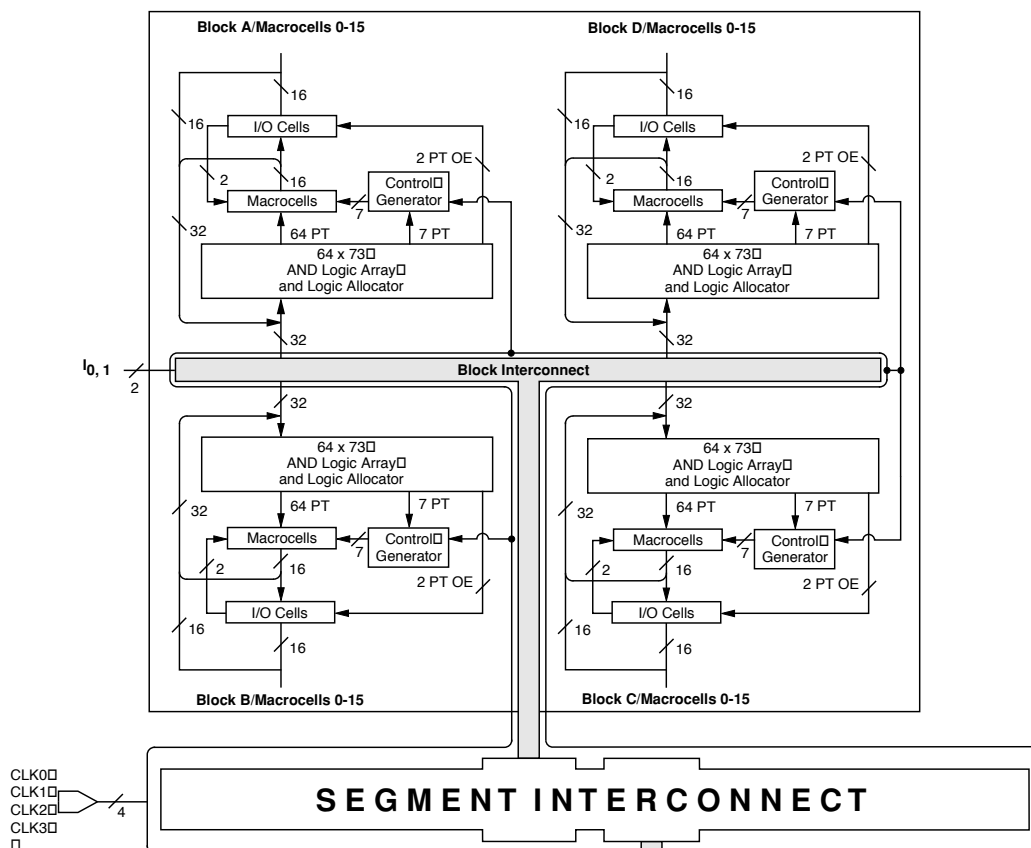
POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

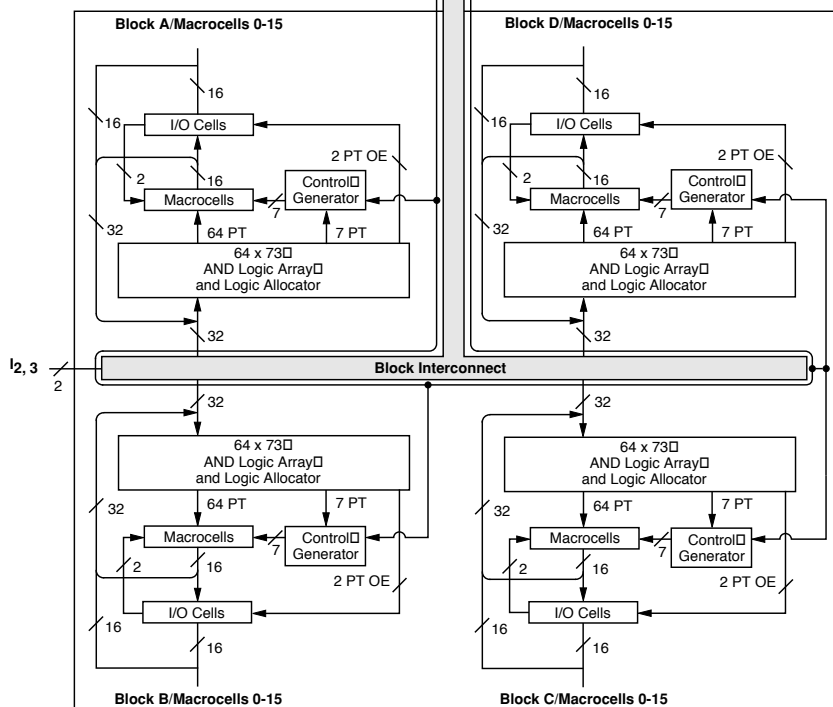
Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0



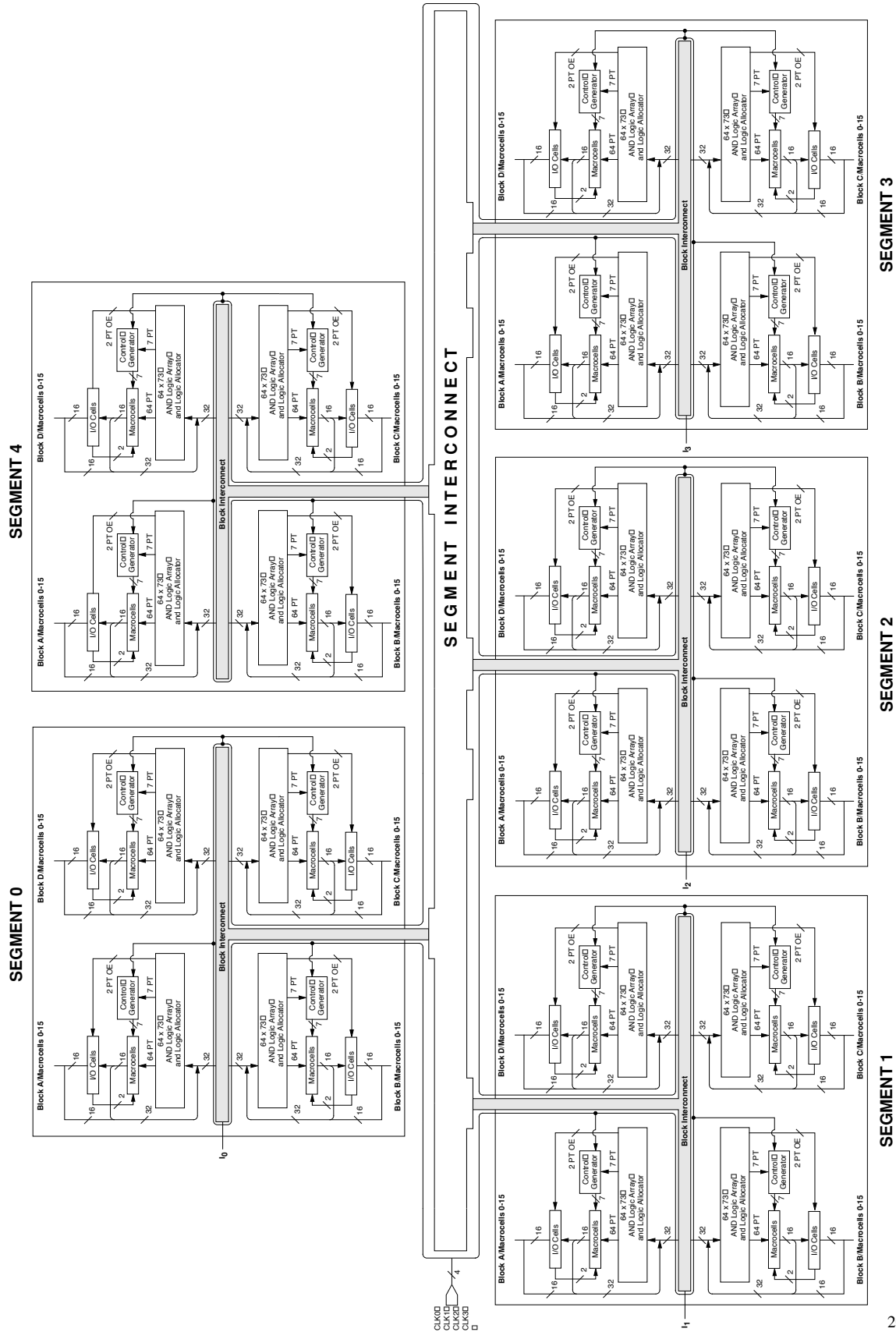
SEGMENT 1



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-007

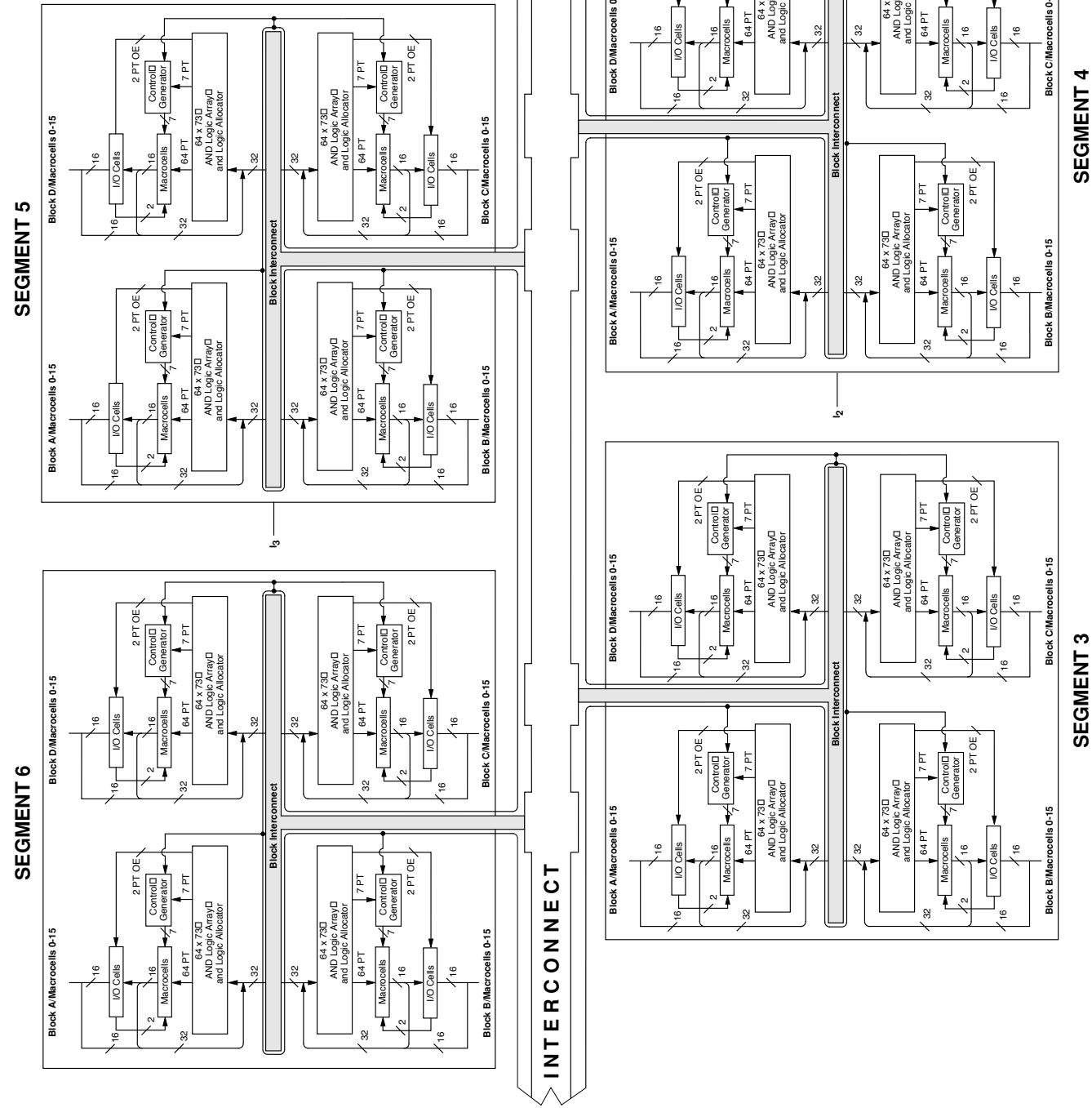
BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-010

BLOCK DIAGRAM — M5(LV)-512/XXX



Continued

Select devices have been discontinued.
See Ordering Information section for product status.

ABSOLUTE MAXIMUM RATINGS

M5LV

Storage Temperature. -65°C to +150°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +4.5 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +3.0 V to +3.6 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued.
See Ordering Information section for product status.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 3.2 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 100 \mu A$		0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16 \text{ mA (Note 1)}$		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH} \text{ Min or } V_{OUT} \leq V_{OL} \text{ Max (Note 2)}$		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 3.6, V_{CC} = \text{Max (Note 3)}$			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0, V_{CC} = \text{Max (Note 3)}$			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0, V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 3)}$			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}, V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-15	-160	mA

Notes:

1. Total I_{OL} between ground pins should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
4. Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

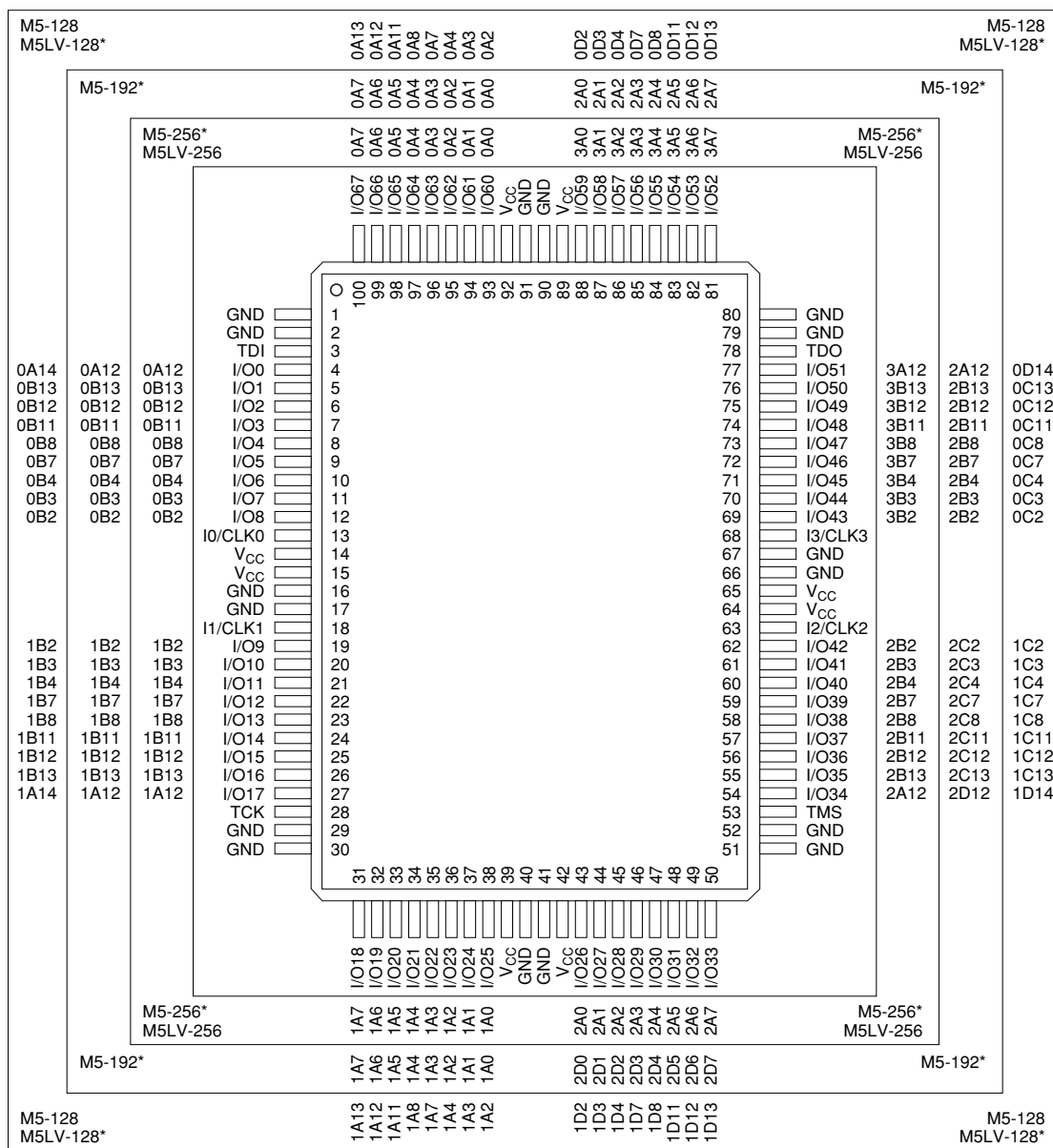
		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Delays:																
t _{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t _{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t _{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t _{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t _{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t _{SRI}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t _{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t _{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

Select devices have been discontinued.
See Ordering Information section for product status.

100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)



*Package obsolete, contact factory.

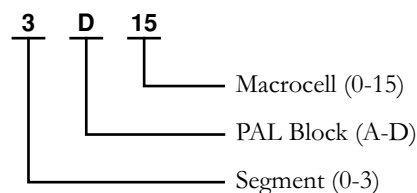
20446G-016

Select devices have been discontinued.
See Ordering Information section for product status.

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

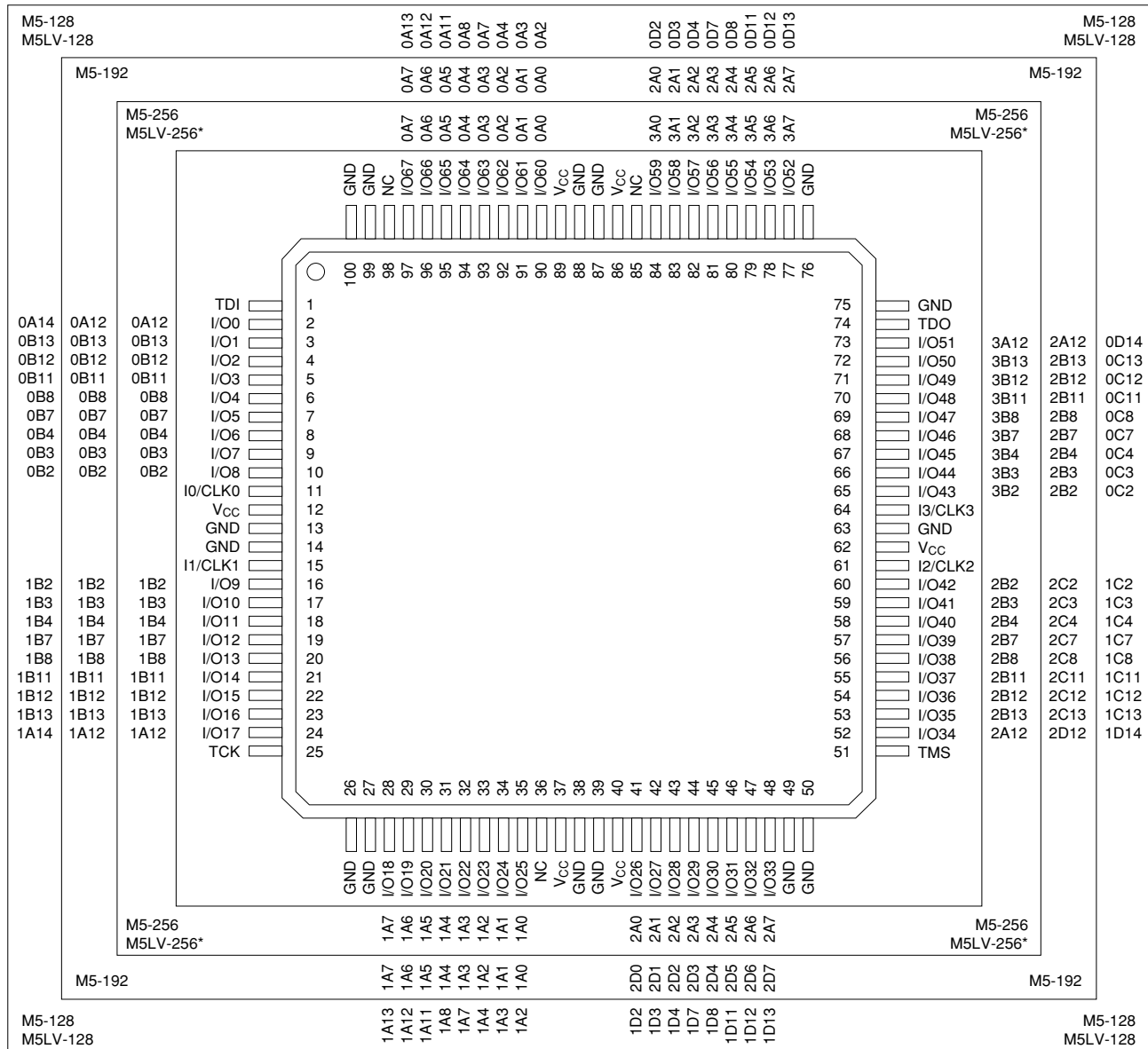
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

Top View

100-Pin TQFP (68 I/O)



*Package obsolete, contact factory.

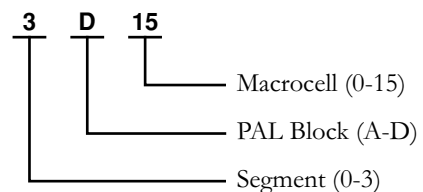
Select devices have been discontinued.
See Ordering Information section for product status.

20446G-017

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

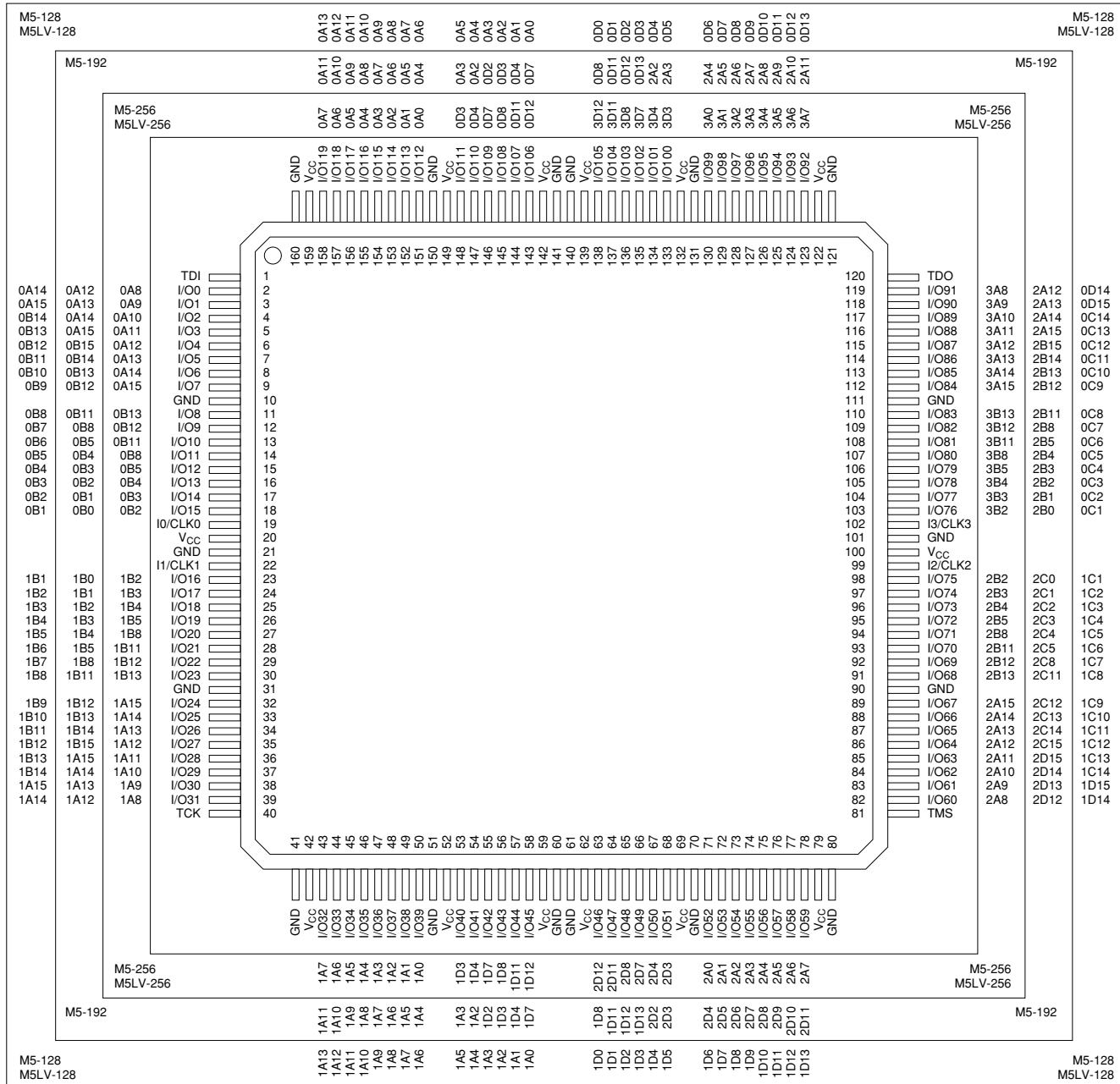


160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

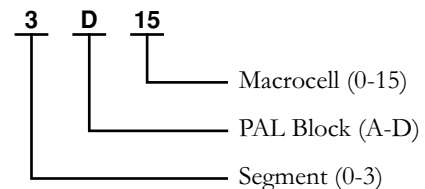
Select devices have been discontinued.
See Ordering Information section for product status.



Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

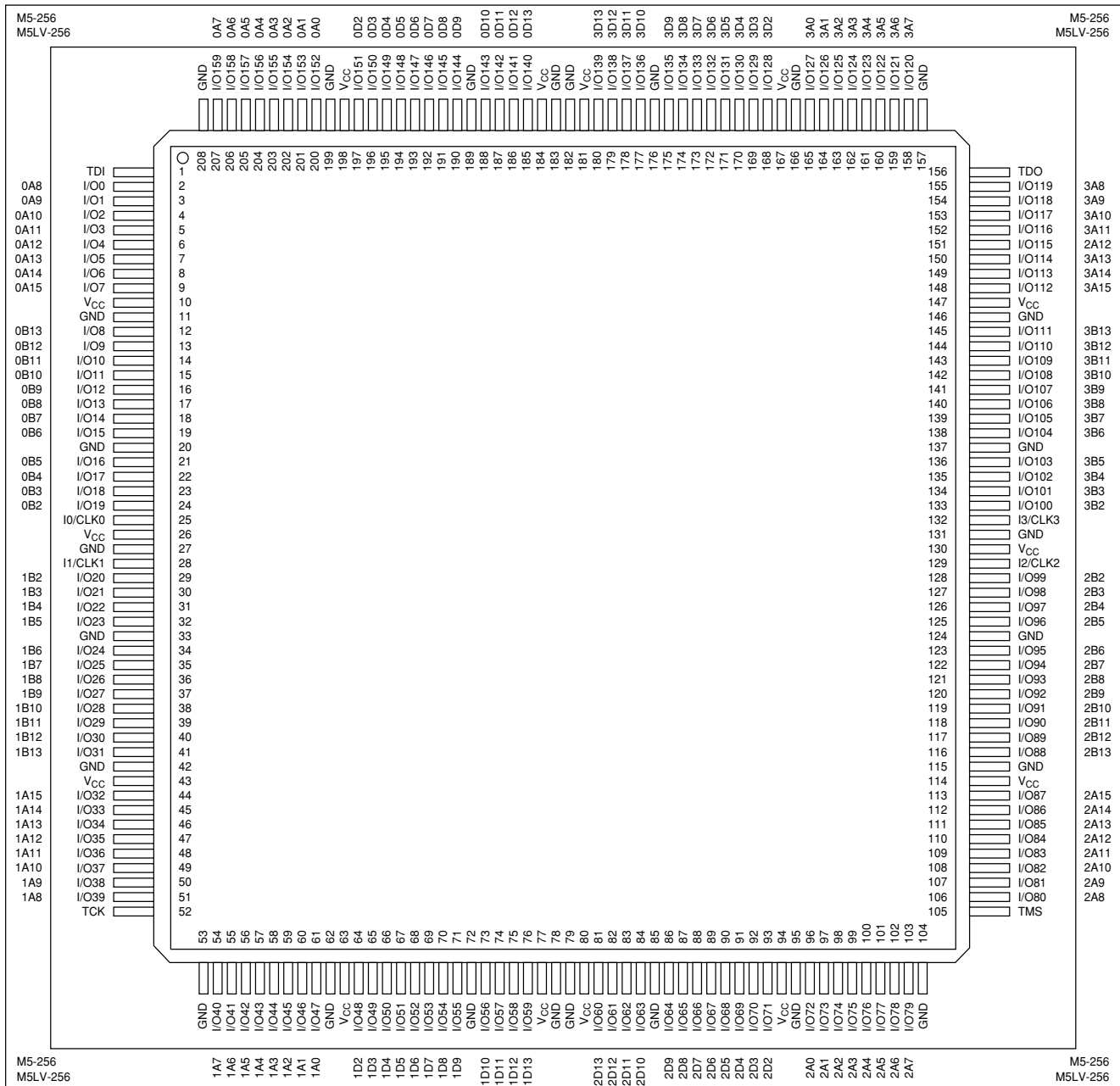
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (256 Macrocells)

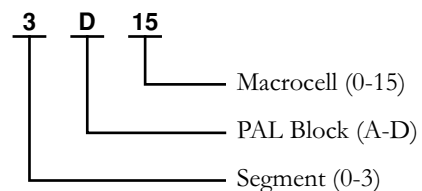


Select devices have been discontinued.
See Ordering Information section for product status.

20446G-023

Pin Designations

CLK = Clock	VCC = Supply Voltage
GND = Ground	TDI = Test Data In
I = Input	TCK = Test Clock
I/O = Input/Output	TMS = Test Mode Select
NC = No Connect	TDO = Test Data Out



256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (I/O Pin-outs)

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11	GND	I/O44	I/O58	GND	I/O70	I/O76	GND	GND	GND	GND	I/O108	I/O116	GND	I/O128	I/O134	GND	GND	GND	A
B	GND	I/O12	I/O28	I/O45	I/O59	I/O64	I/O71	I/O77	I/O84	I/O90	I/O96	I/O102	I/O109	I/O117	I/O122	I/O129	I/O135	I/O148	I/O164	GND	B
C	I/O0	I/O13	V _{CC}	I/O46	I/O60	I/O65	I/O72	I/O78	I/O85	I/O91	I/O97	I/O103	I/O110	I/O118	I/O123	I/O130	I/O136	V _{CC}	I/O165	I/O181	C
D	I/O1	I/O14	I/O29	V _{CC}	V _{CC}	I/O66	V _{CC}	I/O79	I/O86	I/O92	I/O98	I/O104	I/O111	V _{CC}	I/O124	V _{CC}	V _{CC}	I/O149	I/O166	I/O182	D
E	I/O2	I/O15	I/O30	TDI													TDI	I/O150	I/O167	I/O183	E
F	GND	I/O16	I/O31	I/O47													I/O137	I/O151	I/O168	GND	F
G	I/O3	I/O17	I/O32	V _{CC}													V _{CC}	I/O152	I/O169	I/O184	G
H	GND	I/O18	I/O33	I/O48													I/O138	I/O153	I/O170	GND	H
J	I/O4	I/O19	I/O34	I/O49													I/O139	I/O154	I/O171	I/O185	J
K	GND	I/O20	I/O35	I/O50													I/O140	I/O155	I/O172	I/O186	K
L	I/O5	I/O21	I/O36	I/O51													I/O141	I/O156	I/O173	GND	L
M	I/O6	I/O22	I/O37	I/O52													I/O142	I/O157	I/O174	I/O187	M
N	GND	I/O23	I/O38	I/O53													I/O143	I/O158	I/O175	GND	N
P	I/O7	I/O24	I/O39	V _{CC}													V _{CC}	I/O159	I/O176	I/O188	P
R	GND	I/O25	I/O40	I/O54													I/O144	I/O160	I/O177	GND	R
T	I/O8	I/O26	I/O41	TCK													TMS	I/O161	I/O178	I/O189	T
U	I/O9	I/O27	I/O42	V _{CC}													V _{CC}	I/O162	I/O179	I/O190	U
V	I/O10	I/O28	V _{CC}	I/O55													I/O145	V _{CC}	I/O180	I/O191	V
W	GND	I/O29	I/O43	I/O56													I/O146	I/O163	I/O181	GND	W
Y	GND	I/O30	GND	I/O57													I/O147	GND	I/O182	I/O192	Y

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

Select devices have been discontinued.
See Ordering Information section for product status.

20446G-026

256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (Macrocell Association)

256-Ball BGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
	GND	GND	GND	3B13	4B14	GND	4B8	4B4	GND	GND	GND	GND	4A4	4A8	GND	4A14	0B13	GND	0B2	GND	A	GND	3B1	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2A10	2D13	2D15	GND	GND																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
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_{CC}	4B10	4B9	4B13	4B7	4B5	4B1	4A2	4A7	4A12	4A5	4A3	4A0	4B1	4B3	4B6	4B10	4B11	4B15	4B14	4B13	4B12	4B11	4B10	4B9	4B8	4B7	4B6	4B5	4B4	4B3	4B2	4B1	4A0	4A1	4A2	4A3	4A4	4A5	4A6	4A7	4A8	4A9	4A10	4A11	4A12	4A13	4A14	4A15	4A16	4A17	4A18	4A19	4A20	4A21	4A22	4A23	4A24	4A25	4A26	4A27	4A28	4A29	4A30	4A31	4A32	4A33	4A34	4A35	4A36	4A37	4A38	4A39	4A40	4A41	4A42	4A43	4A44	4A45	4A46	4A47	4A48	4A49	4A50	4A51	4A52	4A53	4A54	4A55	4A56	4A57	4A58	4A59	4A60	4A61	4A62	4A63	4A64	4A65	4A66	4A67	4A68	4A69	4A70	4A71	4A72	4A73	4A74	4A75	4A76	4A77	4A78	4A79	4A80	4A81	4A82	4A83	4A84	4A85	4A86	4A87	4A88	4A89	4A90	4A91	4A92	4A93	4A94	4A95	4A96	4A97	4A98	4A99	4A100	4A101	4A102	4A103	4A104	4A105	4A106	4A107	4A108	4A109	4A110	4A111	4A112	4A113	4A114	4A115	4A116	4A117	4A118	4A119	4A120	4A121	4A122	4A123	4A124	4A125	4A126	4A127	4A128	4A129	4A130	4A131	4A132	4A133	4A134	4A135	4A136	4A137	4A138	4A139	4A140	4A141	4A142	4A143	4A144	4A145	4A146	4A147	4A148	4A149	4A150	4A151	4A152	4A153	4A154	4A155	4A156	4A157	4A158	4A159	4A160	4A161	4A162	4A163	4A164	4A165	4A166	4A167	4A168	4A169	4A170	4A171	4A172	4A173	4A174	4A175	4A176	4A177	4A178	4A179	4A180	4A181	4A182	4A183	4A184	4A185	4A186	4A187	4A188	4A189	4A190	4A191	4A192	4A193	4A194	4A195	4A196	4A197	4A198	4A199	4A200	4A201	4A202	4A203	4A204	4A205	4A206	4A207	4A208	4A209	4A210	4A211	4A212	4A213	4A214	4A215	4A216	4A217	4A218	4A219	4A220	4A221	4A222	4A223	4A224	4A225	4A226	4A227	4A228	4A229	4A230	4A231	4A232	4A233	4A234	4A235	4A236	4A237	4A238	4A239	4A240	4A241	4A242	4A243	4A244	4A245	4A246	4A247	4A248	4A249	4A250	4A251	4A252	4A253	4A254	4A255	4A256	4A257	4A258	4A259	4A260	4A261	4A262	4A263	4A264	4A265	4A266	4A267	4A268	4A269	4A270	4A271	4A272	4A273	4A274	4A275	4A276	4A277	4A278	4A279	4A280	4A281	4A282	4A283	4A284	4A285	4A286	4A287	4A288	4A289	4A290	4A291	4A292	4A293	4A294	4A295	4A296	4A297	4A298	4A299	4A300	4A301	4A302	4A303	4A304	4A305	4A306	4A307	4A308	4A309	4A310	4A311	4A312	4A313	4A314	4A315	4A316	4A317	4A318	4A319	4A320	4A321	4A322	4A323	4A324	4A325	4A326	4A327	4A328	4A329	4A330	4A331	4A332	4A333	4A334	4A335	4A336	4A337	4A338	4A339	4A340	4A341	4A342	4A343	4A344	4A345	4A346	4A347	4A348	4A349	4A350	4A351	4A352	4A353	4A354	4A355	4A356	4A357	4A358	4A359	4A360	4A361	4A362	4A363	4A364	4A365	4A366	4A367	4A368	4A369	4A370	4A371	4A372	4A373	4A374	4A375	4A376	4A377	4A378	4A379	4A380	4A381	4A382	4A383	4A384	4A385	4A386	4A387	4A388	4A389	4A390	4A391	4A392	4A393	4A394	4A395	4A396	4A397	4A398	4A399	4A400	4A401	4A402	4A403	4A404	4A405	4A406	4A407	4A408	4A409	4A410	4A411	4A412	4A413	4A414	4A415	4A416	4A417	4A418	4A419	4A420	4A421	4A422	4A423	4A424	4A425	4A426	4A427	4A428	4A429	4A430	4A431	4A432	4A433	4A434	4A435	4A436	4A437	4A438	4A439	4A440	4A441	4A442	4A443	4A444	4A445	4A446	4A447	4A448	4A449	4A450	4A451	4A452	4A453	4A454	4A455	4A456	4A457	4A458	4A459	4A460	4A461	4A462	4A463	4A464	4A465	4A466	4A467	4A468	4A469	4A470	4A471	4A472	4A473	4A474	4A475	4A476	4A477	4A478	4A479	4A480	4A481	4A482	4A483	4A484	4A485	4A486	4A487	4A488	4A489	4A490	4A491	4A492	4A493	4A494	4A495	4A496	4A497	4A498	4A499	4A500	4A501	4A502	4A503	4A504	4A505	4A506	4A507	4A508	4A509	4A510	4A511	4A512	4A513	4A514	4A515	4A516	4A517	4A518	4A519	4A520	4A521	4A522	4A523	4A524	4A525	4A526	4A527	4A528	4A529	4A530	4A531	4A532	4A533	4A534	4A535	4A536	4A537	4A538	4A539	4A540	4A541	4A542	4A543	4A544	4A545	4A546	4A547	4A548	4A549	4A550	4A551	4A552	4A553	4A554	4A555	4A556	4A557	4A558	4A559	4A560	4A561	4A562	4A563	4A564	4A565	4A566	4A567	4A568	4A569	4A570	4A571	4A572	4A573	4A574	4A575	4A576	4A577	4A578	4A579	4A580	4A581	4A582	4A583	4A584	4A585	4A586	4A587	4A588	4A589	4A590	4A591	4A592	4A593	4A594	4A595	4A596	4A597	4A598	4A599	4A600	4A601	4A602	4A603	4A604	4A605	4A606	4A607	4A608	4A609	4A610	4A611	4A612	4A613	4A614	4A615	4A616	4A617	4A618	4A619	4A620	4A621	4A622	4A623	4A624	4A625	4A626	4A627	4A628	4A629	4A630	4A631	4A632	4A633	4A634	4A635	4A636	4A637	4A638	4A639	4A640	4A641	4A642	4A643	4A644	4A645	4A646	4A647	4A648	4A649	4A650	4A651	4A652	4A653	4A654	4A655	4A656	4A657	4A658	4A659	4A660	4A661	4A662	4A663	4A664	4A665	4A666	4A667	4A668	4A669	4A670	4A671	4A672	4A673	4A674	4A675	4A676	4A677	4A678	4A679	4A680	4A681	4A682	4A683	4A684	4A685	4A686	4A687	4A688	4A689	4A690	4A691	4A692	4A693	4A694	4A695	4A696	4A697	4A698	4A699	4A700	4A701	4A702	4A703	4A704	4A705	4A706	4A707	4A708	4A709	4A710	4A711	4A712	4A713	4A714	4A715	4A716	4A717	4A718	4A719	4A720	4A721	4A722	4A723	4A724	4A725	4A726	4A727	4A728	4A729	4A730	4A731	4A732	4A733	4A734	4A735	4A736	4A737	4A738	4A739	4A740	4A741	4A742	4A743	4A744	4A745	4A746	4A747	4A748	4A749	4A750	4A751	4A752	4A753	4A754	4A755	4A756	4A757	4A758	4A759	4A760	4A761	4A762	4A763	4A764	4A765	4A766	4A767	4A768	4A769	4A770	4A771	4A772	4A773	4A774	4A775	4A776	4A777	4A778	4A779	4A780	4A781	4A782	4A783	4A784	4A785	4A786	4A787	4A788	4A789	4A790	4A791	4A792	4A793	4A794	4A795	4A796	4A797	4A798	4A799	4A800	4A801	4A802	4A803	4A804	4A805	4A806	4A807	4A808	4A809	4A810	4A811	4A812	4A813	4A814	4A815	4A816	4A817	4A818	4A819	4A820	4A821	4A822	4A823	4A824	4A825	4A826	4A827	4A828	4A829	4A830	4A831	4A832	4A833	4A834	4A835	4A836	4A837	4A838	4A839	4A840	4A841	4A842	4A843	4A844	4A845	4A846	4A847	4A848	4A849	4A850	4A851	4A852	4A853	4A854	4A855	4A856	4A857	4A858	4A859	4A860	4A861	4A862	4A863	4A864	4A865	4A866	4A867	4A868	4A869	4A870	4A871	4A872	4A873	4A874	4A875	4A876	4A877	4A878	4A879	4A880	4A881	4A882	4A883	4A884	4A885	4A886	4A887	4A888	4A889	4A890	4A891	4A892	4A893	4A894	4A895	4A896	4A897	4A898	4A899	4A900	4A901	4A902	4A903	4A904	4A905	4A906	4A907	4A908	4A909	4A910	4A911	4A912	4A913	4A914	4A915	4A916	4A917	4A918	4A919	4A920	4A921	4A922	4A923	4A924	4A925	4A926	4A927	4A928	4A929	4A930	4A931	4A932	4A933	4A934	4A935	4A936	4A937	4A938	4A939	4A940	4A941	4A942	4A943	4A944	4A945	4A946	4A947	4A948	4A949	4A950	4A951	4A952	4A953	4A954	4A955	4A956	4A957	4A958	4A959	4A960	4A961	4A962	4A963	4A964	4A965	4A966	4A967	4A968	4A969	4A970	4A971	4A972	4A973	4A974	4A975	4A976	4A977	4A978	4A979	4A980	4A981	4A982	4A983	4A984	4A985	4A986	4A987	4A988	4A989	4A990	4A991	4A992	4A993	4A994	4A995	4A996	4A997	4A998	4A999	4A1000	4A1001	4A1002	4A1003	4A1004	4A1005	4A1006	4A1007	4A1008	4A1009	4A1010	4A1011	4A1012	4A1013	4A1014	4A1015	4A1016	4A1017	4A1018	4A1019	4A1020	4A1021	4A1022	4A1023	4A1024	4A1025	4A1026	4A1027	4A1028	4A1029	4A1030	4A1031	4A1032	4A1033	4A1034	4A1035	4A1036	4A1037	4A1038	4A1039	4A1040	4A1041	4A1042	4A1043	4A1044	4A1045	4A1046	4A1047	4A1048	4A1049	4A1050	4A1051	4A1052	4A1053	4A1054	4A

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I/O233 I ₃ /CLK ₃	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O205	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	NC
3	GND	GND	NC	TDO	I/O189	I/O190	I/O191	V _{CC}	I/O192	V _{CC}	I/O193	I/O194	I/O195	V _{CC}	I/O196	I/O197	I/O198	V _{CC}	I/O199	V _{CC}	I/O200	I/O201	I/O223	TMS	NC	NC
4	NC	I/O188	NC	I/O184	I/O178	I/O177	I/O176	I/O175	I/O174	I/O173	I/O172	I/O171	I/O166	I/O165	I/O164	I/O163	I/O162	I/O161	I/O160	I/O159	I/O158	I/O157	I/O156	I/O155	I/O154	I/O153
5	GND	I/O183	I/O184	V _{CC}	I/O178	I/O177	I/O176	I/O175	I/O174	I/O173	I/O172	I/O171	I/O166	I/O165	I/O164	I/O163	I/O162	I/O161	I/O160	I/O159	I/O158	I/O157	I/O156	I/O155	I/O154	I/O153
6	NC	I/O176	I/O177	I/O178	I/O178	I/O177	I/O176	I/O175	I/O174	I/O173	I/O172	I/O171	I/O166	I/O165	I/O164	I/O163	I/O162	I/O161	I/O160	I/O159	I/O158	I/O157	I/O156	I/O155	I/O154	I/O153
7	GND	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187	I/O188	I/O189	I/O190	I/O191	I/O192	I/O193
8	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	I/O181	I/O182	I/O183	I/O184	I/O185	I/O186	I/O187
9	I/O156	I/O157	I/O158	I/O159	V _{CC}	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I/O172
10	GND	I/O150	I/O151	V _{CC}	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167
11	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	I/O163	I/O164	I/O165	I/O166	I/O167
12	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159
13	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145	I/O146	I/O147	I/O148	I/O149	I/O150	I/O151	I/O152	I/O153
14	GND	I/O122	I/O123	V _{CC}	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	I/O144	I/O145
15	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131	I/O132	I/O133	I/O134	I/O135	I/O136	I/O137	I/O138	I/O139
16	NC	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117	I/O118	I/O119	I/O120	I/O121	I/O122	I/O123	I/O124	I/O125	I/O126	I/O127	I/O128	I/O129	I/O130	I/O131
17	I/O101	I/O102	I/O103	I/O104	V _{CC}	I/O097	I/O098	I/O099	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105	I/O106	I/O107	I/O108	I/O109	I/O110	I/O111	I/O112	I/O113	I/O114	I/O115	I/O116	I/O117
18	GND	I/O87	I/O88	V _{CC}	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105
19	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98	I/O99	I/O100	I/O101	I/O102	I/O103	I/O104	I/O105
20	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91	I/O92	I/O93	I/O94	I/O95	I/O96	I/O97	I/O98
21	GND	I/O68	I/O69	I/O70	V _{CC}	I/O71	I/O72	I/O73	I/O74	I/O75	I/O76	I/O77	I/O78	I/O79	I/O80	I/O81	I/O82	I/O83	I/O84	I/O85	I/O86	I/O87	I/O88	I/O89	I/O90	I/O91
22	I/O51	I/O52	I/O53	V _{CC}	I/O54	I/O55	V _{CC}	I/O56	V _{CC}	I/O57	I/O58	I/O59	V _{CC}	I/O60	I/O61	I/O62	V _{CC}	I/O63	V _{CC}	I/O64	I/O65	I/O66	TCK	NC	NC	NC
23	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	NC	NC	NC	NC
24	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	NC	NC	NC	NC
25	NC	NC	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0	I/O0
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	NC	NC	NC	NC	NC

Pin Designations

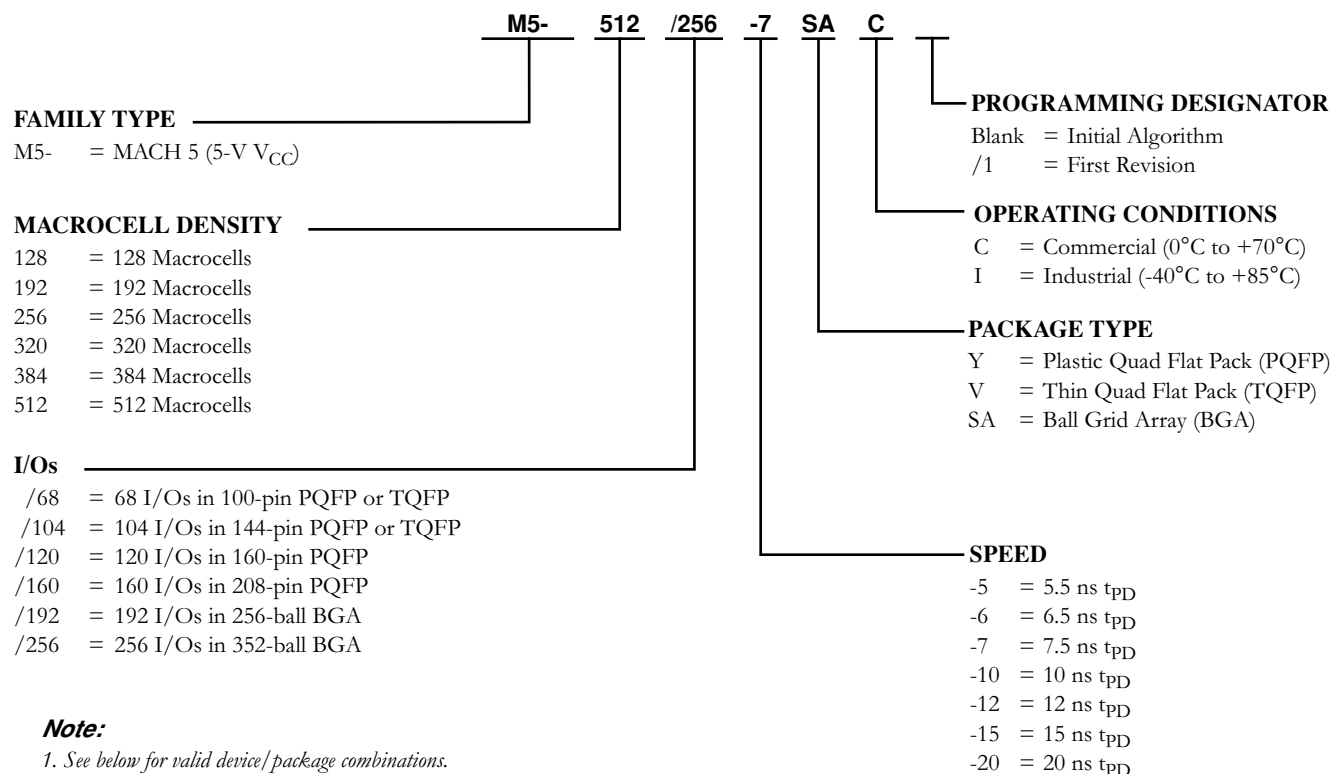
CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

20446G-030

Select devices have been discontinued.
See Ordering Information section for product status.

5V M5 ORDERING INFORMATION^{1,2}

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

- See below for valid device/package combinations.
- M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC ¹ , YI ¹
M5-128/120		YC, YI
M5-192/68		VC, VI
M5-192/120		YC, YI
M5-256/68		VC, VI
M5-256/120		YC, YI
M5-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

1. M5-128/104-xxYC/1 and M5-128/104-xxYI/1 have been discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Valid Combinations		
M5-320/160	Commercial: -6, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, YI
M5-320/192		SAC, SAI
M5-384/160		YC, YI
M5-512/160		YC, YI
M5-512/256		SAC, SAI

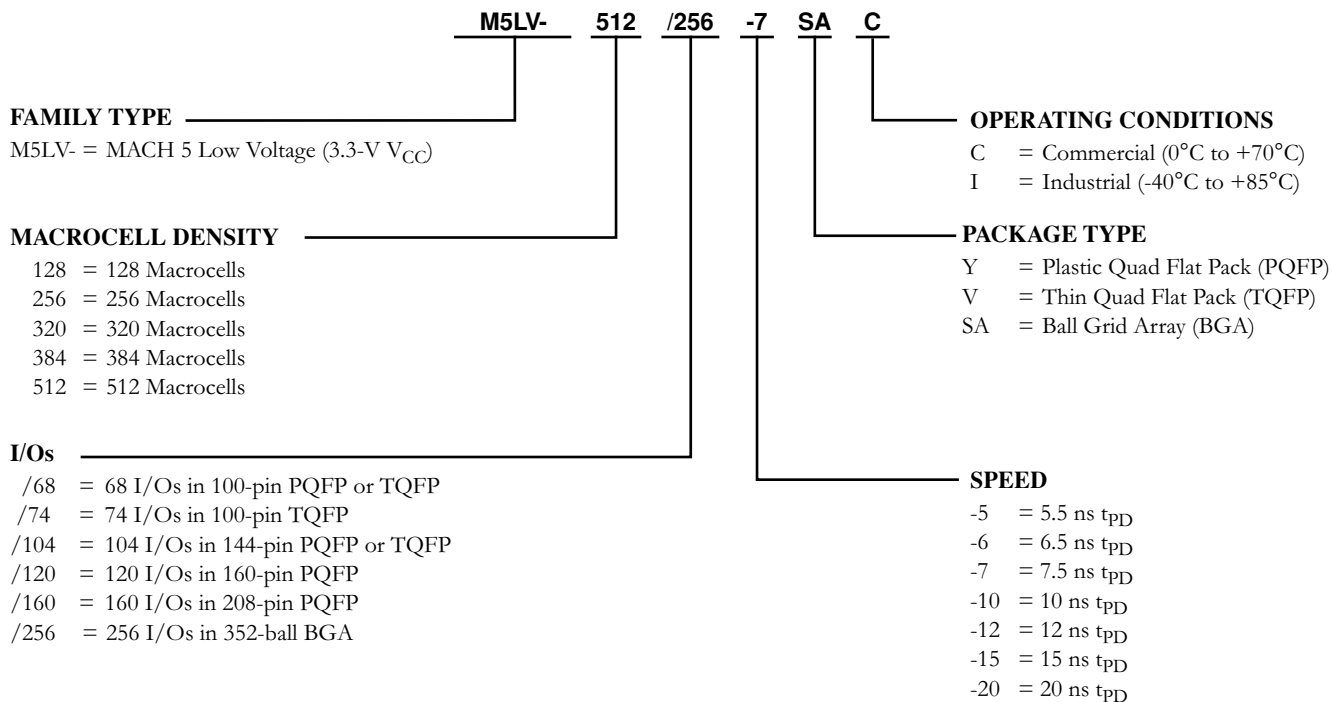
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.

3.3V M5LV ORDERING INFORMATION¹

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:

1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12	VC, VI
M5LV-128/74		VC, VI
M5LV-128/104		VC, VI
M5LV-128/120		YC, YI
M5LV-256/68	Industrial: -7, -10, -12, -15	YC, YI
M5LV-256/74		VC, VI
M5LV-256/104		VC, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15	YC, YI
M5LV-320/160		YC, YI
M5LV-384/120		YC, YI
M5LV-384/160		YC, YI
M5LV-512/120	Industrial: -10, -12, -15, -20	YC, YI
M5LV-512/160		YC, YI
M5LV-512/256		SAC, SAI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Select devices have been discontinued.
See Ordering Information section for product status.