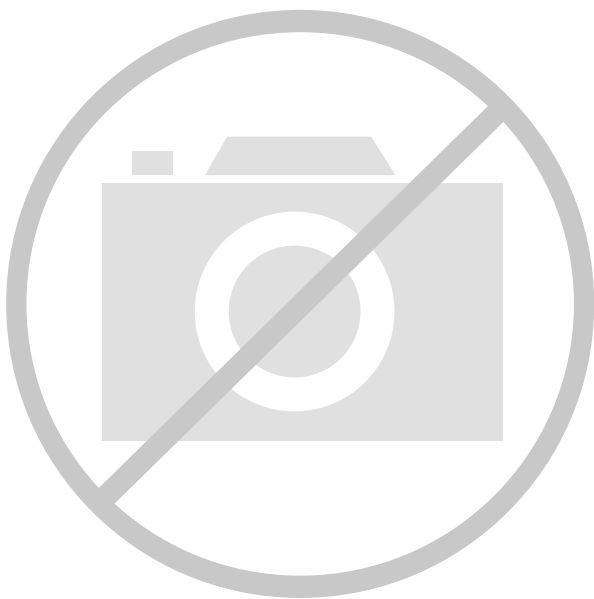




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

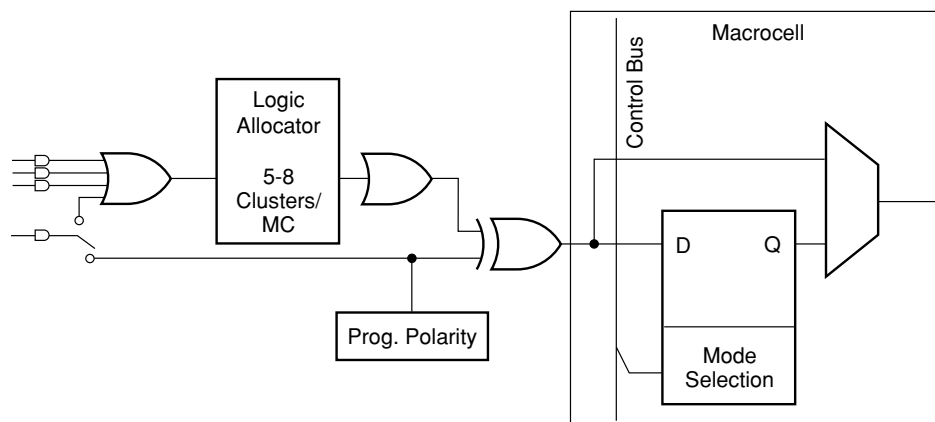
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	512
Number of Gates	-
Number of I/O	160
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-512-160-7yi

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The

I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as “buried” macrocells to drive device logic via the matrix.



20446G-003

Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- ◆ Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- ◆ Product-term clock ($A*B*C$)
- ◆ Sum-term clock ($A+B+C$)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.
See Ordering Information section for product status.

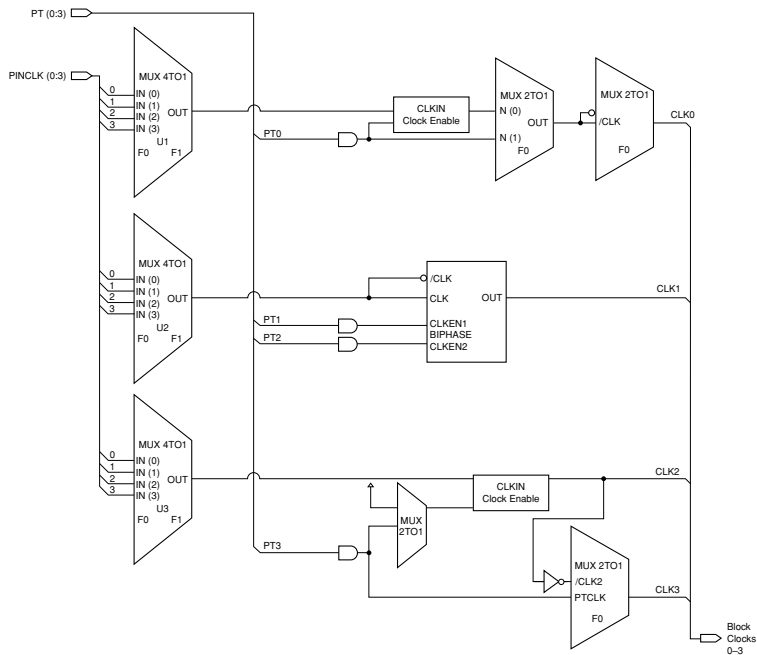
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

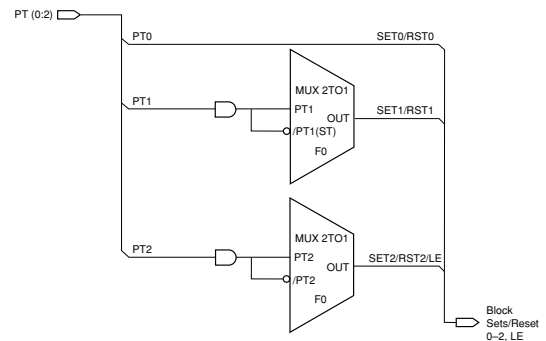
Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable)



20446G-004

Figure 4. Clock Generator



20446G-005

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

**Select devices have been discontinued.
See Ordering Information section for product status.**

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

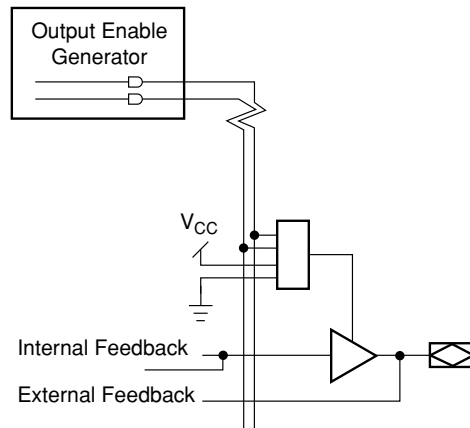
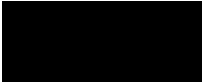


Figure 6. Output Enable Generator and I/O Cell

20446G-006

Select devices have been discontinued.
See Ordering Information section for product status.



MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

Select devices have been discontinued.
See Ordering Information section for product status.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS ¹

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

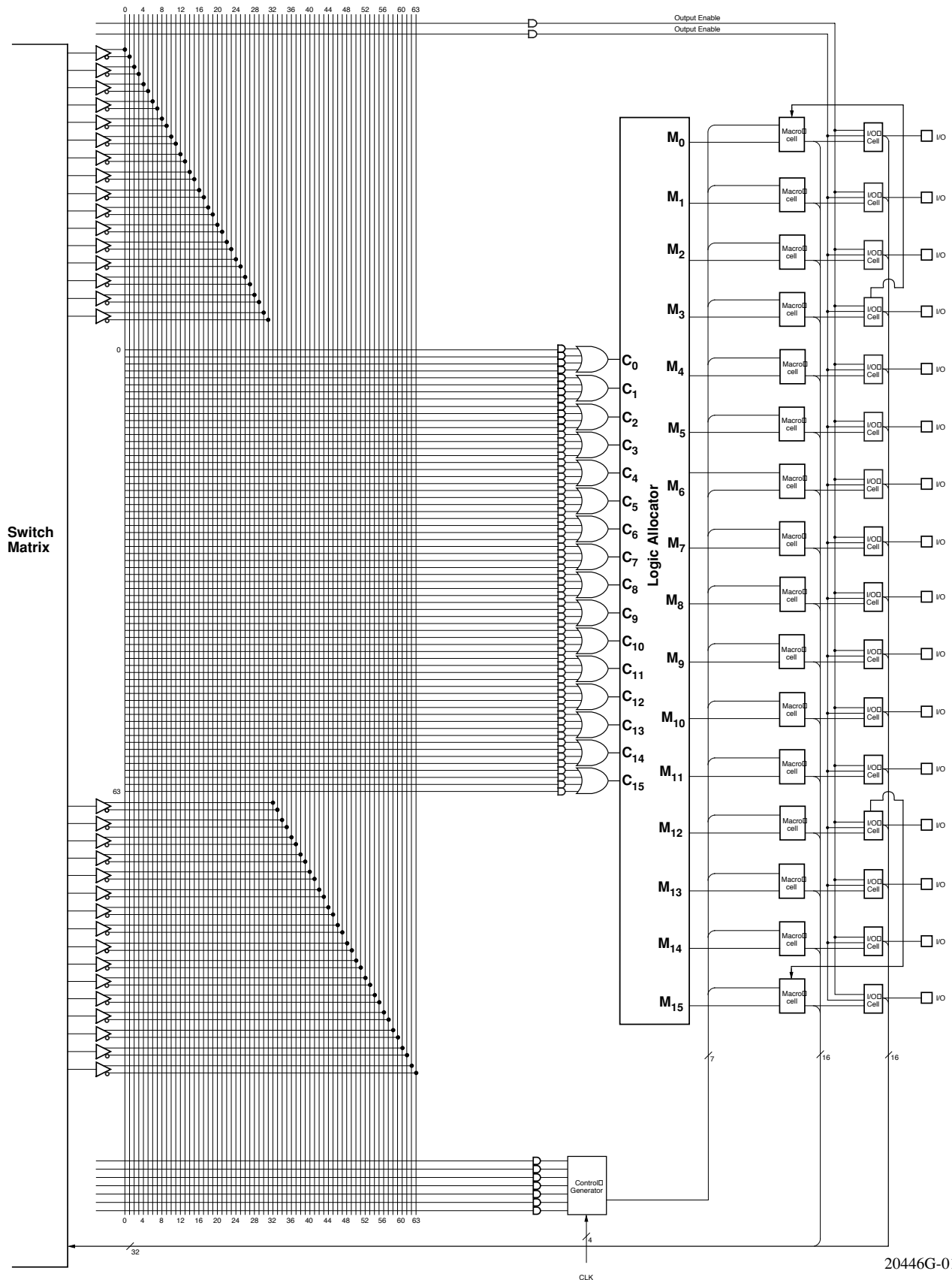
Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

Select devices have been discontinued. See Ordering Information section for product status.

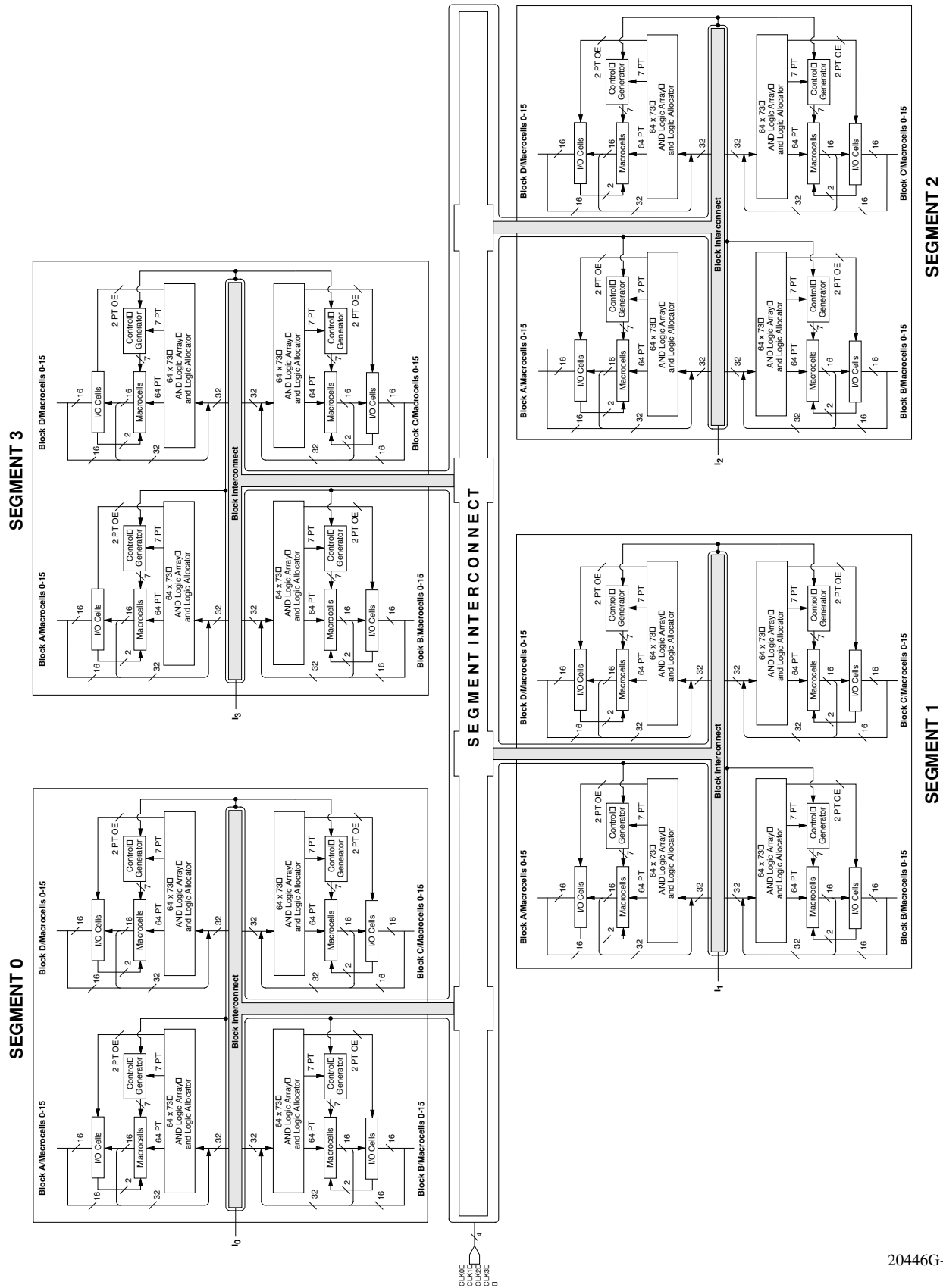
MACH 5 PAL BLOCK



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-015

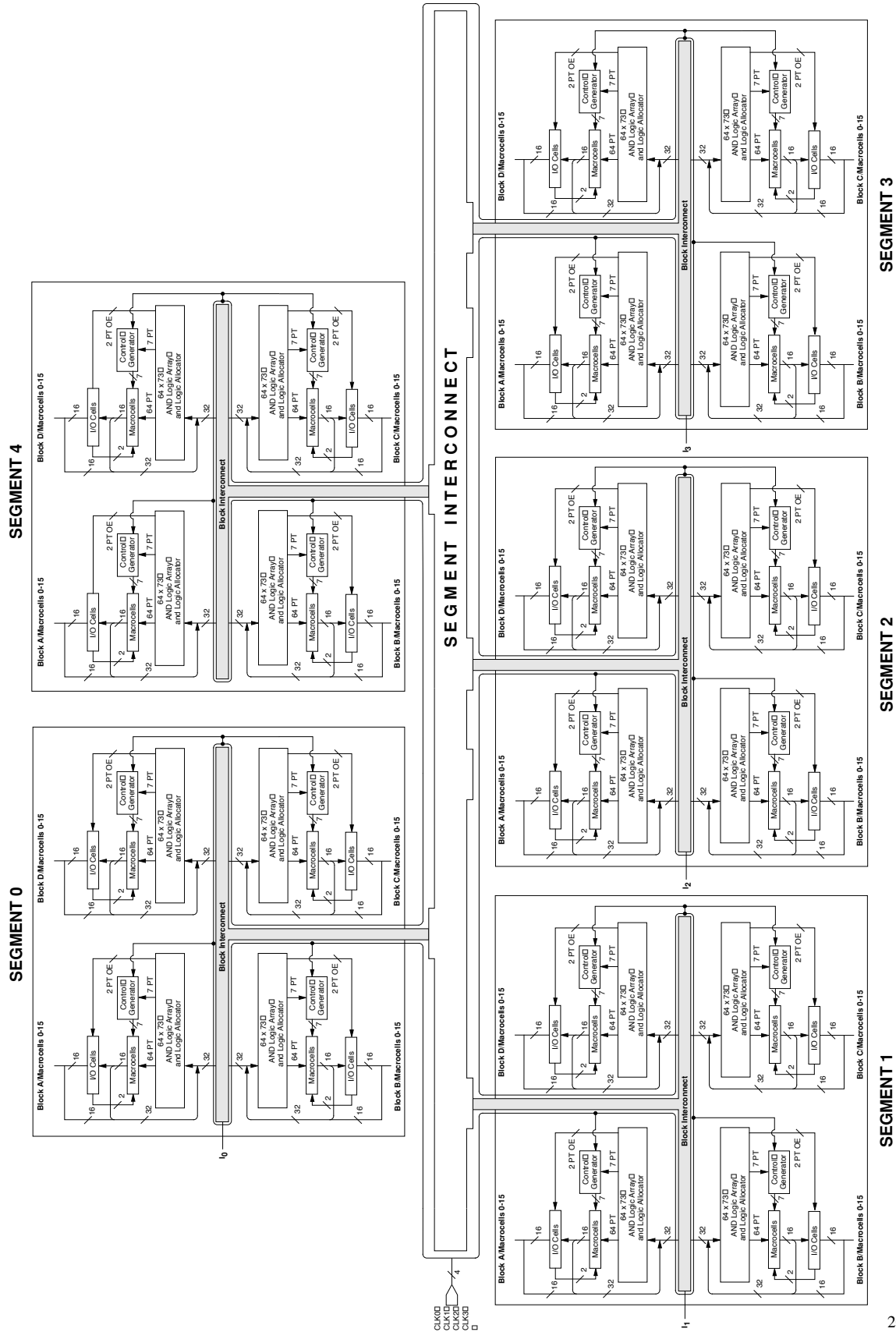
BLOCK DIAGRAM — M5(LV)-256/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-009

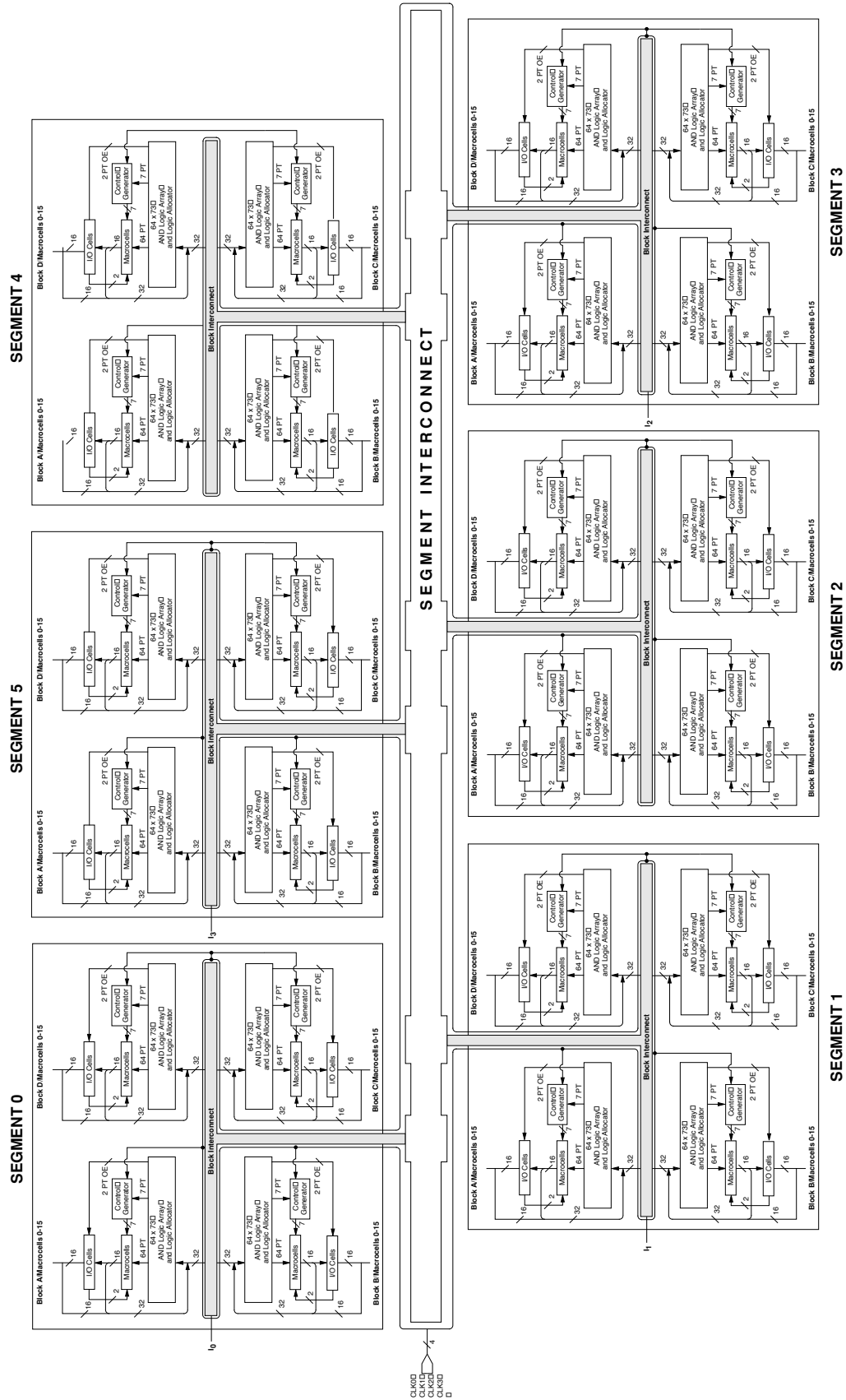
BLOCK DIAGRAM — M5(LV)-320/XXX



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-010

BLOCK DIAGRAM — M5(LV)-384/XXX

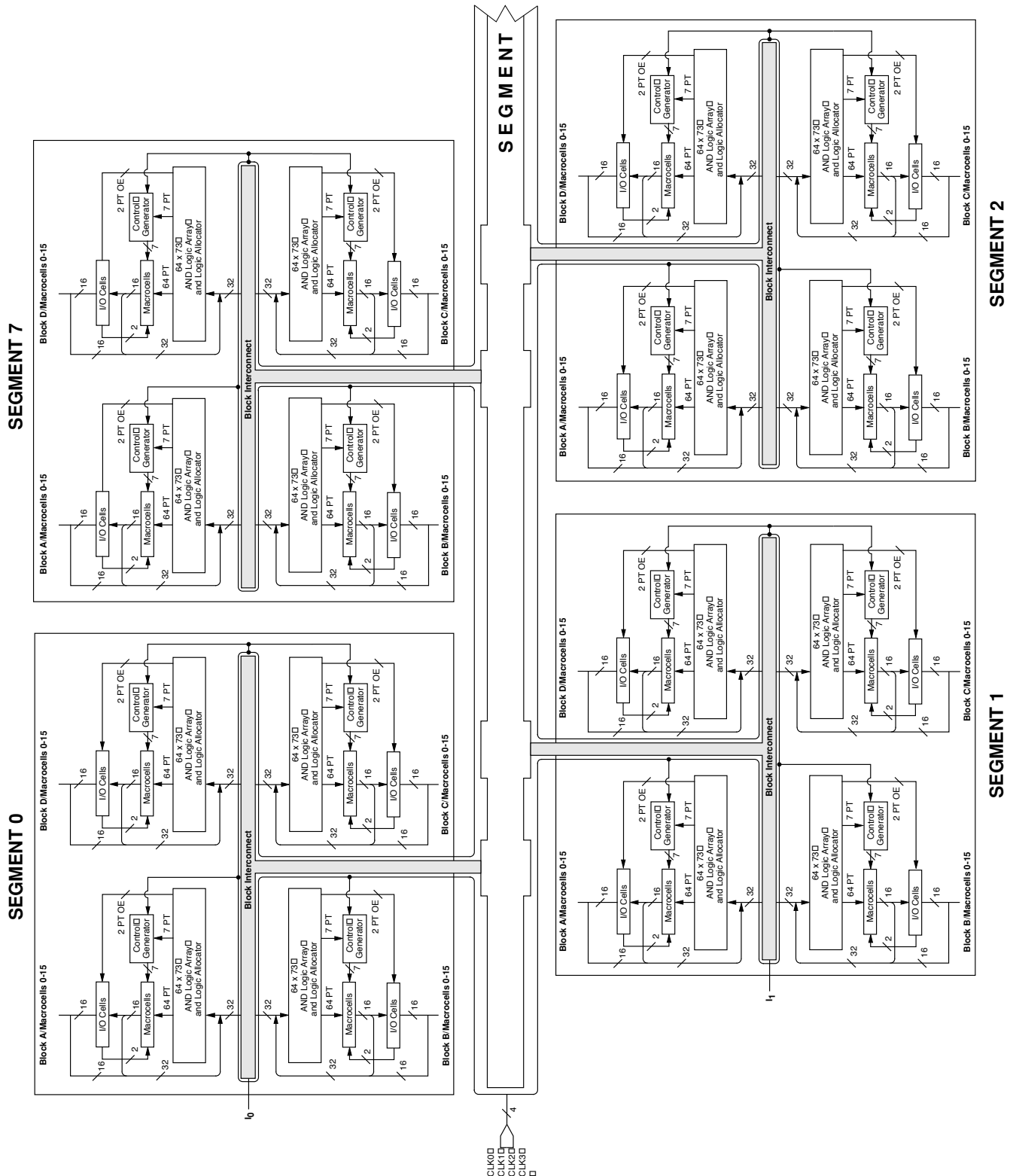


20446G-011

Select devices have been discontinued.
See Ordering Information section for product status.

BLOCK DIAGRAM — M5(LV)-512/XXX

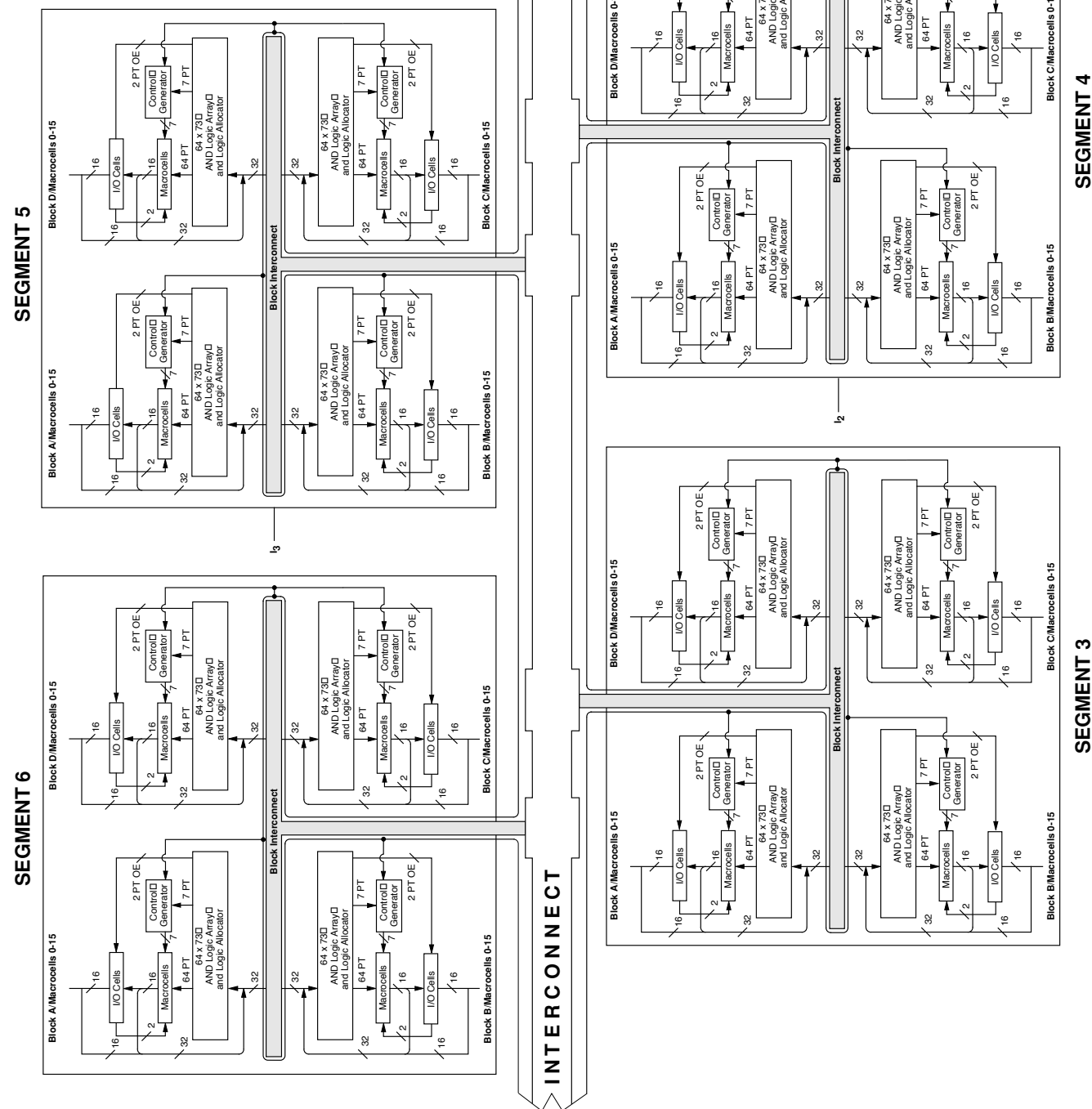
Continued



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-012

BLOCK DIAGRAM — M5(LV)-512/XXX



Continued

Select devices have been discontinued.
See Ordering Information section for product status.

ABSOLUTE MAXIMUM RATINGS

M5

Storage Temperature. -65°C to +150°C
 Device Junction
 Temperature (Note 1) +130°C or +150°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to 5.5 V
 Static Discharge Voltage 2000 V
 Latchup Current (-40°C to +85°C) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Select devices have been discontinued.
See Ordering Information section for product status.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = -100 \mu\text{A}$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL}		3.3	3.6	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	$I_{OH} = -3.2 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = -2.5 \text{ mA}$, $V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{IH}$ or V_{IL}			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	$I_{OL} = +16 \text{ mA}$, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$, $V_{CC} = \text{Max}$ (Note 4)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$, $V_{CC} = \text{Max}$ (Note 4)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5 V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 5)	-30		-180	mA

Note:

- 150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.
- Total I_{OL} between ground pins should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH} .
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Delays:																
t _{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t _{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t _{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t _{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t _{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t _{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t _{SRI}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t _{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t _{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t _{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t _{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t _{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t _{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

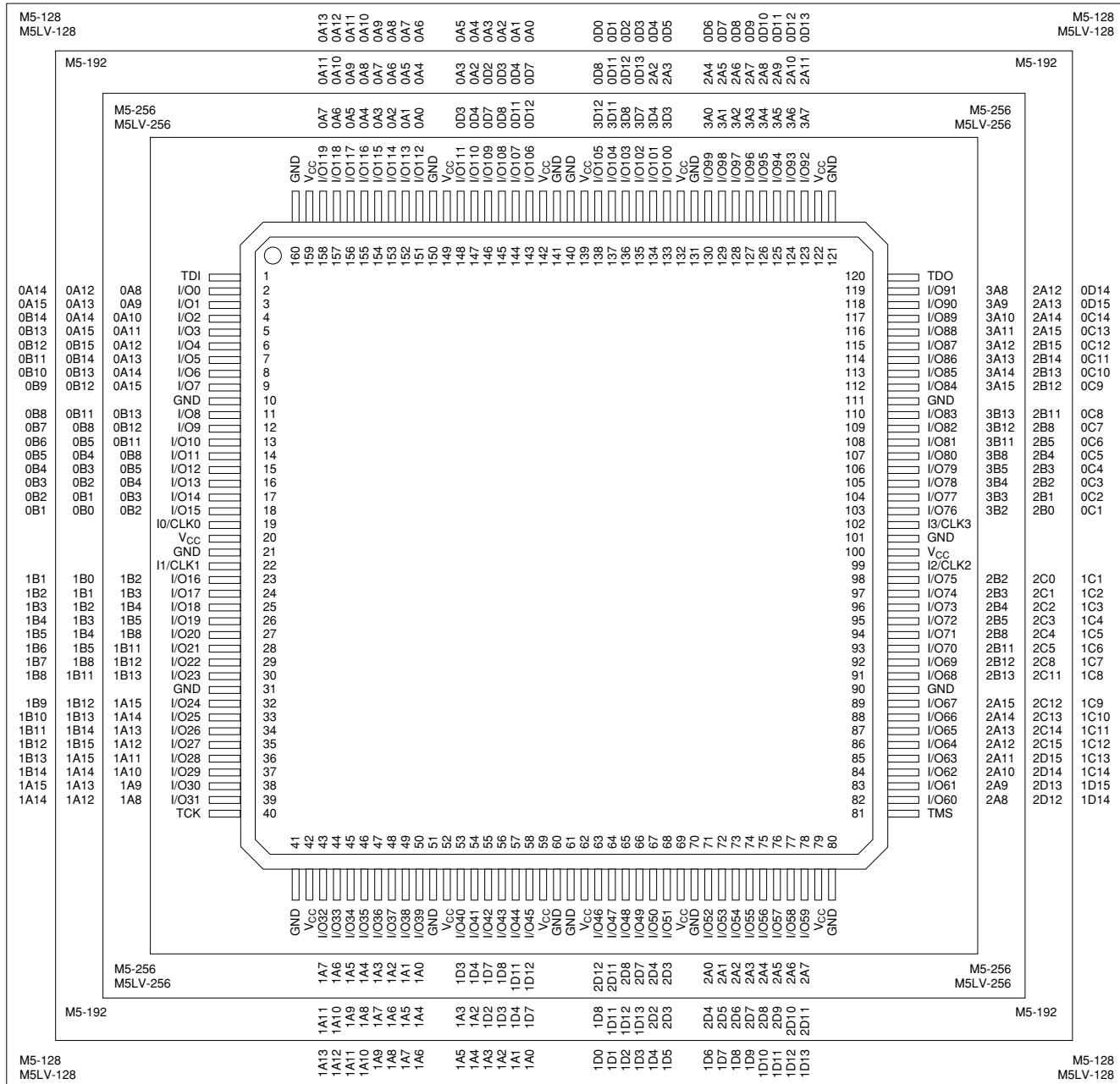
Select devices have been discontinued.
See Ordering Information section for product status.

160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

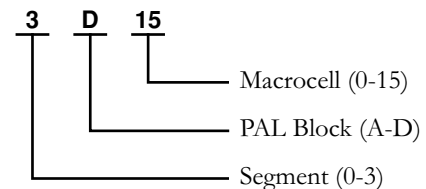
Select devices have been discontinued.
See Ordering Information section for product status.



Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

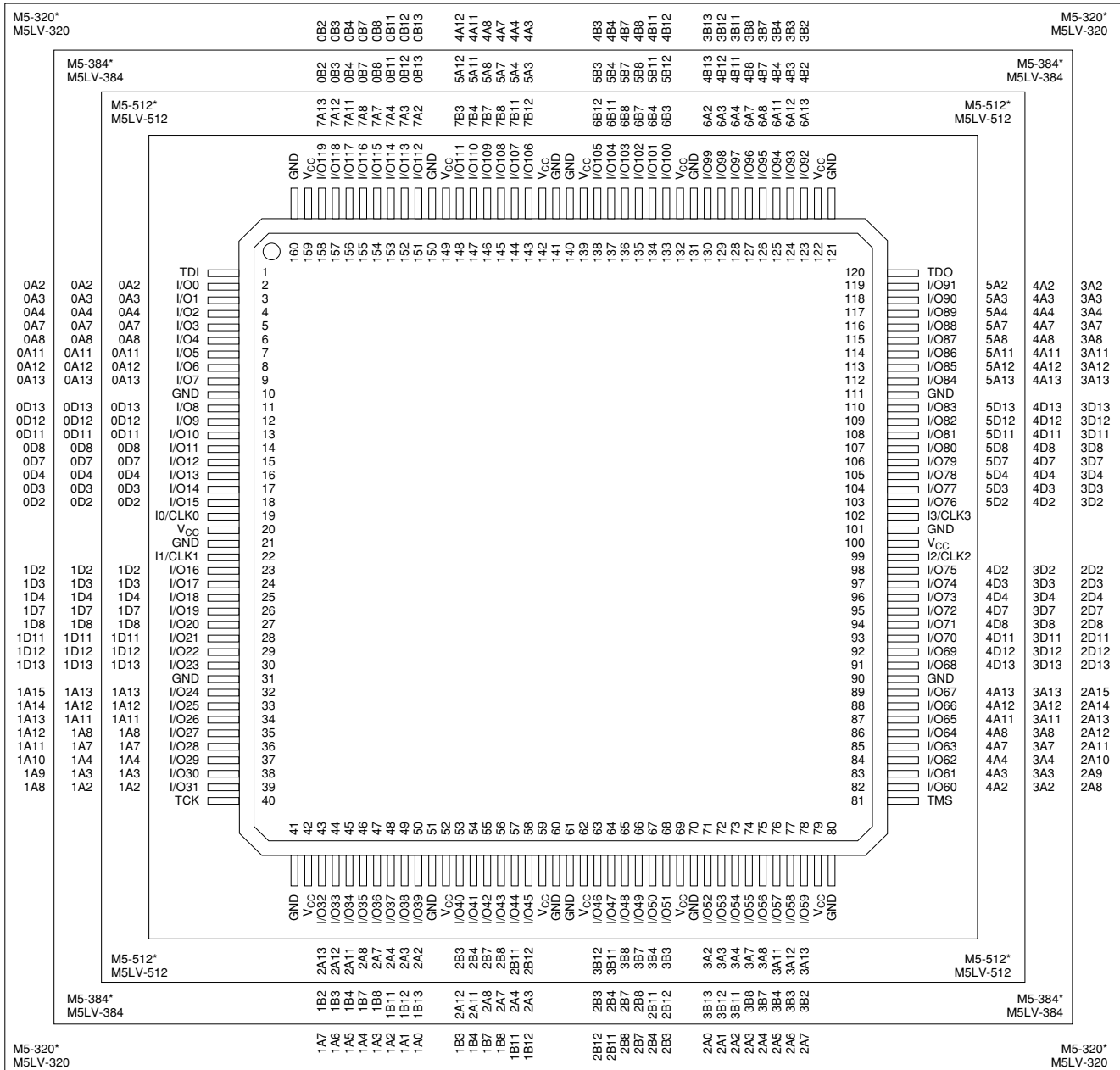
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM

Top View

160-Pin PQFP (320, 384, 512 Macrocells)



Select devices have been discontinued.
See Ordering Information section for product status.

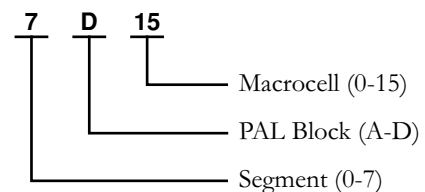
*Package obsolete, contact factory.

20446G-022

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect

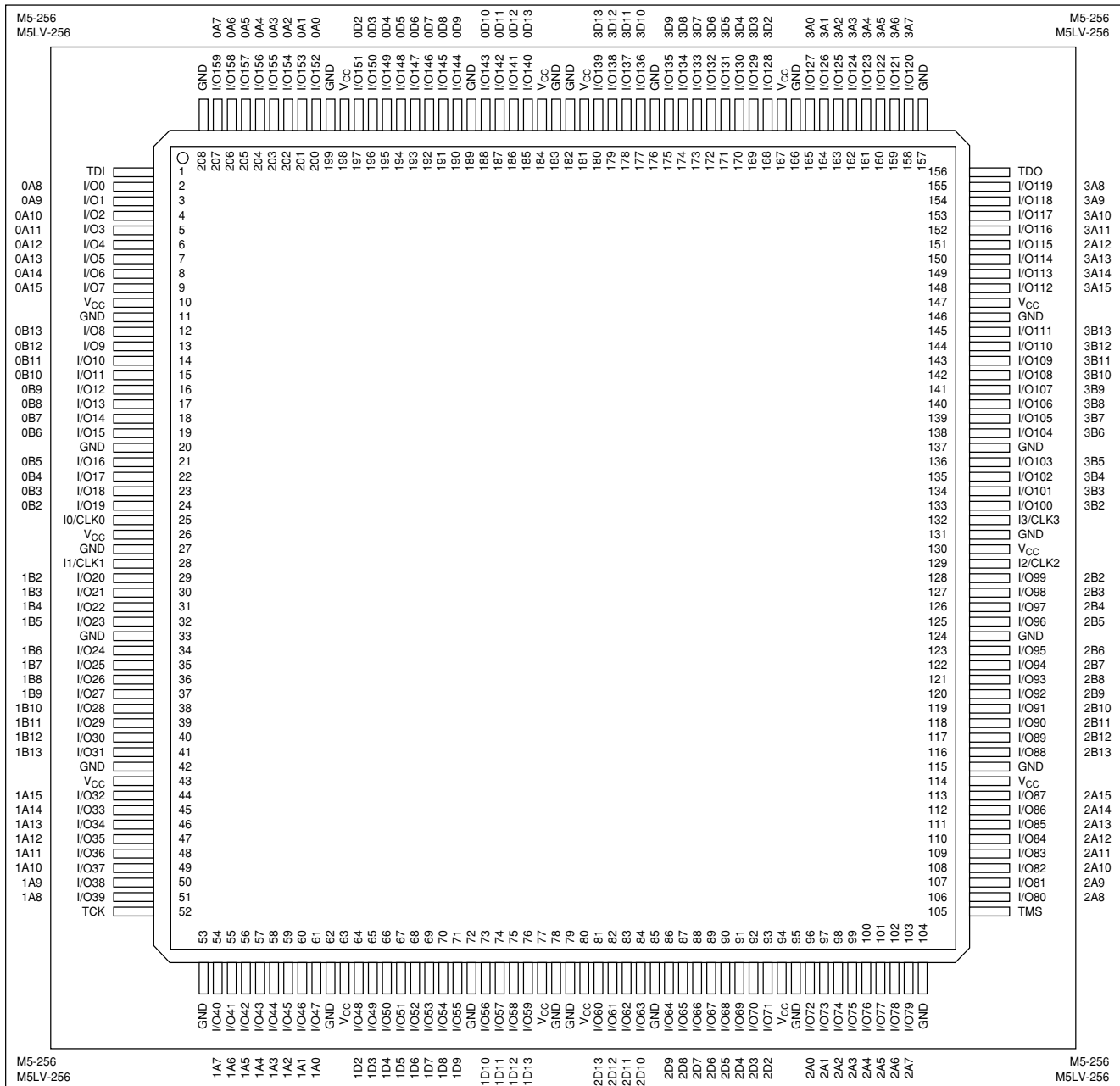
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (256 Macrocells)

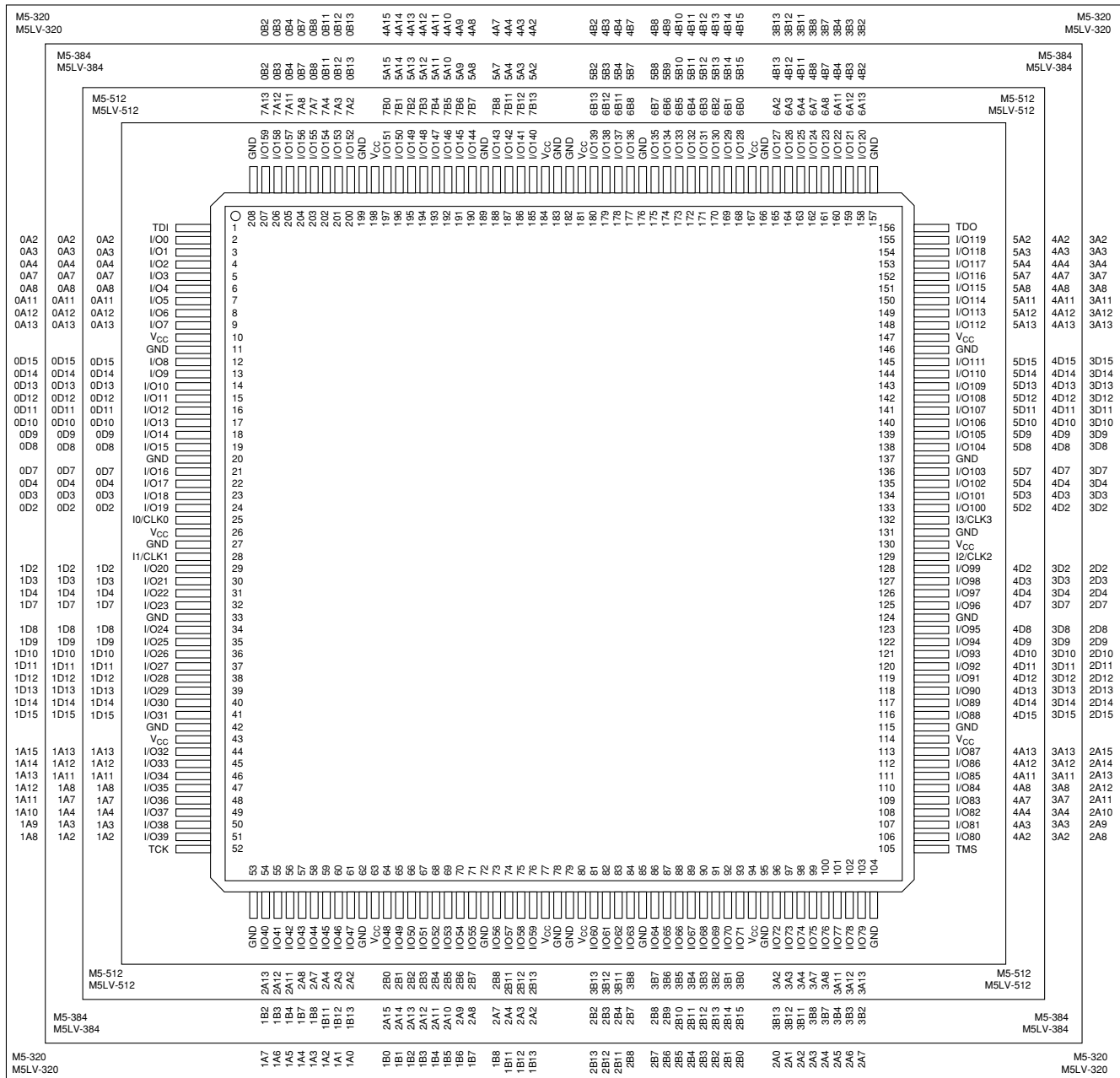


Select devices have been discontinued.
See Ordering Information section for product status.

20446G-023

208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM Top View

208-Pin PQFP (320, 384, 512 Macrocells)



Select devices have been discontinued.
See Ordering Information section for product status.

20446G-024

256-BALL BGA CONNECTION DIAGRAM — M5-320

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2D10	2D13	2D15	GND	GND	1
2	GND	3B2	3A3	3A8	3A13	3D13	3D9	3D8	3D4	13/CLK3	12/CLK2	2D3	2D4	2D8	2D12	2A15	2A13	2A12	2A9	2A7	2
3	GND	3B8	V _{CC}	3A2	3A4	3A12	3D14	3D10	3D5	3D0	2D0	2D5	2D9	2D14	2A14	2A10	2A8	V _{CC}	2A3	GND	3
4	3B13	3B11	3B3	V _{CC}	TDO	3A7	V _{CC}	3D11	3D6	3D1	2D1	2D6	2D11	V _{CC}	2A11	TMS	V _{CC}	2A6	2A2	2A0	4
5	4B14	4B15	3B4	V _{CC}	Pin Designations CLK = Clock GND = Ground I = Input I/O = Input/Output NC = No Connect V_{CC} = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out 4 D 15 Macrocell (0-15) PAL Block (A-D) Segment (0-4)	4B8	4B10	4B13	V _{CC}	2A4	2A1	2B0	2B1	5							
6	GND	4B11	3B12	3B7		V _{CC}	2B3	2B6	2B9	2B11	6										
7	4B8	4B10	4B13	V _{CC}		V _{CC}	2B2	2B5	2B7	7											
8	4B4	4B6	4B9	4B12		2B8	2B10	2B12	GND	8											
9	GND	4B3	4B5	4B7		2B13	2B14	2B15	GND	9											
10	GND	4B0	4B1	4B2		1B13	1B14	1B15	GND	10											
11	GND	4A0	4A1	4A2		1B8	1B10	1B12	GND	11											
12	GND	4A3	4A5	4A7		1B3	1B6	1B9	1B11	12											
13	4A4	4A6	4A9	4A12		V _{CC}	1B2	1B5	1B7	13											
14	4A8	4A10	4A13	V _{CC}		1A4	1A1	1B4	GND	14											
15	GND	4A11	0B12	0B7		V _{CC}	1A5	1B0	1B1	15											
16	4A14	4A15	0B4	V _{CC}		0B13	0B11	0B3	V _{CC}	16											
17	0B13	0B11	0B3	V _{CC}	TDI	0A7	V _{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V _{CC}	1A11	TCK	V _{CC}	1A6	1A2	1A0	17
18	GND	0B8	V _{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A14	1A10	1A8	V _{CC}	1A3	GND	18
19	0B2	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	10/CLK0	11/CLK1	1D4	1D8	1D9	1D13	1A15	1A12	1A9	1A7	GND	19
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A13	GND	GND	20

Select devices have been discontinued.
See Ordering Information section for product status.

352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (Macrocell Association)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A14	3A15	3A13	3A12
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	NC	NC
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I ₂ /CLK ₂	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	NC
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V _{CC}	5A11	V _{CC}	5D12	5D7	5D2	V _{CC}	4D3	4D8	4D12	V _{CC}	4A11	V _{CC}	4A4	4A0	V _{CC}	3A14	3A15	3A13	3A12
5	GND	6A12	6A13	V _{CC}																			3A14	3A11	3A9	GND	GND
6	NC	6A9	6A10	6A15																			3A10	3A8	3A7	3A5	
7	GND	6A6	6A8	6A11																			3A6	3A4	3A3	3A0	
8	6A1	6A4	6A5	6A7																			3A2	3A1	3B0	NC	
9	6B1	6A0	6A2	6A3																			V _{CC}	3B1	3B2	GND	
10	GND	6B2	6B0	V _{CC}																			3B3	3B4	3B5	3B6	
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	3B10	
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B14	
13	6B14	6B13	6B12	6B11																			V _{CC}	2B15	3B15	GND	3B14
14	GND	7B15	6B15	V _{CC}																			2B11	2B12	2B13	2B14	
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10	
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6	
17	7B7	7B6	7B5	7B4																			V _{CC}	2B0	2B2	GND	
18	GND	7B3	7B2	V _{CC}																			2A3	2A2	2A0	2B1	
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1	
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND	
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC	
22	GND	7A9	7A11	7A15																			V _{CC}	2A13	2A12	GND	
23	7A10	7A13	7A14	V _{CC}				0A11	V _{CC}	0D14	0D8	0D3	V _{CC}	1D2	1D7	1D12	V _{CC}	1A11	V _{CC}	1A6	1A3	1A0	TCK	NC	2A14	NC	
24	NC	NC	TDI	0A2	0A5	0A7	0A10	0A14	0D13	0D11	0D7	0D4	I ₀ /CLK ₀	1D1	1D5	1D9	1D14	1A13	1A10	1A8	1A7	1A4	1A1	NC	GND	GND	
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D10	0D10	0D6	0D2	0D0	1D0	1D4	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	I ₁ /CLK ₁	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	

Pin Designations

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

NC = No Connect

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

7

D

15

Macrocell (0-15)

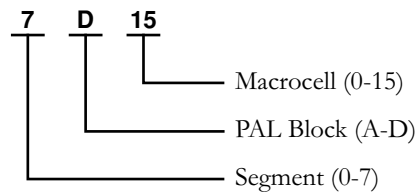
PAL Block (A-D)

Segment (0-7)

20446G-031

Pin Designations

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- NC = No Connect
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



20446G-031

Select devices have been discontinued.
See Ordering Information section for product status.