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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 20 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 512 |
| Number of Gates | - |
| Number of I/O | 256 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 352-LBGA |
| Supplier Device Package | 352-SBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/m5lv-512-256-20sai |

Table 1. MACH 5 Device Features [1]

| Feature | M5-128/1 M5LV-128 | | M5-192/1 | M5-256/1 M5LV-256 | | M5-320 M5LV-320 | | M5-384 M5LV-384 | | M5-512 M5LV-512 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage (V) | 5 | 3.3 | 5 | 5 | 3.3 | 5 | 3.3 | 5 | 3.3 | 5 | 3.3 |
| Macrocells | 128 | 128 | 192 | 256 | 256 | 320 | 320 | 384 | 384 | 512 | 512 |
| Maximum User I/O Pins | 120 | 120 | 120 | 160 | 160 | 192 | 160 | 160 | 160 | 256 | 256 |
| $t_{PD}$ (ns) | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | 6.5 | 6.5 | 6.5 | 6.5 | 6.5 | 6.5 |
| $t_{SS}$ (ns) | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 |
| $t_{COS}$ (ns) | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 |
| $f_{CNT}$ (MHz) | 182 | 182 | 182 | 182 | 182 | 167 | 167 | 167 | 167 | 167 | 167 |
| Typical Static Power (mA) | 35 | 35 | 45 | 55 | 55 | 70 | 70 | 75 | 75 | 100 | 100 |
| IEEE 1149.1 Boundary Scan Compliant | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PCI-Compliant | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

***Note:***

*1. "M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.*

## GENERAL DESCRIPTION

The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on $E^2$CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.

Select devices have been discontinued.
See Ordering Information section for product status.

**Table 2. MACH 5 Speed Grades**

| Device | Speed Grade[1] | | | | | | |
|---|---|---|---|---|---|---|---|
| | -5 | -6 | -7 | -10 | -12 | -15 | -20 |
| M5-128[2] | | | C | C, I | C, I | C, I | I |
| M5-128/1 | C | | C, I | C, I | C, I | C, I | I |
| M5LV-128 | C | | C,I | C, I | C, I | I | |
| M5-192/1 | C | | C, I | C, I | C, I | C, I | I |
| M5-256[2] | | | C | C, I | C, I | C, I | I |
| M5-256/1 | C | | C, I | C, I | C, I | C, I | I |
| M5LV-256 | C | | C, I | C, I | C, I | I | |
| M5-320 | | C | C, I | C, I | C, I | C, I | I |
| M5LV-320 | | C | C, I | C, I | C, I | C, I | I |
| M5-384 | | C | C, I | C, I | C, I | C, I | I |
| M5LV-384 | | C | C, I | C, I | C, I | C, I | I |
| M5-512 | | C | C, I | C, I | C, I | C, I | I |
| M5LV-512 | | C | C, I | C, I | C, I | C, I | I |

***Note:***

1. *C = Commercial grade, I = Industrial grade*
2. */1 version recommended for new designs*

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL® block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

**Table 3. MACH 5 Package and I/O Options [1]**

| | M5-128/1 M5LV-128 | | M5-192/1 | M5-256/1 M5LV-256 | | M5-320 M5LV-320 | | M5-384 M5LV-384 | | M5-512 M5LV-512 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Supply Voltage** | **5** | **3.3** | **5** | **5** | **3.3** | **5** | **3.3** | **5** | **3.3** | **5** | **3.3** |
| 100-pin TQFP | 68 | 68, 74 | 68 | 68 | 68*, 74 | | | | | | |
| 100-pin PQFP | 68 | 68* | 68* | 68* | 68 | | | | | | |
| 144-pin TQFP | | 104 | | | 104 | | | | | | |
| 144-pin PQFP | 104 | 104* | 104* | 104* | 104* | | | | | | |
| 160-pin PQFP | 120 | 120 | 120 | 120 | 120 | 120* | 120 | 120* | 120 | 120* | 120 |
| 208-pin PQFP | | | | 160 | 160 | 160 | 160 | 160 | 160 | 160 | 160 |
| 240-pin PQFP | | | | | | 184* | 184* | 184* | 184* | 184* | 184* |
| 256-ball BGA | | | | | | 192 | 192* | 192* | 192* | 192* | 192* |
| 352-ball BGA | | | | | | | | | | 256 | 256 |

***Note:***

1. *The I/O options indicated with a "*" are obsolete, please contact factory for more information.*

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design,

Select devices have been discontinued.
See Ordering Information section for product status.

and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

## FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.

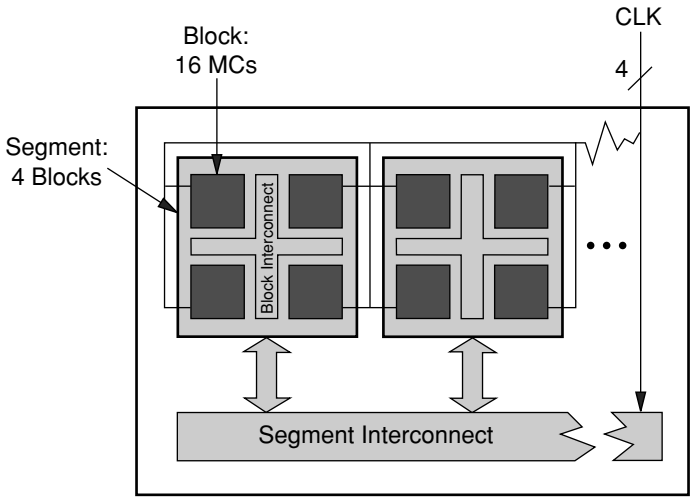


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**Figure 1. MACH 5 Block Diagram**

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- I/O cells
- Product-term array and Logic Allocator
- Macrocells
- Register control generator
- Output enable generator

### I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

Select devices have been discontinued.
See Ordering Information section for product status.

## Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The
I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as "buried" macrocells to drive device logic via the matrix.

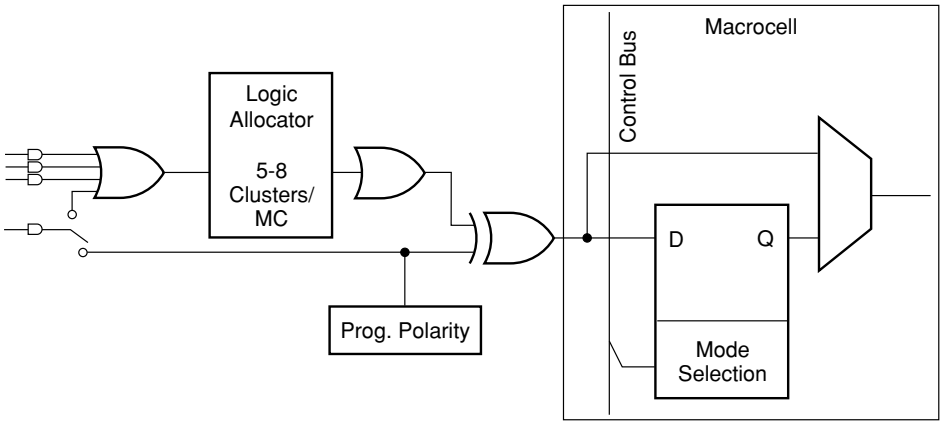


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**Figure 3. Macrocell Diagram**

## Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

**Clock Line 0 Options**

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

**Clock Line 1 Options**

- Global clock (0, 1, 2, or 3) with positive edge clock enable
- Global clock (0, 1, 2, or 3) with negative edge clock enable

Select devices have been discontinued.
See Ordering Information section for product status.

## OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

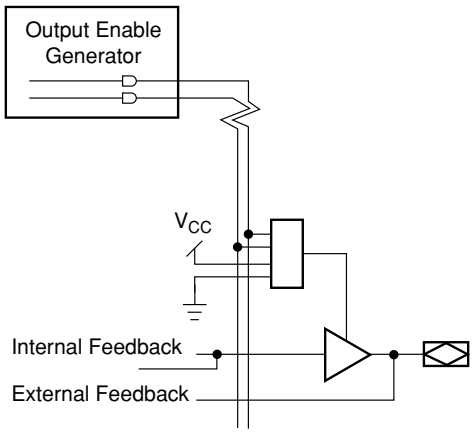


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**Figure 6. Output Enable Generator and I/O Cell**

Select devices have been discontinued.
See Ordering Information section for product status.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS [1]

Both the 3.3-V and 5-V $V_{CC}$ MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

***Note:***

1. *Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".*

## BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

**Table 5. Power Levels**

| | |
|---|---|
| High Speed/High Power | 100% Power |
| Medium High Speed/Medium High Power | 67% Power |
| Medium Low Speed/Medium Low Power | 40% Power |
| Low Speed/Low Power | 20% Power |

## PROGRAMMABLE SLEW RATE

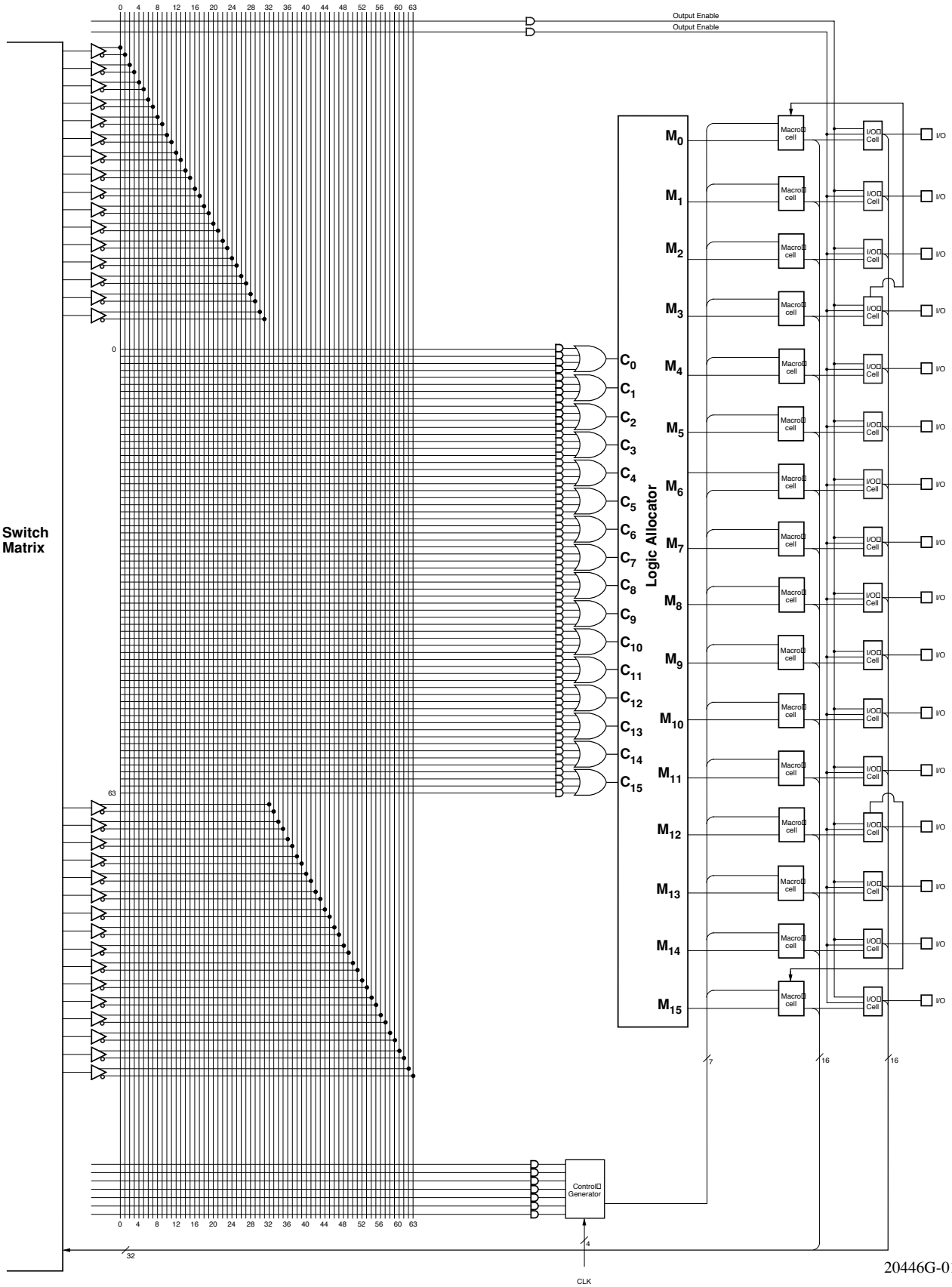
Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the $V_{CC}$ rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

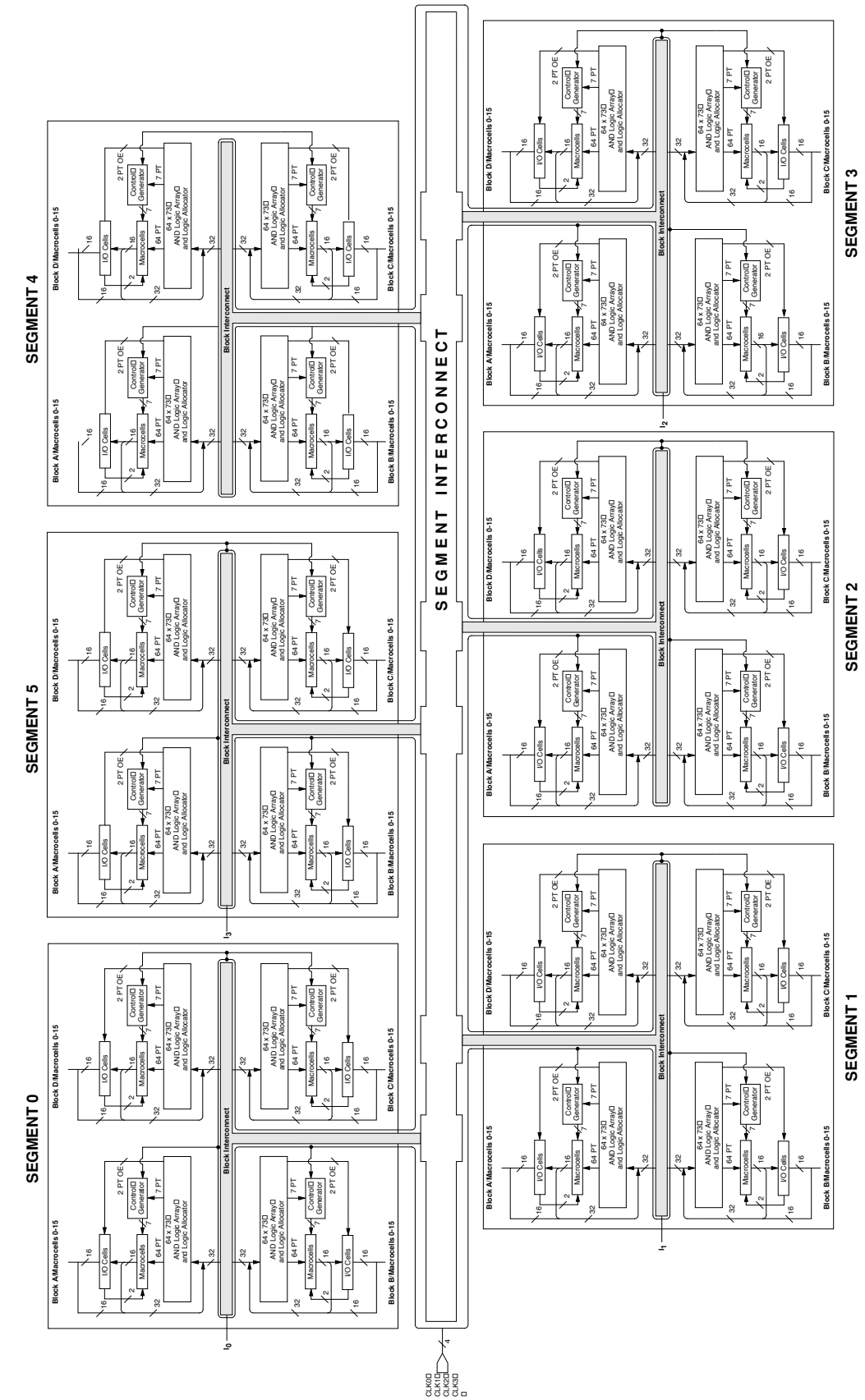
Select devices have been discontinued.
See Ordering Information section for product status.

# MACH 5 PAL BLOCK




**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# BLOCK DIAGRAM — M5(LV)-384/XXX

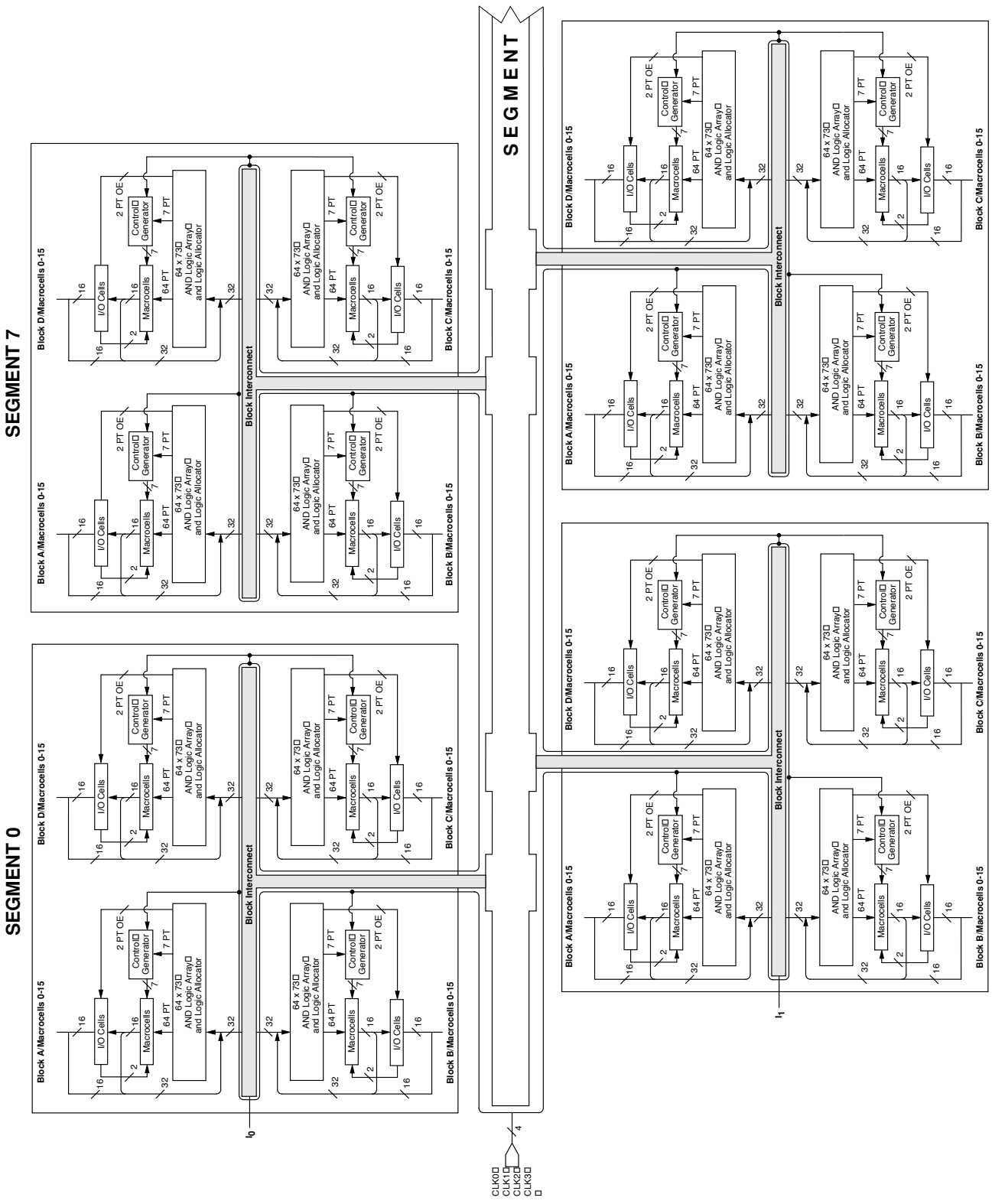



20446G-011

**Select devices have been discontinued.**
**See Ordering Information section for product status.**

# BLOCK DIAGRAM — M5(LV)-512/XXX

Continued




Select devices have been discontinued.
See Ordering Information section for product status.

20446G-012

## M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1]

| | | -5 | | -6 | | -7 | | -10 | | -12 | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Combinatorial Delay:** | | | | | | | | | | | | | | | | |
| $t_{PDi}$ | Internal combinatorial propagation delay | | 3.5 | | 4.5 | | 5.5 | | 8.0 | | 10.0 | | 13.0 | | 18.0 | ns |
| $t_{PD}$ | Combinatorial propagation delay | | 5.5 | | 6.5 | | 7.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |
| **Registered Delays:** | | | | | | | | | | | | | | | | |
| $t_{SS}$ | Synchronous clock setup time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 8.0 | | 10.0 | | ns |
| $t_{SA}$ | Asynchronous clock setup time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{HS}$ | Synchronous clock hold time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HA}$ | Asynchronous clock hold time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{COSi}$ | Synchronous clock to internal output | | 2.5 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 8.0 | | 10.0 | ns |
| $t_{COS}$ | Synchronous clock to output | | 4.5 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | 10.0 | | 12.0 | ns |
| $t_{COAi}$ | Asynchronous clock to internal output | | 6.0 | | 6.0 | | 8.0 | | 10.0 | | 13.0 | | 15.0 | | 18.0 | ns |
| $t_{COA}$ | Asynchronous clock to output | | 8.0 | | 8.0 | | 10.0 | | 12.0 | | 15.0 | | 17.0 | | 20.0 | ns |
| **Latched Delays:** | | | | | | | | | | | | | | | | |
| $t_{SAL}$ | Latch setup time | 3.0 | | 4.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{HAL}$ | Latch hold time | 3.0 | | 3.0 | | 4.0 | | 5.0 | | 6.0 | | 7.0 | | 8.0 | | ns |
| $t_{PDLi}$ | Transparent latch internal | | 6.0 | | 7.0 | | 7.0 | | 8.0 | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{PDL}$ | Propagation delay through transparent latch | | 8.0 | | 9.0 | | 9.0 | | 10.0 | | 11.0 | | 12.0 | | 12.0 | ns |
| $t_{GOAi}$ | Gate to internal output | | 7.0 | | 8.0 | | 8.0 | | 9.0 | | 10.0 | | 11.0 | | 12.0 | ns |
| $t_{GOA}$ | Gate to output | | 9.0 | | 10.0 | | 10.0 | | 11.0 | | 12.0 | | 13.0 | | 14.0 | ns |
| **Input Register Delays:** | | | | | | | | | | | | | | | | |
| $t_{SIRS}$ | Input register setup time using a synchronous clock | 2.0 | | 2.0 | | 2.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{SIRA}$ | Input register setup time using an asynchronous clock | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HIRS}$ | Input register hold time using a synchronous clock | 3.0 | | 3.0 | | 3.0 | | 4.0 | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{HIRA}$ | Input register hold time using an asynchronous clock | 6.0 | | 6.0 | | 6.0 | | 7.0 | | 7.0 | | 7.0 | | 7.0 | | ns |
| **Input Latch Delays:** | | | | | | | | | | | | | | | | |
| $t_{SIL}$ | Input latch setup time | 2.0 | | 2.0 | | 2.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{HIL}$ | Input latch hold time | 6.0 | | 6.0 | | 6.0 | | 7.0 | | 7.0 | | 7.0 | | 7.0 | | ns |
| $t_{PDILi}$ | Transparent input latch | | 5.0 | | 5.0 | | 5.5 | | 6.0 | | 6.0 | | 6.0 | | 6.0 | ns |
| **Output Delays:** | | | | | | | | | | | | | | | | |
| $t_{BUF}$ | Output buffer delay | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | ns |
| $t_{SLW}$ | Slow slew rate delay | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | ns |
| $t_{EA}$ | Output enable time | | 7.5 | | 7.5 | | 9.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |
| $t_{ER}$ | Output disable time | | 7.5 | | 7.5 | | 9.5 | | 10.0 | | 12.0 | | 15.0 | | 20.0 | ns |

Select devices have been discontinued.
See Ordering Information section for product status.

## CAPACITANCE[1]

| Parameter Symbol | Parameter Description | Test conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | I/CLK pin | $V_{IN}$ =2.0 V | 3.3 V or 5 V, 25° C, 1 MHz | 12 | pF |
| $C_{I/O}$ | I/O pin | $V_{OUT}$ =2.0 V | 3.3 V or 5 V, 25° C, 1 MHz | 10 | pF |

*1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.*

## $I_{CC}$ vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

## $I_{CC}$ CURVES AT HIGH /LOW POWER MODES

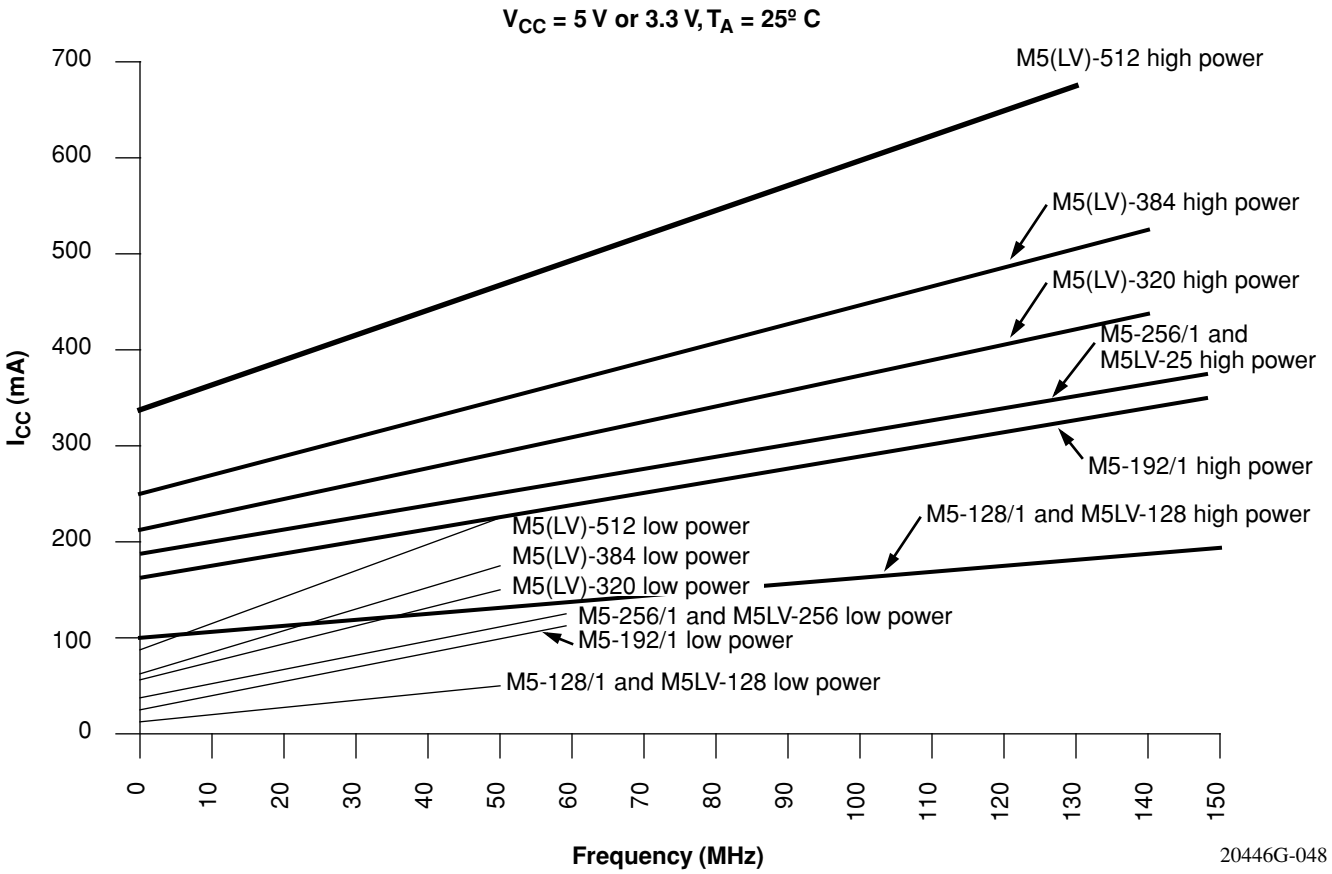



**Figure 8. $I_{CC}$ Curves at High/Low Power Modes**

Select devices have been discontinued.
See Ordering Information section for product status.

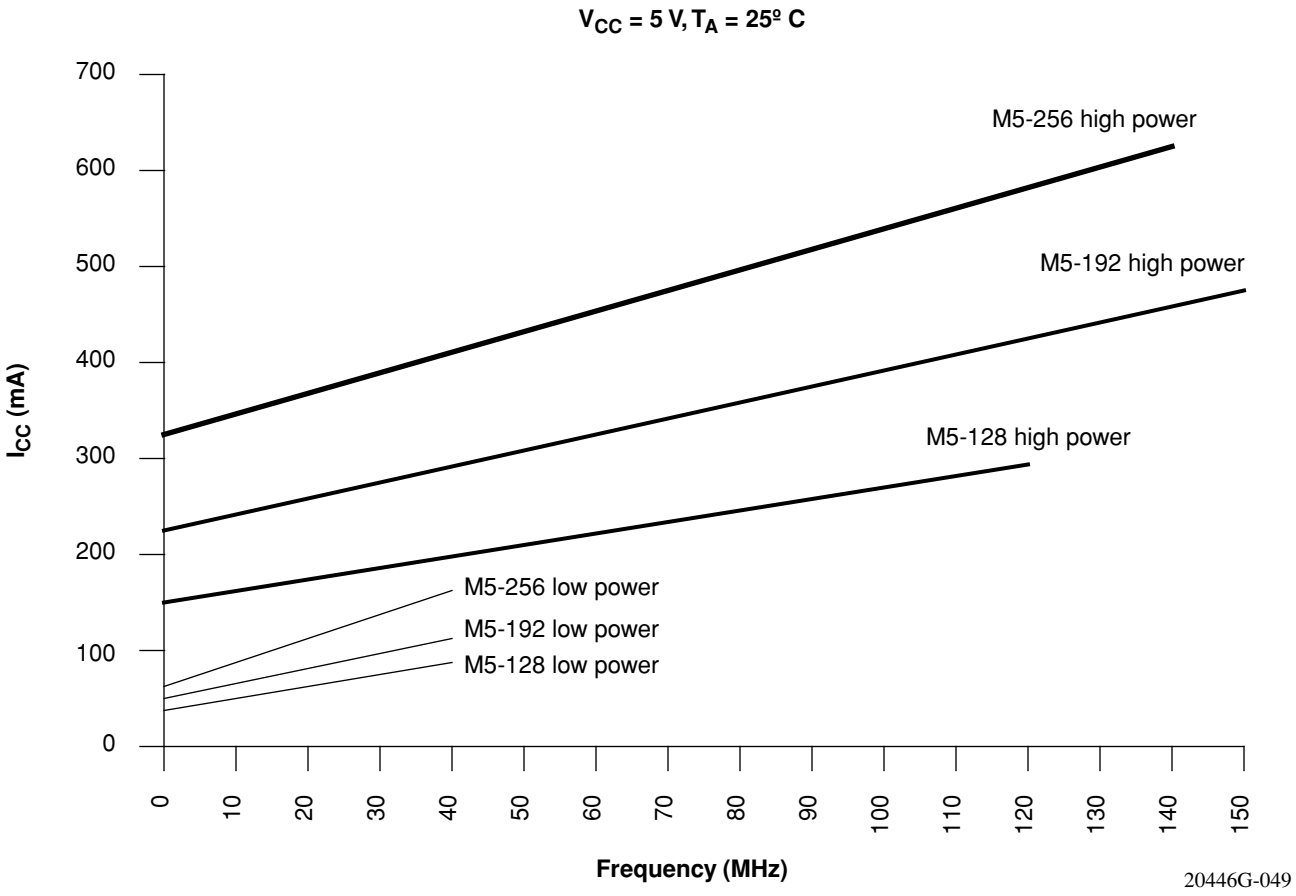


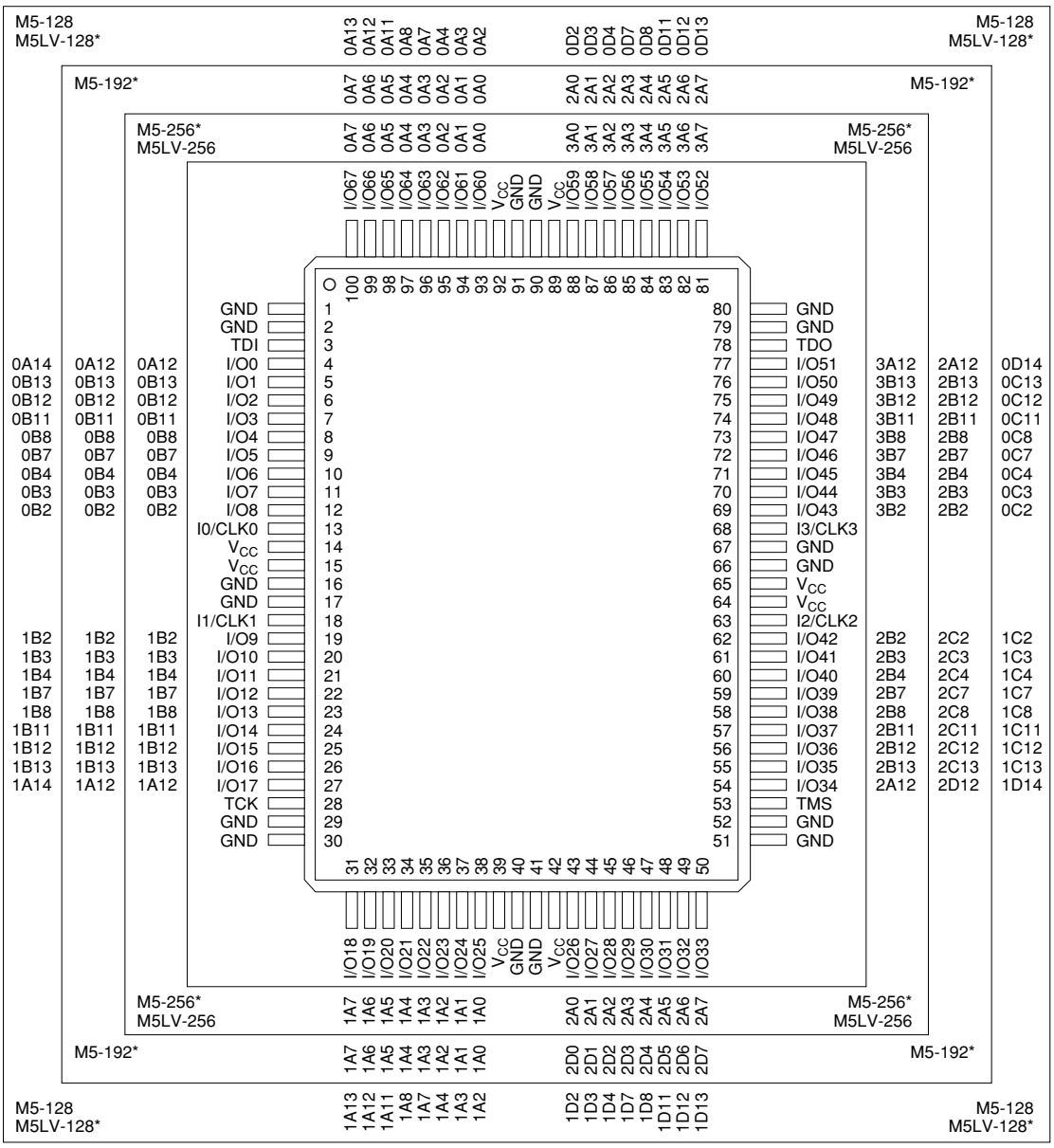

**Figure 9. $I_{CC}$ Curves at High/Low Power Modes**

Select devices have been discontinued.
See Ordering Information section for product status.

# 100-PIN PQFP CONNECTION DIAGRAM

## Top View

**100-Pin PQFP (68 I/O)**



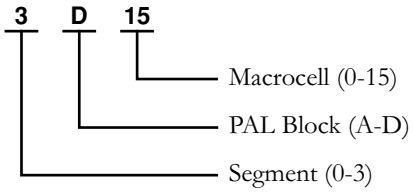

*Package obsolete, contact factory.

20446G-016

**Select devices have been discontinued. See Ordering Information section for product status.**

### Pin Designations

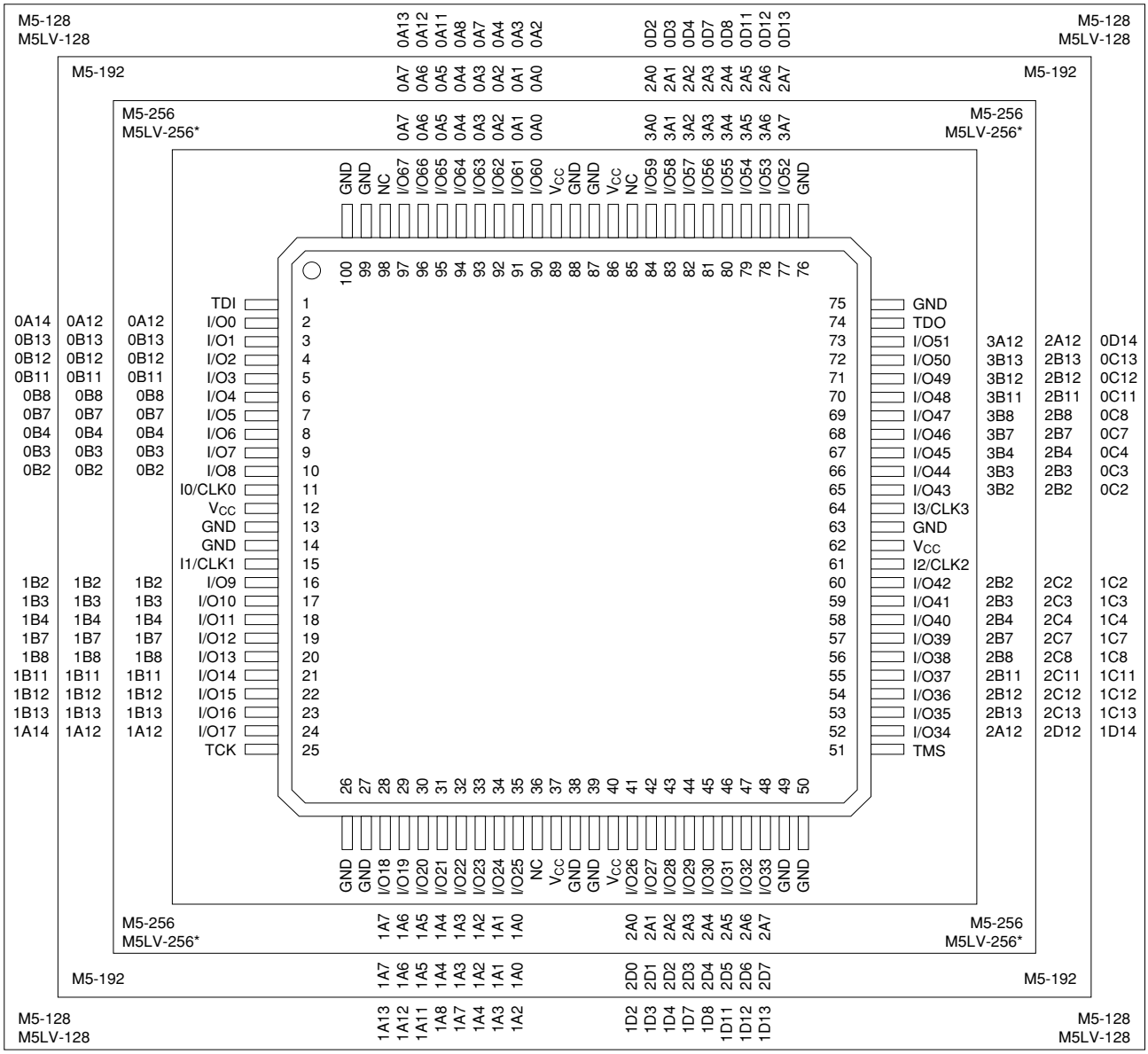
| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |



# 100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

## Top View

**100-Pin TQFP (68 I/O)**



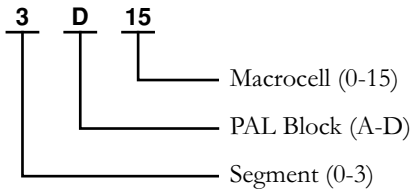

*Package obsolete, contact factory.

20446G-017

Select devices have been discontinued.
See Ordering Information section for product status.

### Pin Designations

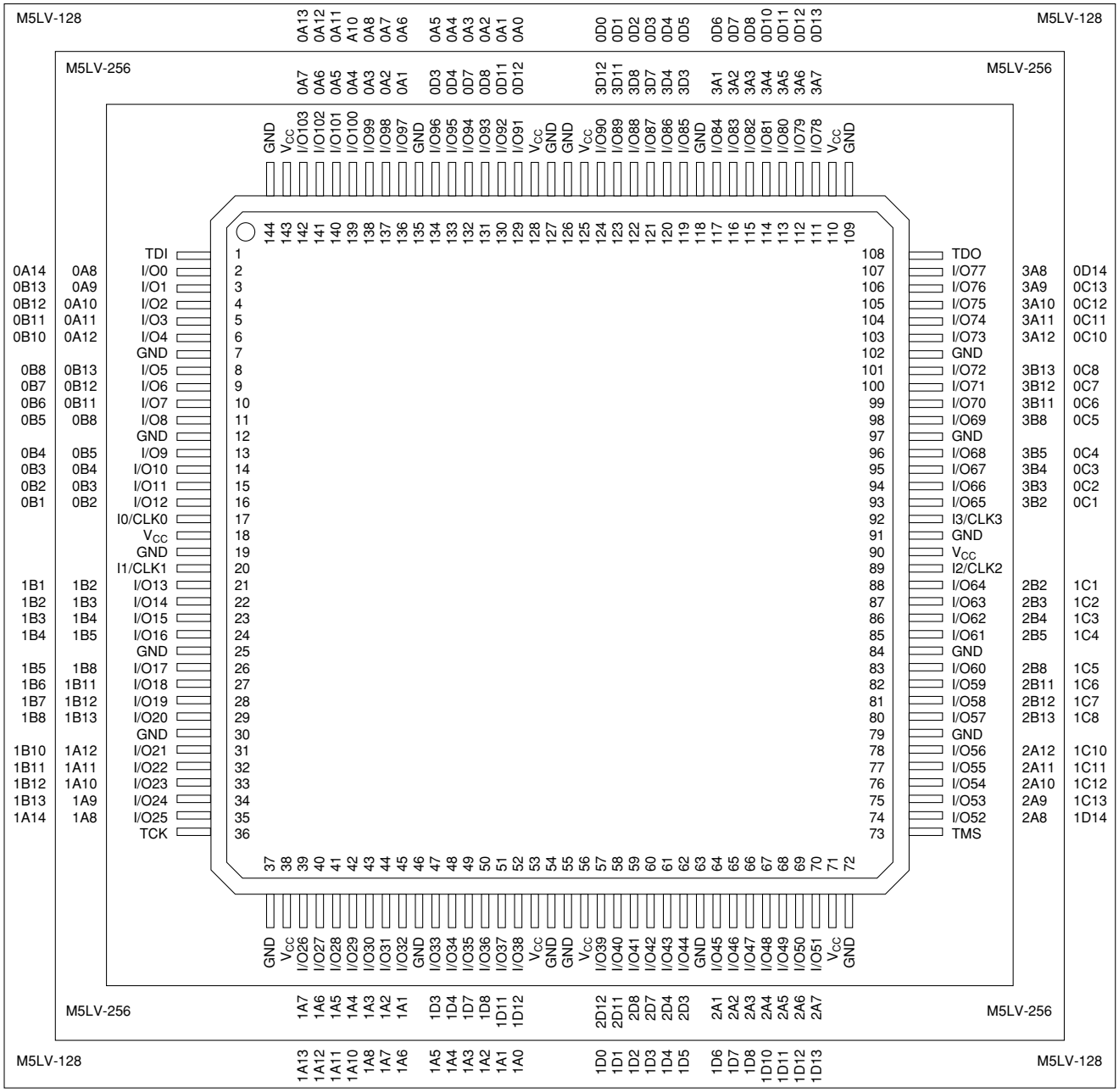
| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |



# 144-PIN TQFP CONNECTION DIAGRAM

## Top View

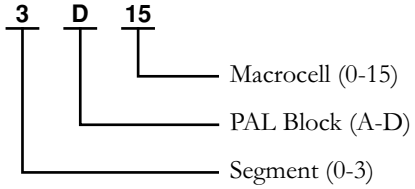
**144-Pin TQFP**




20446G-020

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |

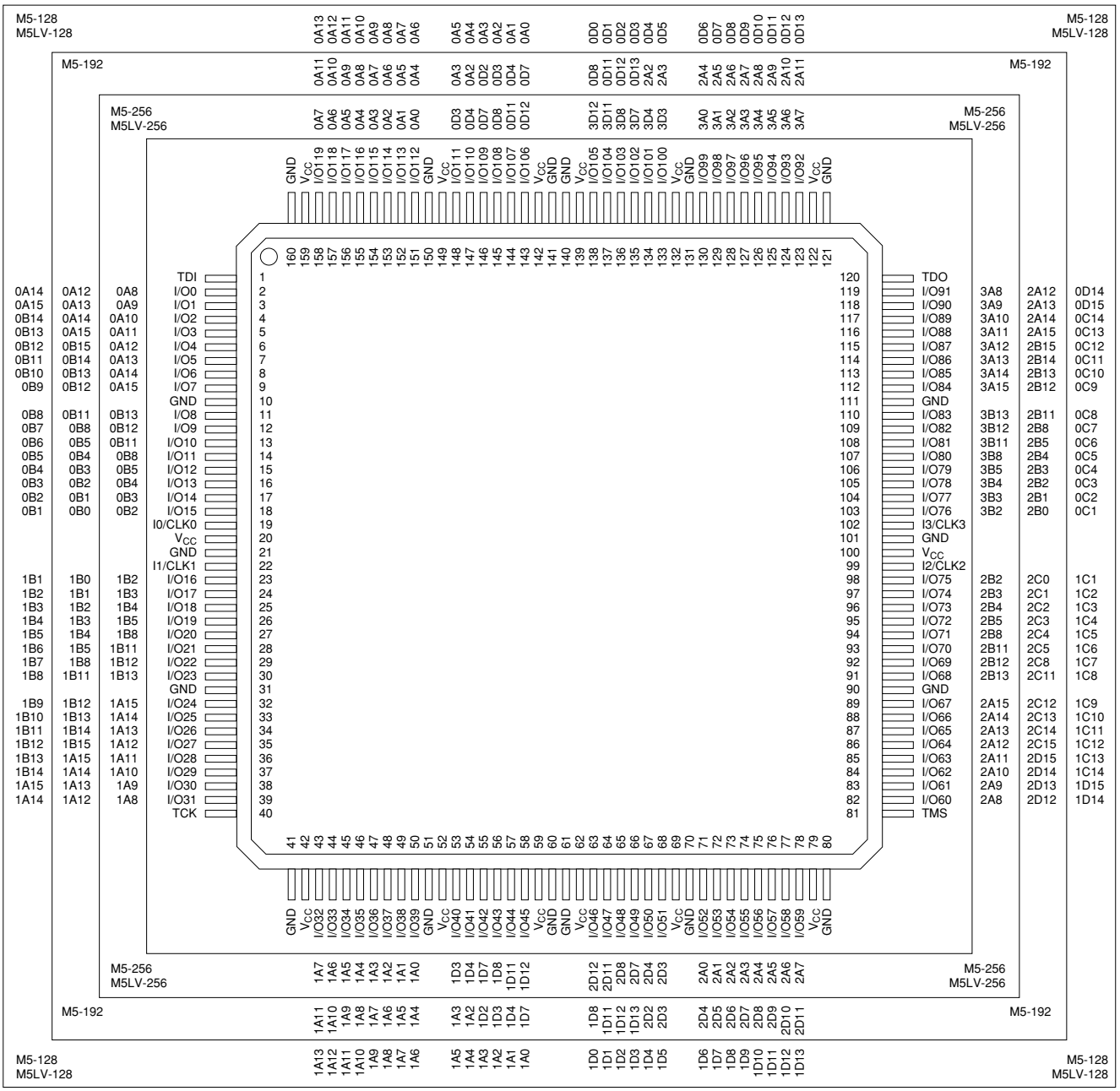



**Select devices have been discontinued. See Ordering Information section for product status.**

# 160-PIN PQFP CONNECTION DIAGRAM

## Top View

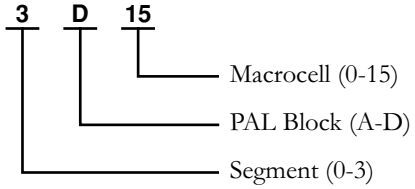
**160-Pin PQFP (128, 192, 256 Macrocells)**




20446G-021

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |

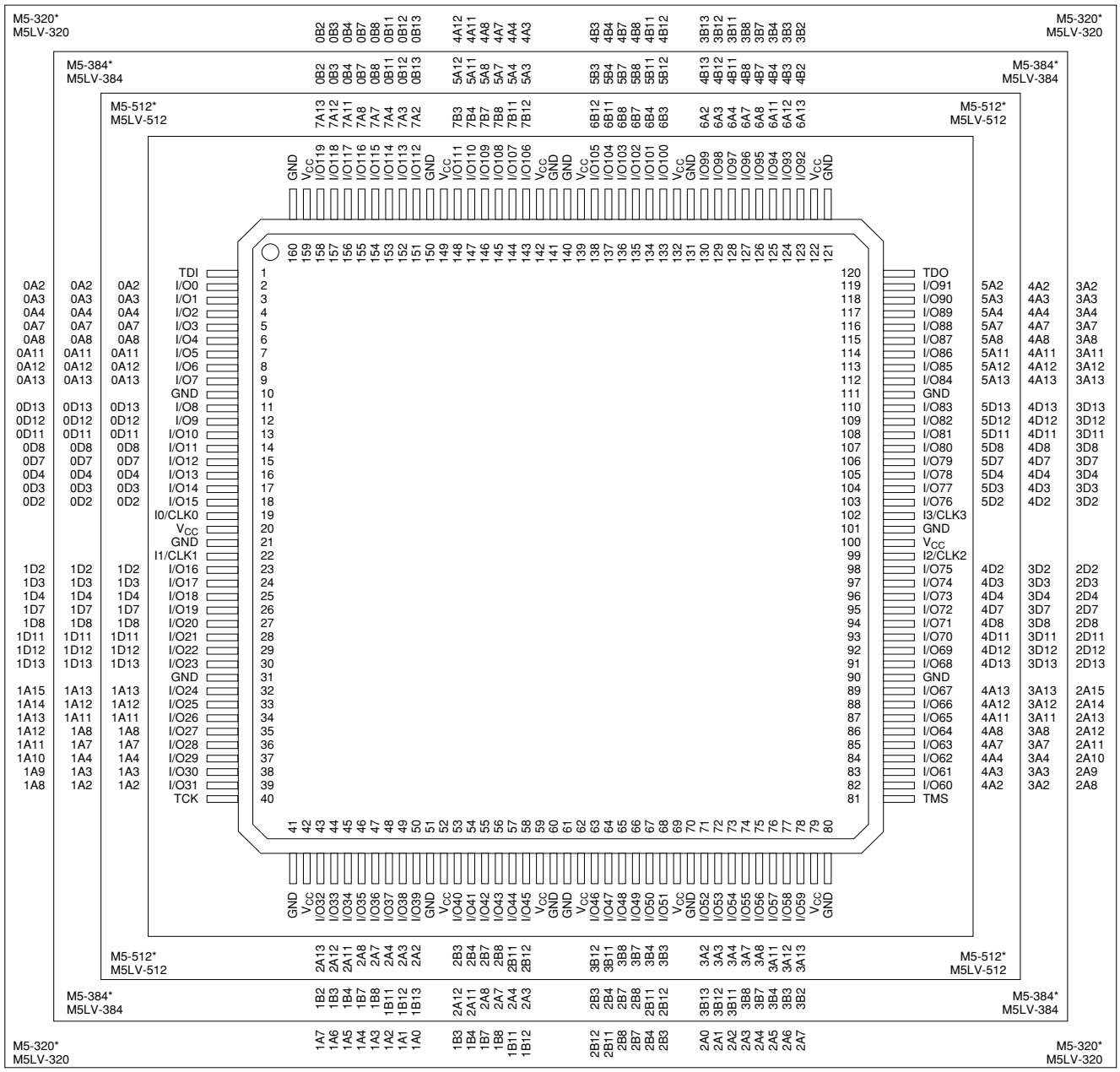



**Select devices have been discontinued. See Ordering Information section for product status.**

# 160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM

## Top View

**160-Pin PQFP (320, 384, 512 Macrocells)**



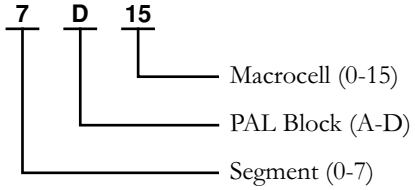

*Package obsolete, contact factory.

20446G-022

**Select devices have been discontinued. See Ordering Information section for product status.**

### Pin Designations

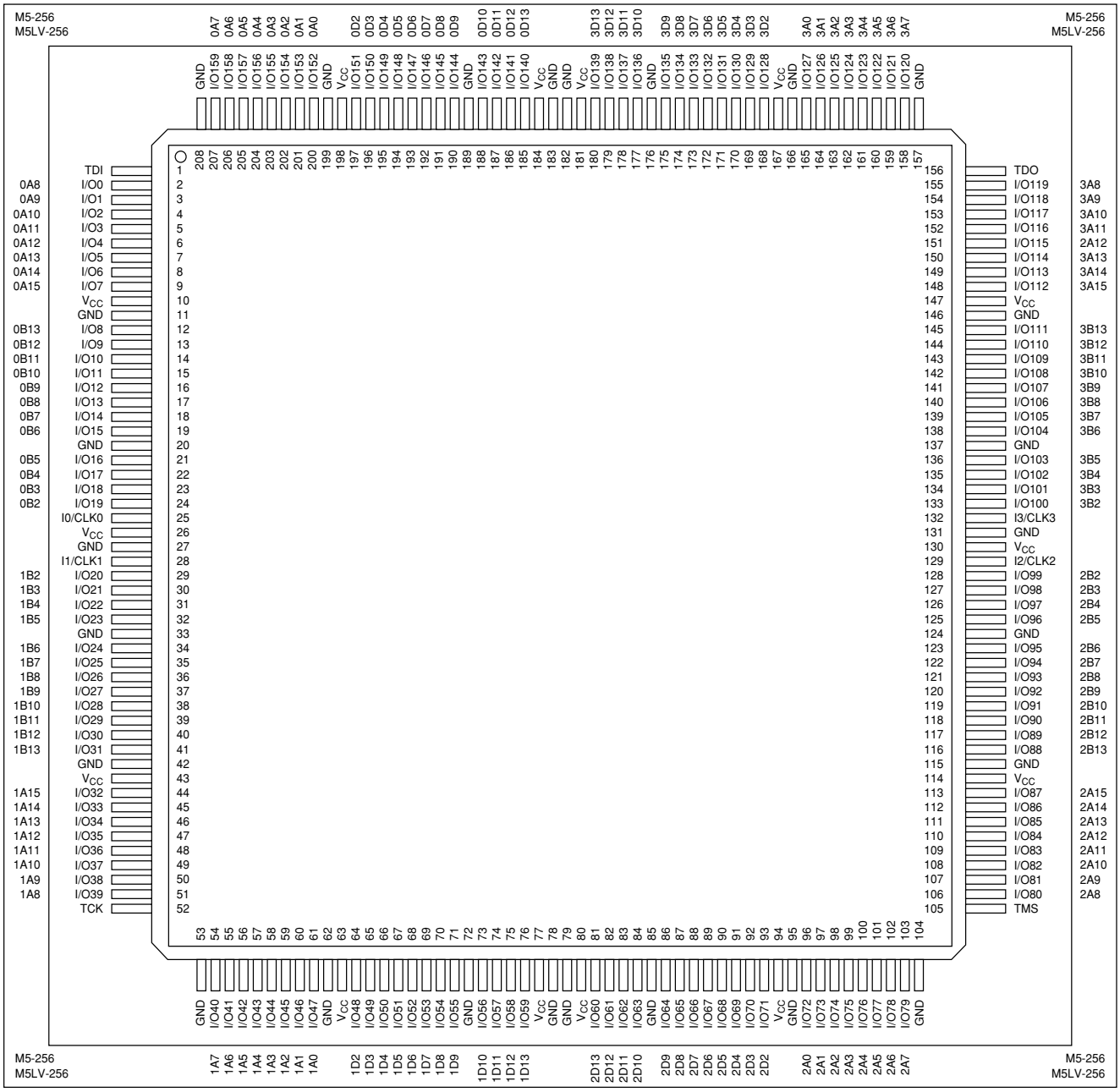
| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |



# 208-PIN PQFP CONNECTION DIAGRAM

## Top View

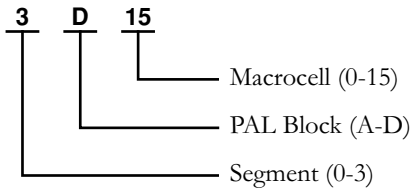
**208-Pin PQFP (256 Macrocells)**




20446G-023

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |

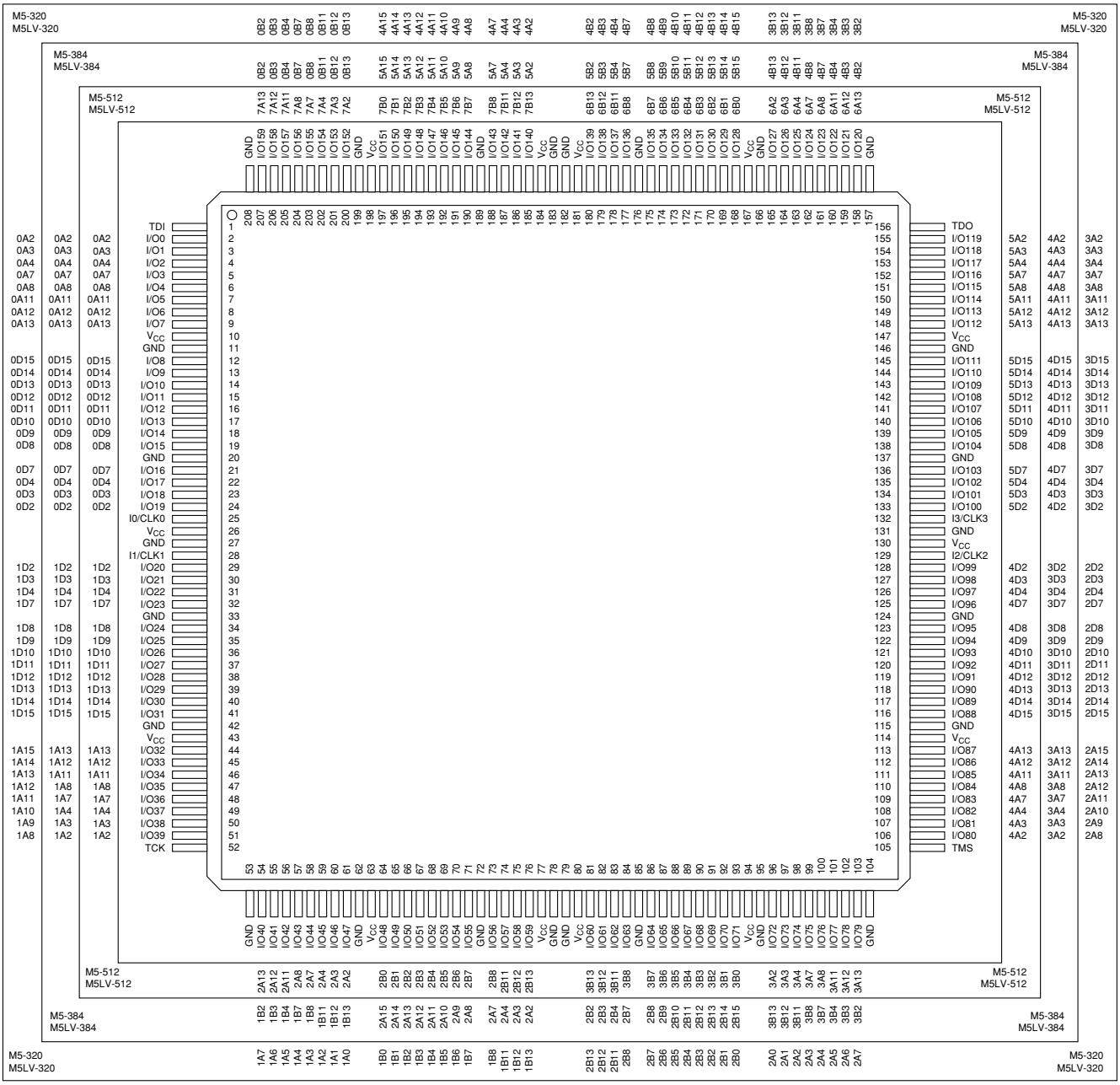



**Select devices have been discontinued. See Ordering Information section for product status.**

# 208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM

## Top View

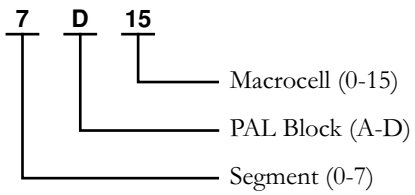
**208-Pin PQFP (320, 384, 512 Macrocells)**




20446G-024

### Pin Designations

| | | | | | |
|---|---|---|---|---|---|
| CLK | = | Clock | $V_{CC}$ | = | Supply Voltage |
| GND | = | Ground | TDI | = | Test Data In |
| I | = | Input | TCK | = | Test Clock |
| I/O | = | Input/Output | TMS | = | Test Mode Select |
| NC | = | No Connect | TDO | = | Test Data Out |




**Select devices have been discontinued. See Ordering Information section for product status.**

# 256-BALL BGA CONNECTION DIAGRAM — M5-320

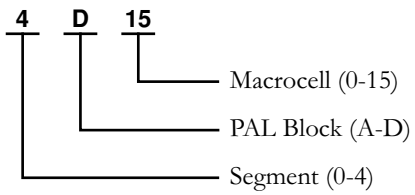
## Bottom View (Macrocell Association)

**256-Ball BGA**

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | Y | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | 3A11 | 3D15 | 3D12 | GND | 3D7 | GND | 3D3 | 3D2 | GND | 2D2 | GND | 2D7 | GND | 2D10 | 2D13 | 2D15 | GND | GND | 1 |
| 2 | GND | 3B2 | 3A3 | 3A8 | 3A13 | 3D13 | 3D9 | 3D8 | 3D4 | I3/CLK3 | I2/CLK2 | 2D3 | 2D4 | 2D8 | 2D12 | 2A15 | 2A13 | 2A12 | 2A9 | 2A7 | 2 |
| 3 | GND | 3B8 | $V_{CC}$ | 3A2 | 3A4 | 3A12 | 3D14 | 3D10 | 3D5 | 3D0 | 2D0 | 2D5 | 2D9 | 2D14 | 2A14 | 2A10 | 2A8 | $V_{CC}$ | 2A3 | GND | 3 |
| 4 | 3B13 | 3B11 | 3B3 | $V_{CC}$ | TDO | 3A7 | $V_{CC}$ | 3D11 | 3D6 | 3D1 | 2D1 | 2D6 | 2D11 | $V_{CC}$ | 2A11 | TMS | $V_{CC}$ | 2A6 | 2A2 | 2A0 | 4 |
| 5 | 4B14 | 4B15 | 3B4 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 2A5 | 2B0 | 2B1 | 5 |
| 6 | GND | 4B11 | 3B12 | 3B7 | | | | | | | | | | | | | 2A4 | 2A1 | 2B4 | GND | 6 |
| 7 | 4B8 | 4B10 | 4B13 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 2B2 | 2B5 | 2B7 | 7 |
| 8 | 4B4 | 4B6 | 4B9 | 4B12 | | | | | | | | | | | | | 2B3 | 2B6 | 2B9 | 2B11 | 8 |
| 9 | GND | 4B3 | 4B5 | 4B7 | | | | | | | | | | | | | 2B8 | 2B10 | 2B12 | GND | 9 |
| 10 | GND | 4B0 | 4B1 | 4B2 | | | | | | | | | | | | | 2B13 | 2B14 | 2B15 | GND | 10 |
| 11 | GND | 4A0 | 4A1 | 4A2 | | | | | | | | | | | | | 1B13 | 1B14 | 1B15 | GND | 11 |
| 12 | GND | 4A3 | 4A5 | 4A7 | | | | | | | | | | | | | 1B8 | 1B10 | 1B12 | GND | 12 |
| 13 | 4A4 | 4A6 | 4A9 | 4A12 | | | | | | | | | | | | | 1B3 | 1B6 | 1B9 | 1B11 | 13 |
| 14 | 4A8 | 4A10 | 4A13 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 1B2 | 1B5 | 1B7 | 14 |
| 15 | GND | 4A11 | 0B12 | 0B7 | | | | | | | | | | | | | 1A4 | 1A1 | 1B4 | GND | 15 |
| 16 | 4A14 | 4A15 | 0B4 | $V_{CC}$ | | | | | | | | | | | | | $V_{CC}$ | 1A5 | 1B0 | 1B1 | 16 |
| 17 | 0B13 | 0B11 | 0B3 | $V_{CC}$ | TDI | 0A7 | $V_{CC}$ | 0D11 | 0D6 | 0D1 | 1D1 | 1D6 | 1D11 | $V_{CC}$ | 1A11 | TCK | $V_{CC}$ | 1A6 | 1A2 | 1A0 | 17 |
| 18 | GND | 0B8 | $V_{CC}$ | 0A2 | 0A4 | 0A12 | 0D14 | 0D9 | 0D5 | 0D0 | 1D0 | 1D5 | 1D10 | 1D14 | 1A14 | 1A10 | 1A8 | $V_{CC}$ | 1A3 | GND | 18 |
| 19 | 0B2 | 0A3 | 0A8 | 0A11 | 0A13 | 0D12 | 0D8 | 0D4 | 0D3 | I0/CLK0 | I1/CLK1 | 1D4 | 1D8 | 1D9 | 1D13 | 1A15 | 1A12 | 1A9 | 1A7 | GND | 19 |
| 20 | GND | GND | 0D15 | 0D13 | 0D10 | GND | 0D7 | GND | 0D2 | GND | 1D2 | 1D3 | GND | 1D7 | GND | 1D12 | 1D15 | 1A13 | GND | GND | 20 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | Y | |

### Pin Designations

| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| NC | = | No Connect |
| $V_{CC}$ | = | Supply Voltage |
| TDI | = | Test Data In |
| TCK | = | Test Clock |
| TMS | = | Test Mode Select |
| TDO | = | Test Data Out |




20446G-029

**Select devices have been discontinued. See Ordering Information section for product status.**