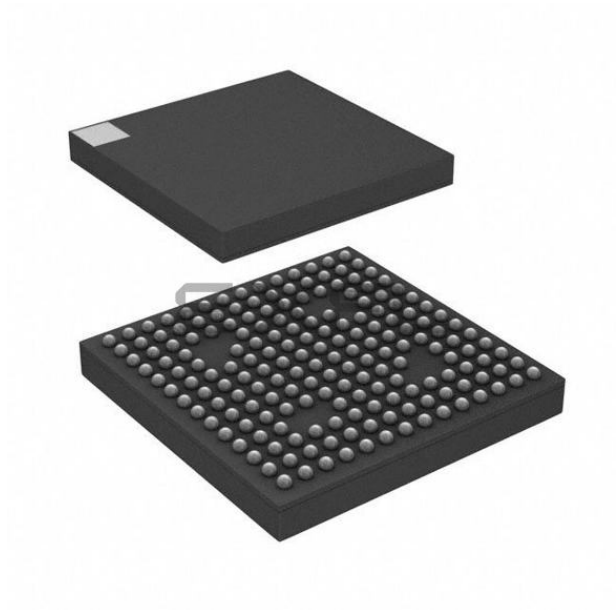

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf703wcbcz411

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ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

12 mm × 12 mm 88-LEAD LFCSP (QFN) SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 11. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
GND	Ground	Not Muxed	GND
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG\_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_10	Position 00 through Position 10	C	PC_00-PC_10
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_AFS	SPORT0 Channel A Frame Sync	A	PA_12
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_05
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	A	PA_15
SPT0_BCLK	SPORT0 Channel B Clock	B	PB_04
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_04
SPT0_BD0	SPORT0 Channel B Data 0	B	PB_05
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_06
SPT0_BD1	SPORT0 Channel B Data 1	B	PB_07
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_01
SPT0_BFS	SPORT0 Channel B Frame Sync	B	PB_06
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_07
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	A	PA_15
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_08
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_10
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_11
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_09
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	A	PA_07
SPT1_BCLK	SPORT1 Channel B Clock	B	PB_00
SPT1_BCLK	SPORT1 Channel B Clock	C	PC_10
SPT1_BD0	SPORT1 Channel B Data 0	B	PB_02
SPT1_BD1	SPORT1 Channel B Data 1	B	PB_03
SPT1_BFS	SPORT1 Channel B Frame Sync	B	PB_01
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	A	PA_07
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE
$\overline{\text{SYS\_FAULT}}$	Active-Low Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04

Table 14. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	$\overline{\text{UART1\_TX}}$	SPT0_AD1	PPI0_D15		
PC_01	$\overline{\text{UART1\_RX}}$	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	$\overline{\text{UART0\_RTS}}$	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	$\overline{\text{UART0\_CTS}}$	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	$\overline{\text{SPI1\_SEL3}}$		TM0_ACLK1

ADSP-BF70x DESIGNER QUICK REFERENCE

Table 15 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Pin Type: The Type column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (none), I/O (input/output), a (analog), s (supply), and g (ground).
- Driver Type: The Driver Type column in the table identifies the driver type used by the pin. The driver types are defined in the output drive currents section of this data sheet.
- Internal Termination: The Int Term column in the table specifies the termination present when the processor is not in the reset or hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Termination: The Reset Term column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Drive: The Reset Drive column in the table specifies the active drive on the signal when the processor is in the reset state.
- Hibernate Termination: The Hiber Term column in the table specifies the termination present when the processor is in the hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Hibernate Drive: The Hiber Drive column in the table specifies the active drive on the signal when the processor is in the hibernate state.
- Power Domain: The Power Domain column in the table specifies the power supply domain in which the signal resides.
- Description and Notes: The Description and Notes column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

If an external pull-up or pull-down resistor is required for any signal, 100 kΩ is the maximum value that can be used unless otherwise noted.

Note that for Port A, Port B, and Port C (PA_00 to PC_14), when $\overline{\text{SYS\_HWRST}}$ is low, these pads are three-state. After $\overline{\text{SYS\_HWRST}}$ is released, but before code execution begins, these pins are internally pulled up. Subsequently, the state depends on the input enable and output enable which are controlled by software.

Software control of internal pull-ups works according to the following settings in the PADS_PCFG0 register. When PADS_PCFG0 = 0: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled when both the input enable and output enable of a particular pin are deasserted. When PADS_PCFG0 = 1: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled as long as the output enable of a particular pin is deasserted.

There are some exceptions to this scheme:

- Internal pull-ups are always disabled if MSI mode is selected for that signal.
- The following signals enabled the internal pull-down when the output enable is de-asserted: $\overline{\text{SMC0\_AMS}}[1:0]$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, $\overline{\text{SMC0\_AOE}}$, SMC0_ARDY, $\overline{\text{SPI0\_SEL}}[6:1]$, $\overline{\text{SPI1\_SEL}}[4:1]$, and $\overline{\text{SPI2\_SEL}}[3:1]$.

Table 15. ADSP-BF70x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 0 Notes: No notes.
DMC0_A01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 1 Notes: No notes.
DMC0_A02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 2 Notes: No notes.
DMC0_A03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 3 Notes: No notes.
DMC0_A04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 4 Notes: No notes.
DMC0_A05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 5 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
GND_HADC	g	na	none	none	none	none	none	na	Desc: Ground HADC Notes: If HADC is not used, connect to ground.
HADC0_VIN0	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If HADC is not used, connect to ground.
HADC0_VIN1	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If HADC is not used, connect to ground.
HADC0_VIN2	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If HADC is not used, connect to ground.
HADC0_VIN3	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If HADC is not used, connect to ground.
HADC0_VREFN	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: If HADC is not used, connect to ground.
HADC0_VREFP	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: If HADC is not used, connect to ground.
JTG_TCK_ SWCLK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Clock | Serial Wire Clock Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: Functional during reset.
JTG_TDO_SWO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out | Serial Wire Out Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS_ SWDIO	I/O	A	pu	none	none	none	none	VDD_EXT	Desc: JTAG Mode Select | Serial Wire DIO Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Reset Notes: Functional during reset, a 10k external pull-down may be used to shorten the t_{VDDEXT_RST} timing requirement.
PA_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Clock | TRACE0 Trace Data 7 | SMC0 Byte Enable 0 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PA_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master In, Slave Out | TRACE0 Trace Data 6 | SMC0 Byte Enable 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Frame Sync | TM0 Timer 3 | MSI0 Command Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Data 0 | SPI0 Master In, Slave Out | MSI0 Data 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Frame Sync | SPI0 Master Out, Slave In | MSI0 Data 2 | TM0 Alternate Capture Input 2 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Data 0 | SPI0 Data 2 | MSI0 Data 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Clock | SPI0 Data 3 | MSI0 Clock | TM0 Alternate Clock 2 Notes: No notes.
PC_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Clock | MSI0 Data 4 | SPI1 Slave Select Output 3 | TM0 Alternate Clock 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Frame Sync | MSI0 Data 5 | SPI0 Slave Select Output 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 0 | MSI0 Data 6 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Internal Supply Voltage	CCLK ≤ 400 MHz	1.045	1.100	1.155	V
V_{DD_EXT}[1]	External Supply Voltage		1.7	1.8	1.9	V
V_{DD_EXT}[1]	External Supply Voltage		3.13	3.30	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.30	3.47	V
V_{DD_RTC}	Real-Time Clock Supply Voltage		2.00	3.30	3.47	V
V_{DD_HADC}	Housekeeping ADC Supply Voltage		3.13	3.30	3.47	V
V_{DD_OTP}[1]	OTP Supply Voltage					
	For Reads		2.25	3.30	3.47	V
	For Writes		3.13	3.30	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 1.9 V	0.7 × V_{DD_EXT}			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = maximum	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[7]		V_{DD_DMC} = 1.9 V	V_{DDR_REF} + 0.25			V
V_{IH_LPDDR}[8]		V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 1.075 V	0.50			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 0.725 V	0.55			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 1.7 V			0.3 × V_{DD_EXT}	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7]		V_{DD_DMC} = 1.7 V			V_{DDR_REF} – 0.25	V
V_{IL_LPDDR}[8]		V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0°C to +70°C	0		105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] If not used, connect to 1.8 V or 3.3 V.
[3] V_{HADC_VREF} should always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional signals except RTC signals, TWI signals, DMC0 signals, and USB0 signals.
[5] Parameter applies to TWI signals.
[6] TWI signals are pulled up to V_{BUSTWI}. See Table 16.
[7] Parameter applies to DMC0 signals in DDR2 mode.
[8] Parameter applies to DMC0 signals in LPDDR mode.
[9] Parameter applies to signals DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$ when used in DDR2 differential input mode.

Table 18. Peripheral Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{OCLK}	Output Clock Frequency				50	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[1, 2]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				50	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				50	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{MSICLKPROG}$	Programmed MSI Clock				50	MHz

[1] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this typical specification for each end application.
[2] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[3] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications section for that peripheral. Pay particular attention to setup and hold times for VDD_EXT = 1.8 V which may preclude the maximum frequency listed here.
[4] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} that clocks the peripheral.

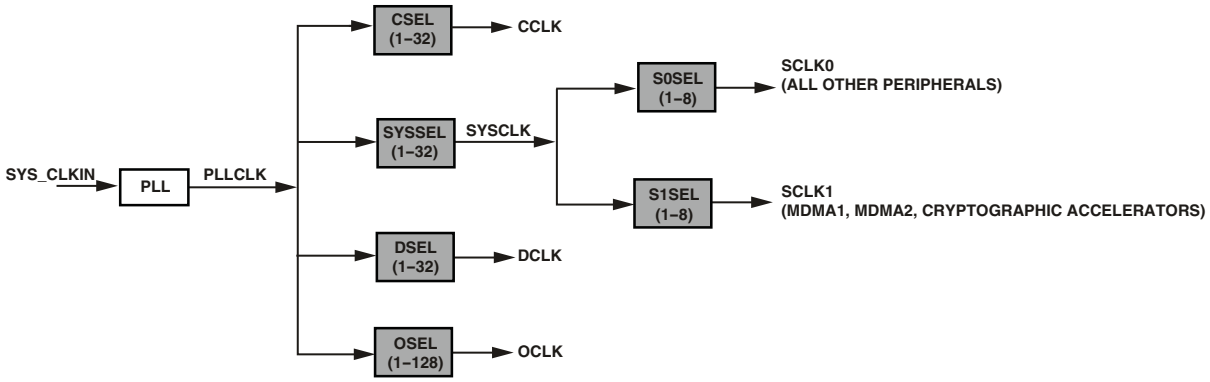

Figure 6. Clock Relationships and Divider Values

Table 19. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	230.2	800	MHz
CGU_CTL.MSEL[1]	PLL Multiplier	8	41	

[1] The CGU_CTL.MSEL setting must also be chosen to ensure that the f_{PLLCLK} specification is not violated.

PACKAGE INFORMATION

The information presented in Figure 7 and Table 27 provides details about package branding. For a complete listing of product availability, see the Ordering Guide.

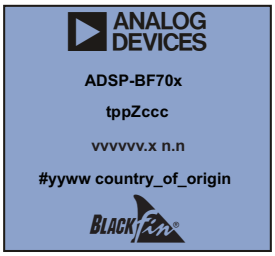

Figure 7. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 27. Package Brand Information

Brand Key	Field Description
ADSP-BF70x	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See Ordering Guide
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 28 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 28. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to +1.20 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
Real-Time Clock Supply Voltage (V_{DD_RTC})	–0.33 V to +3.60 V
Housekeeping ADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
One-Time Programmable Memory Supply Voltage (V_{DD_OTP})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V

Table 28. Absolute Maximum Ratings (Continued)

Parameter	Rating
DDR2 Reference Voltage (V_{DDR_REF})	–0.33 V to +1.90 V
Input Voltage[1, 2]	–0.33 V to +3.60 V
TWI Input Voltage[2, 3]	–0.33 V to +5.50 V
USB0_Dx Input Voltage[4]	–0.33 V to +5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to +6 V
DDR2 Input Voltage[5]	–0.33 V to +1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	4 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] Applies to balls TWI_SCL and TWI_SDA.
[4] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 38.
[5] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Up/Down Counter/Rotary Encoder Timing

Table 47 and Figure 25 describe timing, related to the general-purpose counter (CNT).

Table 47. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

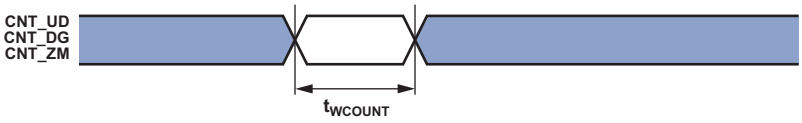

Figure 25. Up/Down Counter/Rotary Encoder Timing

Table 51. Serial Ports—Enable and Three-State

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		14		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1.12		–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8		2.8	ns

[1] Referenced to drive edge.

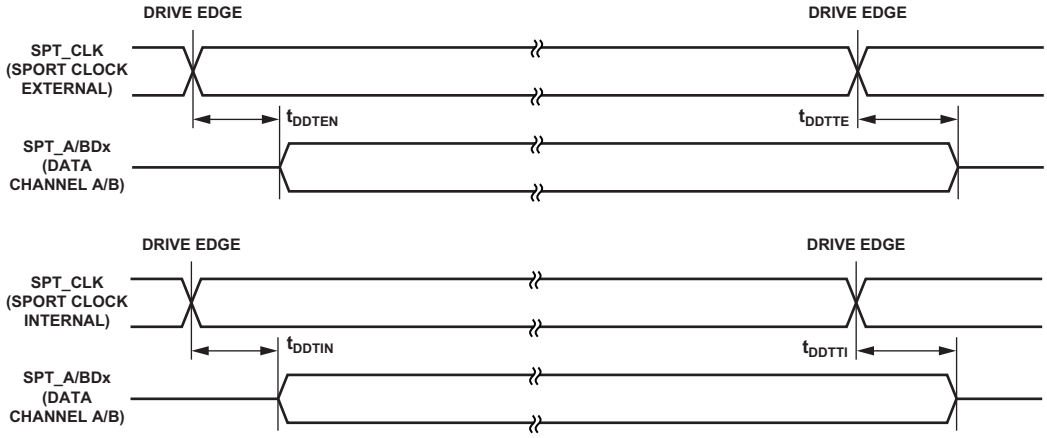

Figure 28. Serial Ports—Enable and Three-State

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

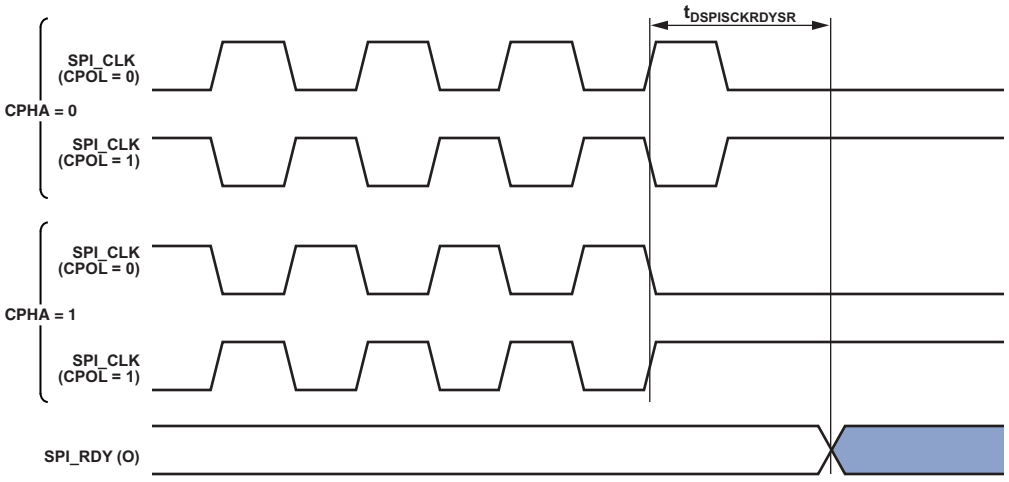

Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

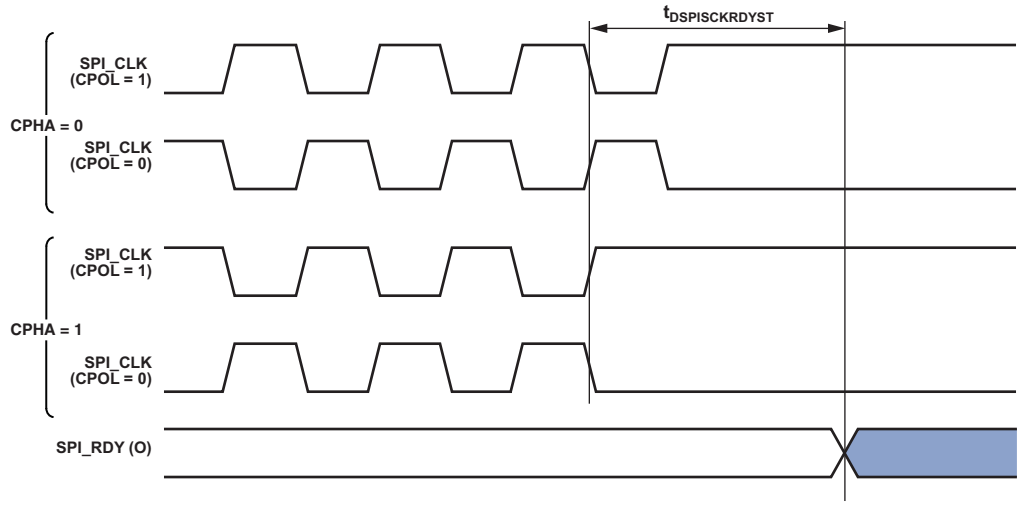

Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

Enhanced Parallel Peripheral Interface Timing

The following tables and figures describe enhanced parallel peripheral interface timing operations. The POLC bits in the EPPI_CTL register may be used to set the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65,535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 60. Enhanced Parallel Peripheral Interface—Internal Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	1.5		1		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.4		5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	1		1		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	16.5		14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	1.5		0		ns
Switching Characteristics						
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 2$		$0.5 \times t_{PCLKPROG} - 2$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 2$		$t_{PCLKPROG} - 2$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		2		2	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–4		–3		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		2		2	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–4		–3		ns

[1] See Table 18 on Page 52 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{PCLKPROG}$.

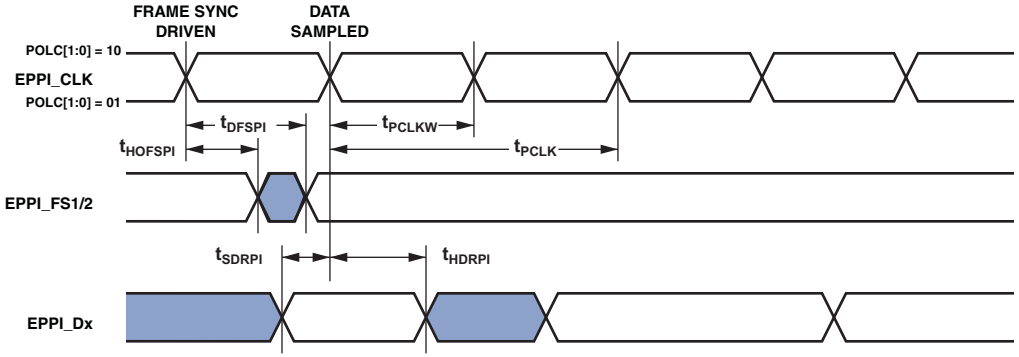

Figure 40. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

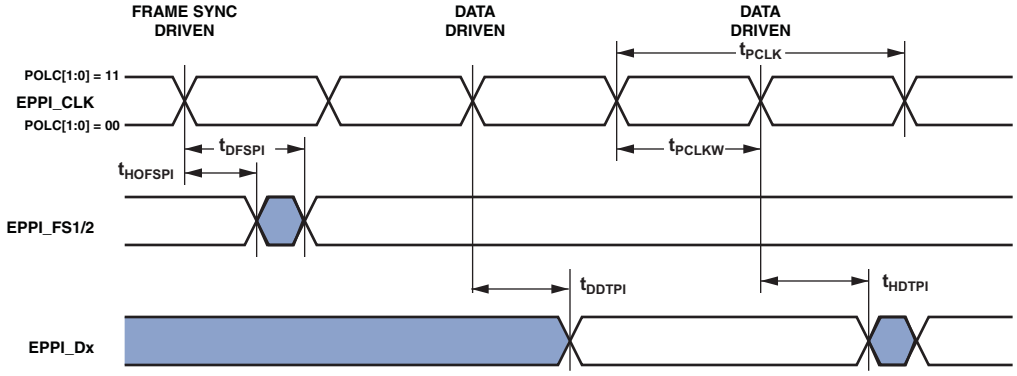

Figure 41. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

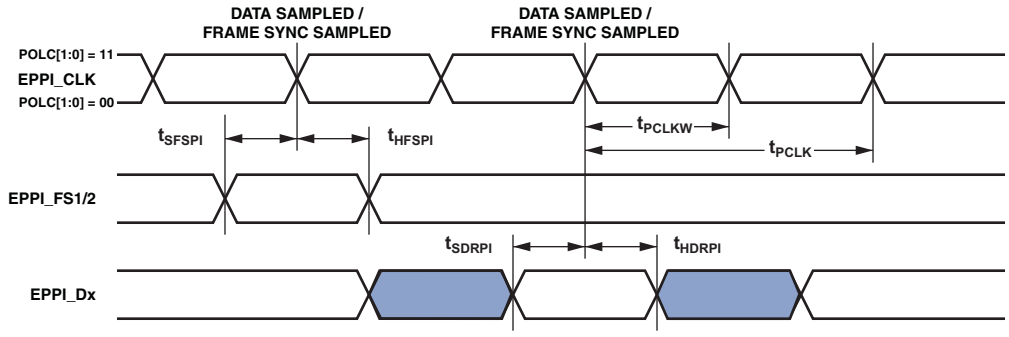

Figure 42. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The universal asynchronous receiver-transmitter (UART) ports receive and transmit operations are described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Controller Area Network (CAN) Interface

The controller area network (CAN) interface timing is described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 62 describes the universal serial bus (USB) on-the-go receive and transmit operations.

Table 62. USB On-The-Go—Receive and Transmit Timing

		V_{DD_USB} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{USBS}	USB_XI Frequency	24	24	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

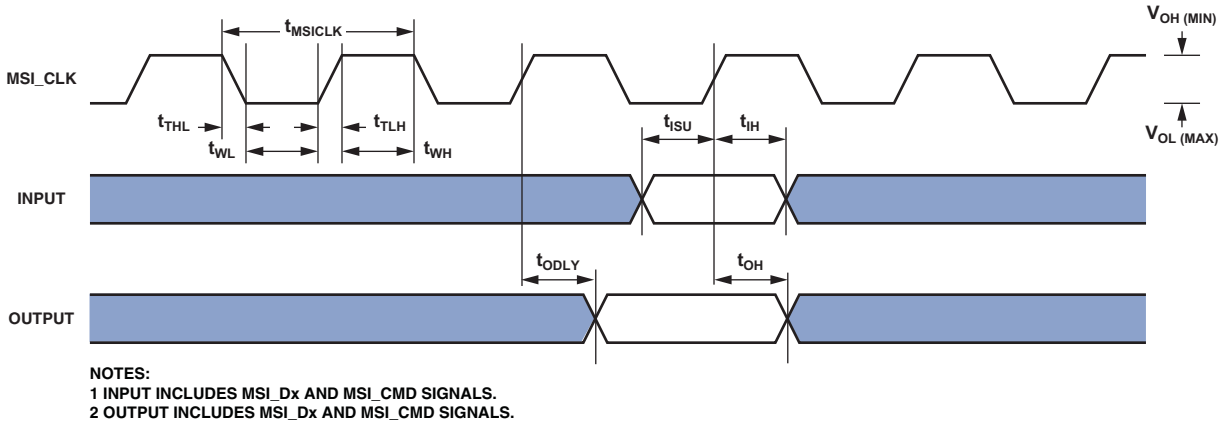

Figure 49. MSI Controller Timing

Dimensions for the 12 mm × 12 mm LFCSP_VQ package in Figure 72 are shown in millimeters.

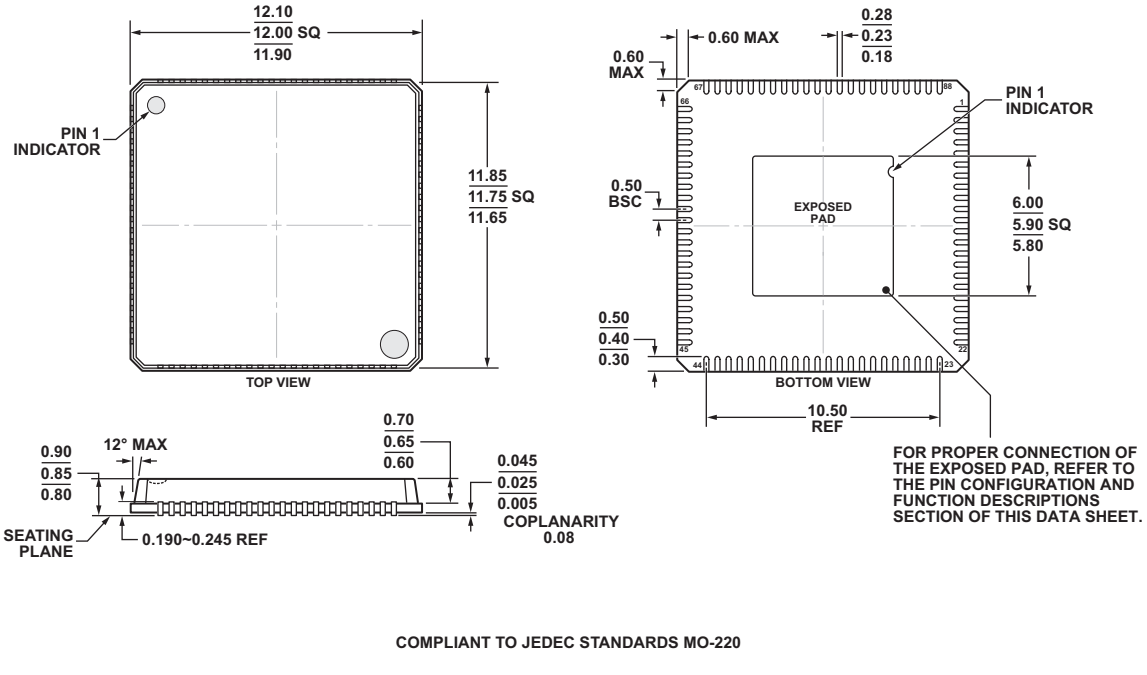

Figure 72. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
(CP-88-8)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 71 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 71. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-184-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter

PLANNED AUTOMOTIVE PRODUCTION PRODUCTS

Model [1, 2, 3]	Max. Core Clock	L2 SRAM	Temperature Grade[4]	Package Description	Package Option
ADBF702WCCPZ3xx	300 MHz	256K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF702WCCPZ4xx	400 MHz	256K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF703WCBCZ3xx	300 MHz	256K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1
ADBF703WCBCZ4xx	400 MHz	256K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1
ADBF704WCCPZ3xx	300 MHz	512K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF704WCCPZ4xx	400 MHz	512K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF705WCBCZ3xx	300 MHz	512K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1
ADBF705WCBCZ4xx	400 MHz	512K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1
ADBF706WCCPZ3xx	300 MHz	1024K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF706WCCPZ4xx	400 MHz	1024K bytes	–40°C to +105°C	88-Lead LFCSP_VQ	CP-88-8
ADBF707WCBCZ3xx	300 MHz	1024K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1
ADBF707WCBCZ4xx	400 MHz	1024K bytes	–40°C to +105°C	184-Ball CSP_BGA	BC-184-1

[1] Select Automotive grade products, supporting –40°C to +105°C $T_{AMBIENT}$ condition, will be available when they appear in the Automotive Products table.
[2] Z = RoHS Compliant Part.
[3] xx denotes the current die revision.
[4] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 50 for the junction temperature (T_J) specification which is the only temperature specification.