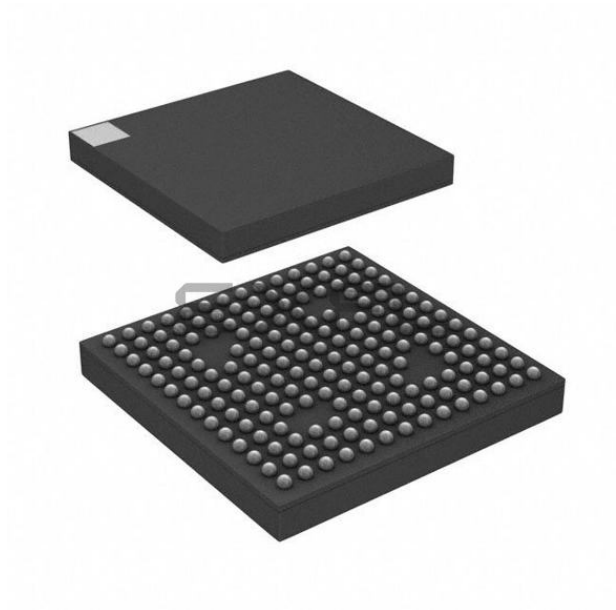

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	512kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf705wcbcz411

output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

MEMORY ARCHITECTURE

The processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency core-accessible memory as cache or SRAM, and larger, lower-cost and performance interface-accessible memory systems. See Figure 3.

Internal (Core-Accessible) Memory

The L1 memory system is the highest-performance memory available to the Blackfin+ processor core.

The core has its own private L1 memory. The modified Harvard architecture supports two concurrent 32-bit data accesses along with an instruction fetch at full processor speed which provides high-bandwidth processor performance. In the core, a 64K byte block of data memory partners with an 64K byte memory block for instruction storage. Each data block is multibanked for efficient data exchange through DMA and can be configured as SRAM. Alternatively, 16K bytes of each block can be configured in L1 cache mode. The four-way set-associative instruction cache and the 2 two-way set-associative data caches greatly accelerate memory access performance, especially when accessing external memories.

The L1 memory domain also features a 8K byte data SRAM block which is ideal for storing local variables and the software stack. All L1 memory is protected by a multi-parity-bit concept, regardless of whether the memory is operating in SRAM or cache mode.

Outside of the L1 domain, L2 and L3 memories are arranged using a Von Neumann topology. The L2 memory domain is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The L2 memory domain is accessible by the Blackfin+ core through a dedicated 64-bit interface. It operates at SYSCLK frequency.

The processor features up to 1M byte of L2 SRAM, which is ECC-protected and organized in eight banks. Individual banks can be made private to any system master. There is also a 512K byte single-bank ROM in the L2 domain. It contains boot code, security code, and general-purpose ROM space.

OTP Memory

The processor features 4 kB of one-time-programmable (OTP) memory which is memory-map accessible. This memory stores a unique chip identification and is used to support secure-boot and secure operation.

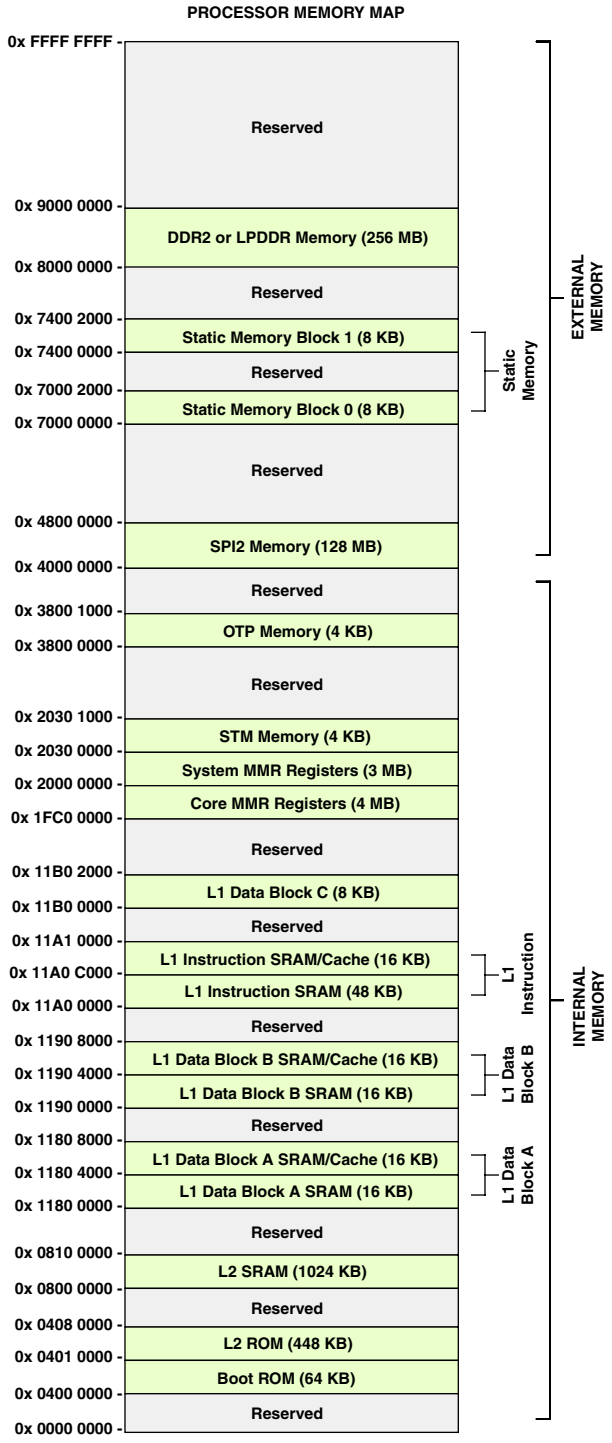

Figure 3. ADSP-BF706/ADSP-BF707 Internal/External Memory Map

184-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_BA0	DMC0 Bank Address Input 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address Input 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address Input 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
$\overline{\text{DMC0\_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_FAULT	Active-Low Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Nonmaskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
UART0_CTS	UART0 Clear to Send	C	PC_03
UART0_RTS	UART0 Request to Send	C	PC_02

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input/external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	A	PA_13
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	C	PC_03
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	C	PC_02
$\overline{\text{UART0\_RX}}$	UART0 Receive	B	PB_09
$\overline{\text{UART0\_TX}}$	UART0 Transmit	B	PB_08
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	B	PB_14
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	B	PB_13
$\overline{\text{UART1\_RX}}$	UART1 Receive	C	PC_01
$\overline{\text{UART1\_TX}}$	UART1 Transmit	C	PC_00
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB0_XTAL
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_OTP	VDD for OTP	Not Muxed	VDD_OTP
VDD_RTC	VDD for RTC	Not Muxed	VDD_RTC
VDD_USB	VDD for USB	Not Muxed	VDD_USB

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_DQ08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 8 Notes: No notes.
DMC0_DQ09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 9 Notes: No notes.
DMC0_DQ10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 10 Notes: No notes.
DMC0_DQ11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes.
DMC0_DQ12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes.
DMC0_DQ13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes.
DMC0_DQ14	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes.
DMC0_DQ15	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes.
DMC0_LDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes.
DMC0_LDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: For LPDDR, a pull-down is required.
$\overline{\text{DMC0\_LDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: For single ended DDR2, connect to DMC0_VREF. For LPDDR, leave unconnected.
DMC0_ODT	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_RAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes.
DMC0_UDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes.
DMC0_UDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: For LPDDR, a pull-down is required.
$\overline{\text{DMC0\_UDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: For single ended DDR2, connect to DMC0_VREF. For LPDDR, leave unconnected.
DMC0_VREF	a	na	none	none	none	none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: For LPDDR, leave unconnected. If the DMC is not used, connect to ground.
$\overline{\text{DMC0\_WE}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes.
GND	g	na	none	none	none	none	none	na	Desc: Ground Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
GND_HADC	g	na	none	none	none	none	none	na	Desc: Ground HADC Notes: If HADC is not used, connect to ground.
HADC0_VIN0	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If HADC is not used, connect to ground.
HADC0_VIN1	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If HADC is not used, connect to ground.
HADC0_VIN2	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If HADC is not used, connect to ground.
HADC0_VIN3	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If HADC is not used, connect to ground.
HADC0_VREFN	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: If HADC is not used, connect to ground.
HADC0_VREFP	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: If HADC is not used, connect to ground.
JTG_TCK_ SWCLK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Clock | Serial Wire Clock Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: Functional during reset.
JTG_TDO_SWO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out | Serial Wire Out Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS_ SWDIO	I/O	A	pu	none	none	none	none	VDD_EXT	Desc: JTAG Mode Select | Serial Wire DIO Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Reset Notes: Functional during reset, a 10k external pull-down may be used to shorten the t_{VDDEXT_RST} timing requirement.
PA_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Clock | TRACE0 Trace Data 7 | SMC0 Byte Enable 0 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PA_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master In, Slave Out | TRACE0 Trace Data 6 | SMC0 Byte Enable 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Frame Sync | TM0 Timer 3 | MSI0 Command Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Data 0 | SPI0 Master In, Slave Out | MSI0 Data 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Frame Sync | SPI0 Master Out, Slave In | MSI0 Data 2 | TM0 Alternate Capture Input 2 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Data 0 | SPI0 Data 2 | MSI0 Data 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Clock | SPI0 Data 3 | MSI0 Clock | TM0 Alternate Clock 2 Notes: No notes.
PC_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Clock | MSI0 Data 4 | SPI1 Slave Select Output 3 | TM0 Alternate Clock 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Frame Sync | MSI0 Data 5 | SPI0 Slave Select Output 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 0 | MSI0 Data 6 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 and Table 18 describe the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Core and System Clock Operating Conditions

Parameter		Ratio Restriction	PLLCLK Restriction	Min	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	PLLCLK = 800		400	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	600 ≤ PLLCLK < 800		390	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	380 ≤ PLLCLK < 600		380	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	230.2 ≤ PLLCLK < 380		PLLCLK	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		PLLCLK = 800	60	200	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		600 ≤ PLLCLK < 800	60	195	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		380 ≤ PLLCLK < 600	60	190	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		230.2 ≤ PLLCLK < 380	60	PLLCLK ÷ 2	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$		30	100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2 Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		125	200	MHz
f_{DCLK}	LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		10	200	MHz

[1] The minimum frequency for SYSCLK and SCLK0 applies only when the USB is used.

Table 18. Peripheral Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{OCLK}	Output Clock Frequency				50	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[1, 2]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				50	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				50	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{MSICLKPROG}$	Programmed MSI Clock				50	MHz

[1] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this typical specification for each end application.
[2] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[3] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications section for that peripheral. Pay particular attention to setup and hold times for VDD_EXT = 1.8 V which may preclude the maximum frequency listed here.
[4] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} that clocks the peripheral.

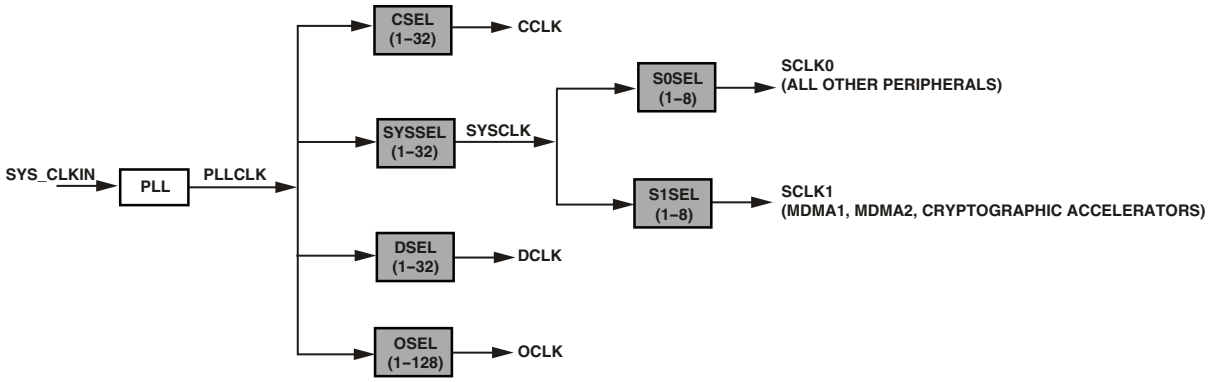

Figure 6. Clock Relationships and Divider Values

Table 19. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	230.2	800	MHz
CGU_CTL.MSEL[1]	PLL Multiplier	8	41	

[1] The CGU_CTL.MSEL setting must also be chosen to ensure that the f_{PLLCLK} specification is not violated.

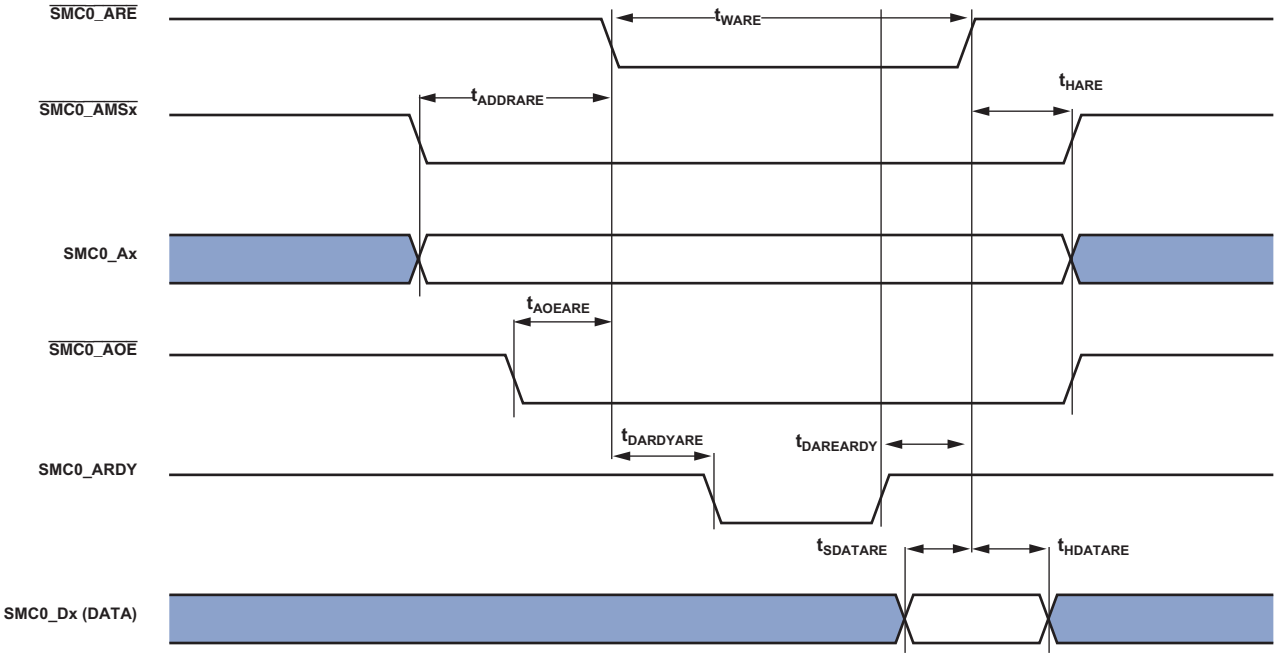

Figure 10. Asynchronous Read

Asynchronous Flash Read

Table 33 and Figure 12 show asynchronous flash memory read timing, related to the static memory controller (SMC).

Table 33. Asynchronous Flash Read

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before SMC0_NORDV Low[1]	PREST × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From SMC0_NORDV High[3]	PREAT × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$, $\overline{\text{SMC0\_AOE}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

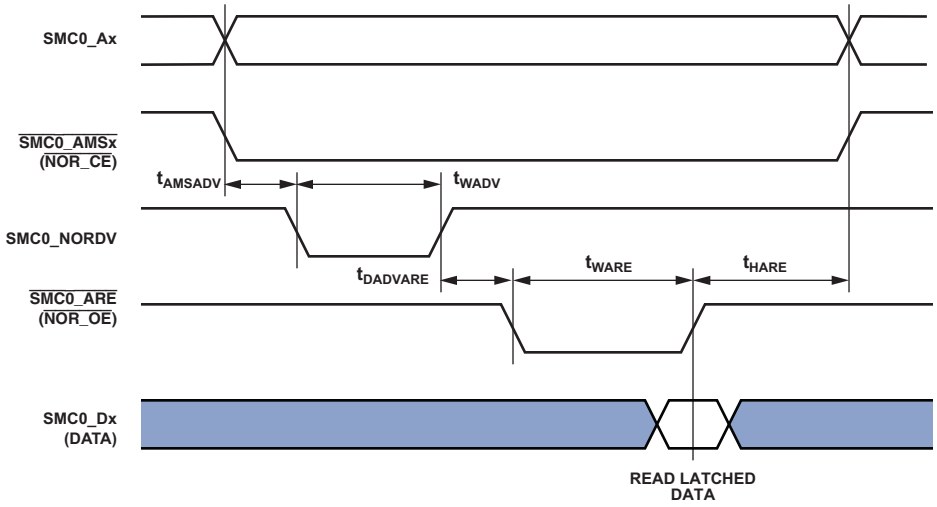

Figure 12. Asynchronous Flash Read

Mobile DDR SDRAM Write Cycle Timing

Table 44 and Figure 22 show mobile DDR SDRAM write cycle timing, related to the dynamic memory controller (DMC).

Table 44. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{DQSS}[1]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	1.8		ns

[1] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

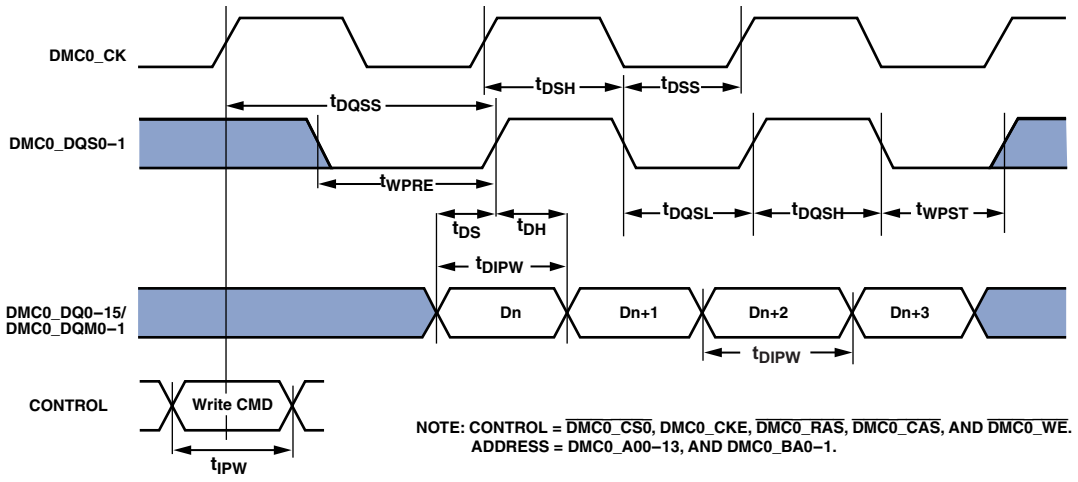

Figure 22. Mobile DDR SDRAM Controller Output AC Timing

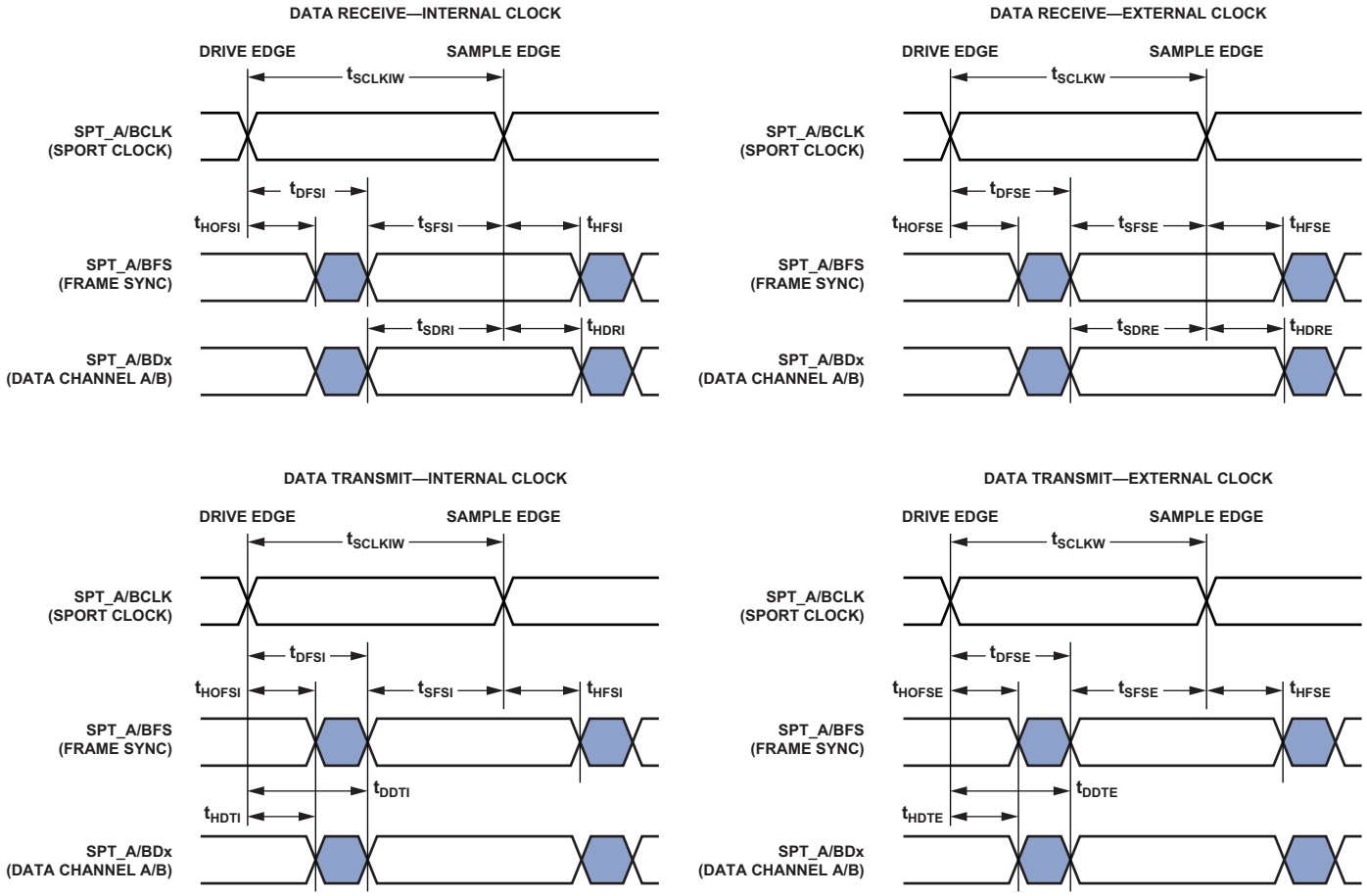

Figure 27. Serial Ports

Table 51. Serial Ports—Enable and Three-State

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		14		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1.12		–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8		2.8	ns

[1] Referenced to drive edge.

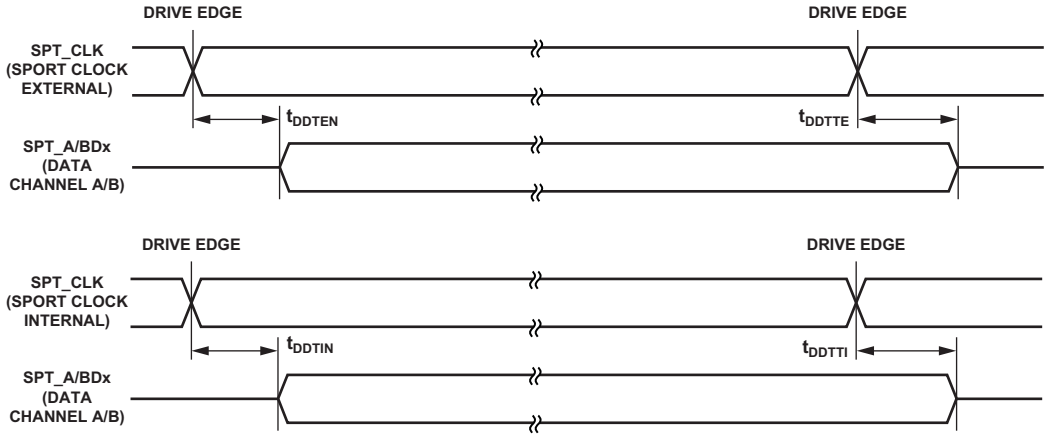

Figure 28. Serial Ports—Enable and Three-State

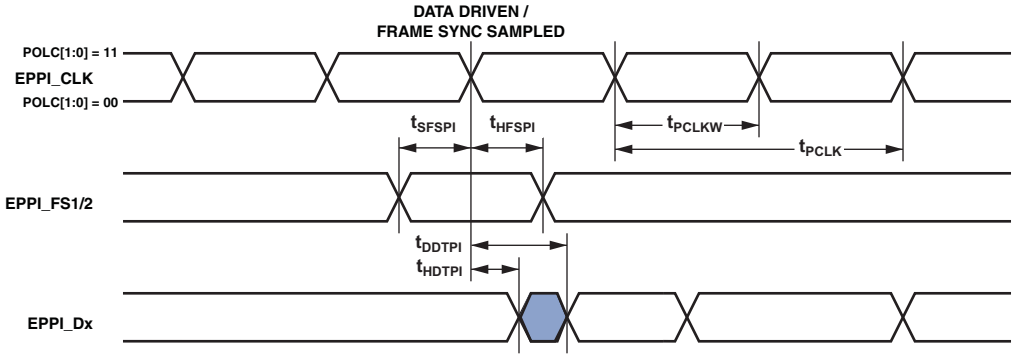

Figure 43. PPI Internal Clock GP Transmit Mode with External Frame Sync Timing

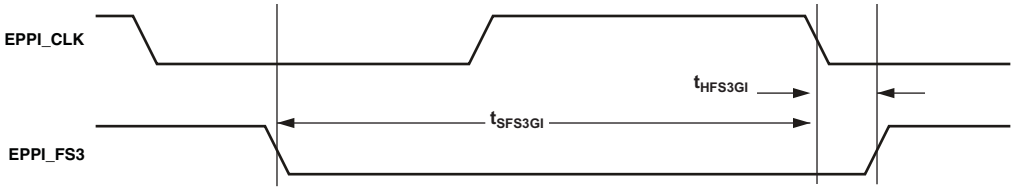

Figure 44. Clock Gating Mode with Internal Clock and External Frame Sync Timing

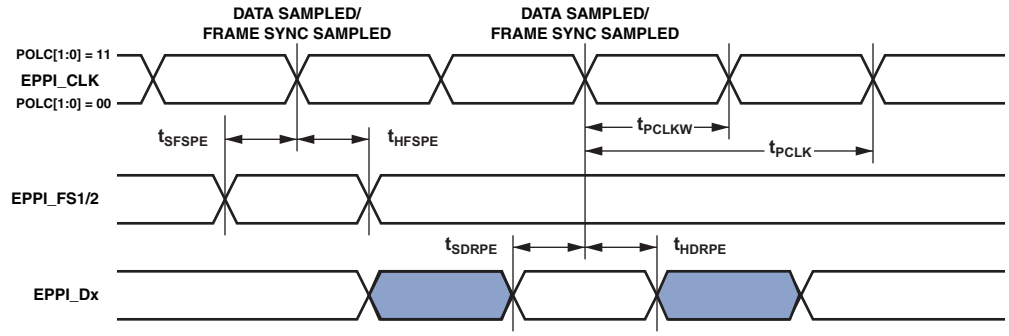

Figure 47. PPI External Clock GP Receive Mode with External Frame Sync Timing

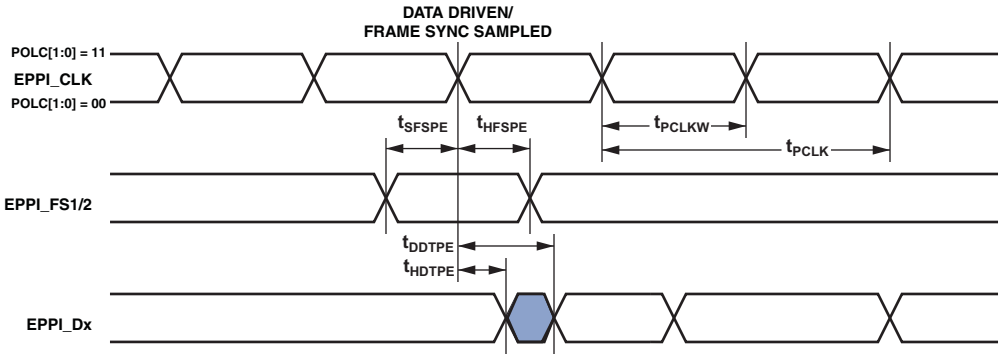

Figure 48. PPI External Clock GP Transmit Mode with External Frame Sync Timing

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 65 and Table 66.

P_D = Power dissipation (see Total Internal Power Dissipation on Page 56 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

In Table 65 and Table 66, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 65. Thermal Characteristics for CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	28.7	°C/W
θ_{JMA}	1 linear m/s air flow	26.2	°C/W
θ_{JMA}	2 linear m/s air flow	25.2	°C/W
θ_{JC}		10.1	°C/W
Ψ_{JT}	0 linear m/s air flow	0.24	°C/W
Ψ_{JT}	1 linear m/s air flow	0.40	°C/W
Ψ_{JT}	2 linear m/s air flow	0.51	°C/W

Table 66. Thermal Characteristics for LFCSP (QFN)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	22.9	°C/W
θ_{JMA}	1 linear m/s air flow	17.9	°C/W
θ_{JMA}	2 linear m/s air flow	16.4	°C/W
θ_{JC}		2.26	°C/W
Ψ_{JT}	0 linear m/s air flow	0.14	°C/W
Ψ_{JT}	1 linear m/s air flow	0.27	°C/W
Ψ_{JT}	2 linear m/s air flow	0.30	°C/W

Table 67. 184-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A01	GND	D08	VDD_DMC	H03	SYS_CLKOUT	L14	GND
A02	DMC0_A09	D09	VDD_DMC	H04	VDD_INT	M01	PC_00
A03	DMC0_BA0	D12	PA_08	H05	GND	M02	RTC0_CLKIN
A04	DMC0_BA1	D13	DMC0_DQ06	H06	GND	M03	PB_15
A05	DMC0_BA2	D14	DMC0_DQ05	H07	GND	M04	PB_12
A06	$\overline{\text{DMC0\_CAS}}$	E01	DMC0_A06	H08	GND	M05	PC_12
A07	$\overline{\text{DMC0\_RAS}}$	E02	DMC0_A05	H09	GND	M06	USB0_VBUS
A08	DMC0_A13	E03	JTG_TDI	H10	GND	M07	USB0_VBC
A09	PA_03	E05	VDD_INT	H11	VDD_DMC	M08	PB_09
A10	DMC0_CK	E06	VDD_DMC	H12	PA_10	M09	PB_05
A11	$\overline{\text{DMC0\_CK}}$	E07	VDD_DMC	H13	PA_11	M10	PB_04
A12	DMC0_LDQS	E08	VDD_DMC	H14	$\overline{\text{DMC0\_UDQS}}$	M11	PB_01
A13	$\overline{\text{DMC0\_LDQS}}$	E09	VDD_DMC	J01	PC_05	M12	PB_03
A14	GND	E10	DMC0_VREF	J02	PC_06	M13	DMC0_LDM
B01	DMC0_A07	E12	SYS_BMODE0	J03	$\overline{\text{SYS\_RESOUT}}$	M14	SYS_CLKIN
B02	DMC0_A08	E13	DMC0_DQ08	J04	VDD_INT	N01	RTC0_XTAL
B03	DMC0_A11	E14	DMC0_DQ07	J05	VDD_RTC	N02	PB_14
B04	DMC0_A10	F01	DMC0_A01	J06	GND	N03	PB_11
B05	DMC0_A12	F02	DMC0_A02	J07	GND	N04	PC_14
B06	$\overline{\text{DMC0\_WE}}$	F03	PC_09	J08	GND	N05	PC_11
B07	$\overline{\text{DMC0\_CS0}}$	F04	VDD_INT	J09	GND	N06	USB0_ID
B08	DMC0_ODT	F05	VDD_INT	J10	GND_HADC	N07	USB0_DP
B09	DMC0_CKE	F06	GND	J11	VDD_OTP	N08	PB_08
B10	DMC0_DQ00	F07	GND	J12	PA_13	N09	PB_06
B11	DMC0_DQ02	F08	GND	J13	DMC0_DQ13	N10	PB_00
B12	DMC0_DQ01	F09	GND	J14	DMC0_UDQS	N11	HADC0_VIN2
B13	DMC0_DQ04	F10	VDD_DMC	K01	PC_04	N12	HADC0_VIN1
B14	DMC0_DQ03	F11	VDD_DMC	K02	PC_01	N13	PA_15
C01	JTG_TDO_SWO	F12	$\overline{\text{SYS\_FAULT}}$	K03	PC_02	N14	SYS_XTAL
C02	JTG_TMS_SWDIO	F13	DMC0_DQ10	K05	VDD_EXT	P01	GND
C03	JTG_TCK_SWCLK	F14	DMC0_DQ09	K06	VDD_EXT	P02	PB_13
C04	PA_01	G01	DMC0_A03	K07	VDD_EXT	P03	PB_10
C05	SYS_EXTWAKE	G02	PA_00	K08	VDD_EXT	P04	PC_13
C06	PA_02	G03	PC_08	K09	VDD_EXT	P05	USB0_XTAL
C07	$\overline{\text{SYS\_NMI}}$	G04	VDD_INT	K10	VDD_HADC	P06	USB0_CLKIN
C08	GND	G05	GND	K12	PA_12	P07	USB0_DM
C09	PA_04	G06	GND	K13	DMC0_DQ15	P08	PB_07
C10	PA_05	G07	GND	K14	DMC0_DQ14	P09	HADC0_VREFN
C11	PA_06	G08	GND	L01	PC_03	P10	HADC0_VREFP
C12	PA_07	G09	GND	L02	TWI0_SDA	P11	HADC0_VIN3
C13	$\overline{\text{SYS\_HWRST}}$	G10	GND	L03	TWI0_SCL	P12	HADC0_VIN0
C14	SYS_BMODE1	G11	VDD_DMC	L06	VDD_USB	P13	PA_14
D01	DMC0_A00	G12	PA_09	L07	VDD_EXT	P14	GND
D02	DMC0_A04	G13	DMC0_DQ11	L08	VDD_EXT		
D03	$\overline{\text{JTG\_TRST}}$	G14	DMC0_DQ12	L09	VDD_EXT		
D06	VDD_DMC	H01	PC_07	L12	PB_02		
D07	VDD_DMC	H02	PC_10	L13	DMC0_UDM		

Table 69 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by lead number for the ADSP-BF70x. Table 70 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by signal.

Table 69. 12 mm × 12 mm 88-Lead LFCSP (QFN) Lead Assignment (Numerical by Lead Number)

Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name
1	PC_10	24	PB_14	47	PB_02	70	PA_07
2	PC_09	25	PB_13	48	PB_01	71	PA_06
3	PC_08	26	VDD_EXT	49	VDD_OTP	72	VDD_EXT
4	VDD_EXT	27	PB_12	50	VDD_EXT	73	PA_05
5	PC_07	28	PB_11	51	VDD_INT	74	PA_04
6	PC_06	29	PB_10	52	PB_00	75	PA_03
7	PC_05	30	VDD_INT	53	PA_15	76	GND
8	PC_04	31	USB0_XTAL	54	PA_14	77	$\overline{\text{SYS\_NMI}}$
9	PC_03	32	USB0_CLKIN	55	VDD_EXT	78	PA_02
10	PC_02	33	USB0_ID	56	SYS_XTAL	79	SYS_EXTWAKE
11	VDD_EXT	34	USB0_VBUS	57	SYS_CLKIN	80	PA_01
12	SYS_CLKOUT	35	USB0_DP	58	PA_13	81	VDD_INT
13	PC_01	36	VDD_USB	59	PA_12	82	VDD_EXT
14	VDD_INT	37	USB0_DM	60	PA_11	83	JTG_TDO_SWO
15	$\overline{\text{SYS\_RESOUT}}$	38	USB0_VBC	61	VDD_INT	84	JTG_TMS_SWDIO
16	PC_00	39	PB_09	62	VDD_EXT	85	JTG_TCK_SWCLK
17	VDD_EXT	40	PB_08	63	PA_10	86	JTG_TDI
18	TWI0_SDA	41	VDD_EXT	64	PA_09	87	$\overline{\text{JTG\_TRST}}$
19	TWI0_SCL	42	PB_07	65	$\overline{\text{SYS\_FAULT}}$	88	PA_00
20	RTC0_XTAL	43	PB_06	66	SYS_BMODE0	89*	GND
21	RTC0_CLKIN	44	PB_05	67	SYS_BMODE1		
22	VDD_RTC	45	PB_04	68	$\overline{\text{SYS\_HWRST}}$		
23	PB_15	46	PB_03	69	PA_08		

*Pin no. 89 is the GND supply (see Figure 70) for the processor; this pad must connect to GND.