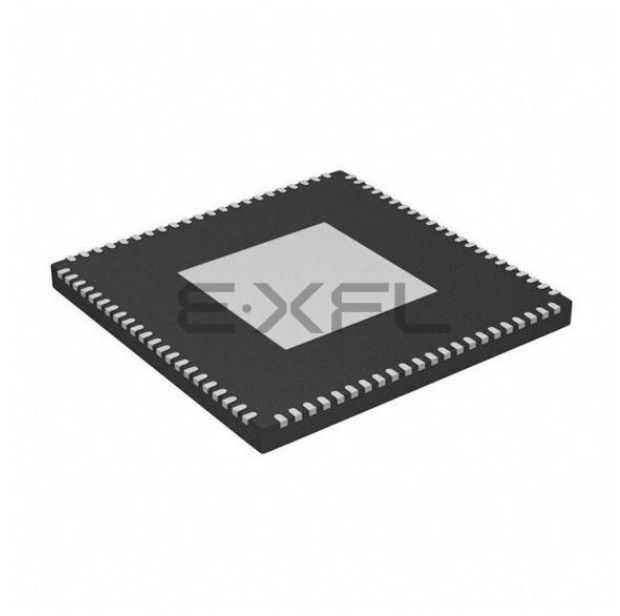

! "#

$ % & % ' %% % ( )
(& & *

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

++ , ' %% % ( )
(& & *

Product Status	Active
Type	² lackfinC
Interface	RAO, DSPI, E² I/E3 I, I0R, PPI, MSPI, SD/SDIN, SPI, SPNVT, UAVT/USAVT, US² NTG
Rlock Vate	1663 Hz
Oon-Bolatile 3 emory	VN3 (825k²)
Nn-Rhip VA3	23 ²
Boltage - I/N	2.4B, °.°B
Boltage - Rore	2.26B
Nperating Temperature	-16-R : 268-R (TA)
3 ounting Type	Surface 3 ount
Package / Rase	44-BFMFO Exposed Pad, RSP
Supplier Device Package	44-LFRSP-BM (25x25)
Purchase UVL	https@/www.e-xfl.com/product-detail/analog-devices/adbfX6Wwccpz122

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9/15—Rev. 0 to Rev. A

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GENERAL DESCRIPTION

The ADSP-BF70x processor is a member of the Blackfin® family of products. The Blackfin processor combines a dual-MAC 16-bit state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture. New enhancements to the Blackfin+ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements—all while maintaining instruction set compatibility to previous Blackfin products.

The processor offers performance up to 400 MHz, as well as low static power consumption. Produced with a low-power and low-voltage design methodology, they provide world-class power management and performance.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the Blackfin processor is the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package. These applications span a wide array of markets, from automotive systems to embedded industrial, instrumentation, video/image analysis, biometric and power/motor control applications.

Table 1. Processor Comparison

Processor Feature		ADSP-BF700	ADSP-BF701	ADSP-BF702	ADSP-BF703	ADSP-BF704	ADSP-BF705	ADSP-BF706	ADSP-BF707
Maximum Speed Grade (MHz)[1]		200		400					
Maximum SYSCLK (MHz)		100		200					
Package Options		88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA
GPIOs		43	47	43	47	43	47	43	47
Memory (bytes)	L1 Instruction SRAM	48K							
	L1 Instruction SRAM/Cache	16K							
	L1 Data SRAM	32K							
	L1 Data SRAM/Cache	32K							
	L1 Scratchpad (L1 Data C)	8K							
	L2 SRAM	128K		256K		512K		1024K	
	L2 ROM	512K							
	DDR2/LPDDR (16-bit)	No	Yes	No	Yes	No	Yes	No	Yes
I^2C		1							
Up/Down/Rotary Counter		1							
GP Timer		8							
Watchdog Timer		1							
GP Counter		1							
SPORTs		2							
Quad SPI		2							
Dual SPI		1							
SPI Host Port		1							
USB 2.0 HS OTG		1							
Parallel Peripheral Interface		1							
CAN		2							
UART		2							
Real-Time Clock		1							
Static Memory Controller (SMC)		Yes							
Security Crypto Engine		Yes							
SD/SDIO (MSI)		4-bit	8-bit	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit
4-Channel 12-Bit ADC		No	Yes	No	Yes	No	Yes	No	Yes

[1] Other speed grades available.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with dynamic branch prediction), and subroutine calls. Hardware supports zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

The Blackfin processor supports a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

INSTRUCTION SET DESCRIPTION

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. The Blackfin processor supports a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Control of all asynchronous and synchronous events to the processor is handled by two subsystems: the core event controller (CEC) and the system event controller (SEC).
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADSP-BF70x processor.

DMA Controllers

The processor uses direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processor can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory-to-memory DMA stream uses two channels, where one channel is the source channel, and the second is the destination channel.

All DMAs can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers, descriptor-based or register-based. Register-based DMA allows the processor to directly program DMA control registers to initiate a DMA transfer. On completion, the control registers may be automatically updated with their original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together and a DMA channel can be programmed to automatically set up and start another DMA transfer after the current sequence completes.

The DMA controller supports the following DMA operations.

- A single linear buffer that stops on completion.
- A linear buffer with negative, positive, or zero stride length.
- A circular, auto-refreshing buffer that interrupts when each buffer becomes full.

General-Purpose Timers

There is one GP timer unit, and it provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TIMER_TMRx pins, an external TIMER_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals through the TRU (for instance, to signal a fault). Each timer may also be started and/or stopped by any TRU master without core intervention.

Core Timer

The processor core also has its own dedicated timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Watchdog Timer

The core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value. This protects the system from remaining in an unknown state where software that would normally reset the timer has stopped running due to an external noise condition or software error.

After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in its timer control register that is set only upon a watchdog-generated reset.

Serial Ports (SPORTs)

Two synchronous serial ports (comprised of four half-SPORTs) provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' audio codecs, ADCs, and DACs. Each half-SPORT is made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory through dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. In this configuration, one SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in six modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode
- Right-justified mode

General-Purpose Counters

A 32-bit counter is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumbwheel devices. All three pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable this timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

Parallel Peripheral Interface (PPI)

The processor provides a parallel peripheral interface (PPI) that supports data widths up to 18 bits. The PPI supports direct connection to TFT LCD panels, parallel analog-to-digital and digital-to-analog converters, video encoders and decoders, image sensor modules, and other general-purpose peripherals.

The following features are supported in the PPI module:

- Programmable data length: 8 bits, 10 bits, 12 bits, 14 bits, 16 bits, and 18 bits per clock.
- Various framed, non-framed, and general-purpose operating modes. Frame syncs can be generated internally or can be supplied by an external device.
- ITU-656 status word error detection and correction for ITU-656 receive modes and ITU-656 preamble and status word decode.
- Optional packing and unpacking of data to/from 32 bits from/to 8 bits, 16 bits and 24 bits. If packing/unpacking is enabled, endianness can be configured to change the order of packing/unpacking of bytes/words.
- RGB888 can be converted to RGB666 or RGB565 for transmit modes.
- Various de-interleaving/interleaving modes for receiving/transmitting 4:2:2 YCrCb data.
- Configurable LCD data enable (DEN) output available on Frame Sync 3.

level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over the required temperature range.

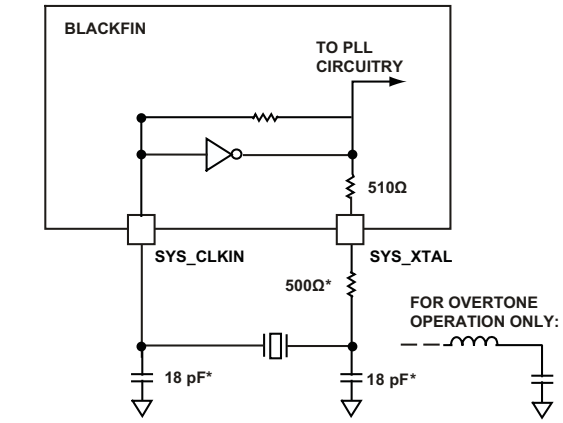

Figure 4. External Crystal Connection

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) *Using Third Overtone Crystals with the ADSP-218x DSP* (www.analog.com/ee-168).

The same recommendations may be used for the USB crystal oscillator.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. Connect RTC pins RTC_CLKIN and RTC_XTAL with external components as shown in Figure 5.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms. The first alarm is for a time of day. The second alarm is for a specific day and time of that day.

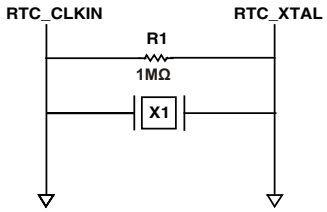

Figure 5. External Components for RTC

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0, and SCLK1), the LPDDR or DDR2 clock (DCLK), and the output clock (OCLK).

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ can be applied after all voltage supplies are within specifications, and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example, PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be output on the SYS_CLKOUT pin.

ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_ARE	SMC0 Read Enable	A	PA_13
SMC0_AWE	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_12
SMC0_D13	SMC0 Data 13	B	PB_13
SMC0_D14	SMC0 Data 14	B	PB_14
SMC0_D15	SMC0 Data 15	B	PB_15
SPI0_CLK	SPI0 Clock	B	PB_00
SPI0_CLK	SPI0 Clock	C	PC_04
SPI0_D2	SPI0 Data 2	B	PB_03
SPI0_D2	SPI0 Data 2	C	PC_08
SPI0_D3	SPI0 Data 3	B	PB_07
SPI0_D3	SPI0 Data 3	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	B	PB_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_06
SPI0_MOSI	SPI0 Master Out, Slave In	B	PB_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_07
SPI0_RDY	SPI0 Ready	A	PA_06
SPI0_SEL1	SPI0 Slave Select Output 1	A	PA_05
SPI0_SEL2	SPI0 Slave Select Output 2	A	PA_06
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_11
SPI0_SEL4	SPI0 Slave Select Output 4	B	PB_04
SPI0_SEL5	SPI0 Slave Select Output 5	B	PB_05
SPI0_SEL6	SPI0 Slave Select Output 6	B	PB_06
SPI0_SS	SPI0 Slave Select Input	A	PA_05
SPI1_CLK	SPI1 Clock	A	PA_00
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_01
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_02
SPI1_RDY	SPI1 Ready	A	PA_03
SPI1_SEL1	SPI1 Slave Select Output 1	A	PA_04
SPI1_SEL2	SPI1 Slave Select Output 2	A	PA_03
SPI1_SEL3	SPI1 Slave Select Output 3	C	PC_10
SPI1_SEL4	SPI1 Slave Select Output 4	A	PA_14
SPI1_SS	SPI1 Slave Select Input	A	PA_04
SPI2_CLK	SPI2 Clock	B	PB_10

12 mm × 12 mm 88-LEAD LFCSP (QFN) SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 11. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
GND	Ground	Not Muxed	GND
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG\_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_10	Position 00 through Position 10	C	PC_00-PC_10
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 6 Notes: No notes.
DMC0_A07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 7 Notes: No notes.
DMC0_A08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 8 Notes: No notes.
DMC0_A09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 9 Notes: No notes.
DMC0_A10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 10 Notes: No notes.
DMC0_A11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 11 Notes: No notes.
DMC0_A12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 12 Notes: No notes.
DMC0_A13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 13 Notes: No notes.
DMC0_BA0	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 0 Notes: No notes.
DMC0_BA1	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 1 Notes: No notes.
DMC0_BA2	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 2 Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_CAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes.
DMC0_CK	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes.
$\overline{\text{DMC0\_CK}}$	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock (complement) Notes: No notes.
DMC0_CKE	I/O	B	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock enable Notes: No notes.
$\overline{\text{DMC0\_CS0}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Chip Select 0 Notes: No notes.
DMC0_DQ00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 0 Notes: No notes.
DMC0_DQ01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 1 Notes: No notes.
DMC0_DQ02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 2 Notes: No notes.
DMC0_DQ03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 3 Notes: No notes.
DMC0_DQ04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 4 Notes: No notes.
DMC0_DQ05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 5 Notes: No notes.
DMC0_DQ06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 6 Notes: No notes.
DMC0_DQ07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 7 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
GND_HADC	g	na	none	none	none	none	none	na	Desc: Ground HADC Notes: If HADC is not used, connect to ground.
HADC0_VIN0	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If HADC is not used, connect to ground.
HADC0_VIN1	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If HADC is not used, connect to ground.
HADC0_VIN2	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If HADC is not used, connect to ground.
HADC0_VIN3	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If HADC is not used, connect to ground.
HADC0_VREFN	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: If HADC is not used, connect to ground.
HADC0_VREFP	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: If HADC is not used, connect to ground.
JTG_TCK_ SWCLK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Clock | Serial Wire Clock Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: Functional during reset.
JTG_TDO_SWO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out | Serial Wire Out Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS_ SWDIO	I/O	A	pu	none	none	none	none	VDD_EXT	Desc: JTAG Mode Select | Serial Wire DIO Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Reset Notes: Functional during reset, a 10k external pull-down may be used to shorten the t_{VDDEXT_RST} timing requirement.
PA_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Clock | TRACE0 Trace Data 7 | SMC0 Byte Enable 0 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PA_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master In, Slave Out | TRACE0 Trace Data 6 | SMC0 Byte Enable 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
VDD_OTP	s	na	none	none	none	none	none	na	Desc: VDD for OTP Notes: Must be powered.
VDD_RTC	s	na	none	none	none	none	none	na	Desc: VDD for RTC Notes: If RTC is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB Notes: If USB is not used, connect to VDD_EXT.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0		33		µA
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current Without USB	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0, USB protection disabled (USB_PHY_CTLDIS = 1)		15		µA
I_{DD_INT}[18]	V_{DD_INT} Current	V_{DD_INT} within operating conditions table specifications			See I_{DDINT_TOT} equation on on Page 56	mA
I_{DD_RTC}	I_{DD_RTC} Current	V_{DD_RTC} = 3.3 V, T_J = 125°C			10	µA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals, and USB0 signals.

[2] Applies to DMC0_Axx, DMC0_CAS, DMC0_CKE, DMC0_CK, DMC0_CK, DMC0_CS, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, DMC0_LDQS, DMC0_ODT, DMC0_RAS, DMC0_UDM, DMC0_UDQS, DMC0_UDQS, and DMC0_WE signals.

[3] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.

[4] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TDI, and JTG_TMS_SWDIO signals.

[5] Applies to DMC0_VREF signal.

[6] Applies to JTG_TCK_SWCLK and JTG_TRST signals.

[7] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TCK, and JTG_TRST signals.

[8] Applies to JTG_TDI, JTG_TMS_SWDIO, PA_xx, PB_xx, and PC_xx signals when internal GPIO pull-ups are enabled. For information on when internal pull-ups are enabled for GPIOs. See ADSP-BF70x Designer Quick Reference on Page 38.

[9] Applies to USB0_CLKIN signal.

[10] Applies to PA_xx, PB_xx, PC_xx, SMC0_AMS0, SMC0_ARE, SMC0_AWE, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, and USB0_VBC signals.

[11] Applies to DMC0_Axx, DMC0_BAxx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, and DMC0_WE signals.

[12] Applies to PA_xx, PB_xx, PC_xx, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_Axx, DMC0_BAx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, DMC0_WE, and TWI signals.

[13] Applies to USB0_VBUS signals.

[14] Applies to all TWI signals.

[15] Applies to all signals, except DMC0 and TWI signals.

[16] Applies to all DMC0 signals.

[17] See the *ADSP-BF70x Blackfin+ Processor Hardware Reference* for definition of deep sleep and hibernate operating modes.

[18] Additional information can be found at Total Internal Power Dissipation.

[19] Applies to VDD_EXT, VDD_DMC, and VDD_USB supply signals only. Clock inputs are tied high or low.

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current (deep sleep)
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DDINT\_TOT} = I_{DDINT\_DEEPSLEEP} + I_{DDINT\_CCLK\_DYN} + I_{DDINT\_PLLCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_USBCLK\_DYN}$$

$I_{DDINT\_DEEPSLEEP}$ is the only item present that is part of the static power dissipation component. $I_{DDINT\_DEEPSLEEP}$ is specified as a function of voltage (V_{DD_INT}) and temperature (see Table 21).

There are eight different items that contribute to the dynamic power dissipation. These components fall into three broad categories: application-dependent currents, clock currents, and data transmission currents.

Application-Dependent Current

The application-dependent currents include the dynamic current in the core clock domain.

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor cores and L1/L2 memories (Table 22). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent data in Table 23 to calculate this portion.

$I_{DDINT\_CCLK\_DYN}$ (mA) = Table 23 × *ASF*

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency and a unique scaling factor.

$I_{DDINT\_PLLCLK\_DYN}$ (mA) = 0.012 × f_{PLLCLK} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SYSCLK\_DYN}$ (mA) = 0.120 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK0\_DYN}$ (mA) = 0.110 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK1\_DYN}$ (mA) = 0.068 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_DCLK\_DYN}$ (mA) = 0.055 × f_{DCLK} (MHz) × V_{DD_INT} (V)

The dynamic component of the USB clock is a unique case. The USB clock contributes a near constant current value when used.

Table 20. $I_{DDINT\_USBCLK\_DYN}$ Current

Is USB Enabled?	$I_{DDINT\_USBCLK\_DYN}$ (mA)
Yes – High-Speed Mode	13.94
Yes – Full-Speed Mode	10.83
Yes – Suspend Mode	5.2
No	0.34

Data Transmission Current

The data transmission current represents the power dissipated when transmitting data. This current is expressed in terms of data rate. The calculation is performed by adding the data rate (MB/s) of each DMA-driven access to peripherals, L1, L2, and external memory. This number is then multiplied by a weighted data-rate coefficient and V_{DD_INT}:

$I_{DDINT\_DMADR\_DYN}$ (mA) = *Weighted DRC* × *Total Data Rate* (MB/s) × V_{DD_INT} (V)

A weighted data-rate coefficient is used because different coefficients exist depending on the source and destination of the transfer. For details on using this equation and calculating the weighted DRC, see the related Engineer Zone material. For a quick maximum calculation, the weighted DRC can be assumed to be 0.0497, which is the coefficient for L1 to L1 transfers.

Table 21. Static Current—$I_{DD\_DEEPSLEEP}$ (mA)

	Voltage (V_{DD_INT})												
T_J (°C)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
–40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
–20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

Table 22. Activity Scaling Factors (ASF)

I_{DDINT} Power Vector	ASF
$I_{DD-IDLE1}$	0.05
$I_{DD-IDLE2}$	0.05
$I_{DD-NOP1}$	0.56
$I_{DD-NOP2}$	0.59
$I_{DD-APP3}$	0.78
$I_{DD-APP1}$	0.79
$I_{DD-APP2}$	0.83
$I_{DD-TYP1}$	1.00
$I_{DD-TYP3}$	1.01
$I_{DD-TYP2}$	1.03
$I_{DD-HIGH1}$	1.39
$I_{DD-HIGH3}$	1.39
$I_{DD-HIGH2}$	1.54

Table 23. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})												
f_{CCLK} (MHz)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

HADC

HADC Electrical Characteristics

Table 24. HADC Electrical Characteristics

Parameter	Test Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current Consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current Consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current Consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down	10	µA

HADC DC Accuracy

Table 25. HADC DC Accuracy

Parameter	Typ	Unit
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB[1]
Differential Nonlinearity (DNL)	±2	LSB[1]
Offset Error	±8	LSB[1]
Offset Error Matching	±10	LSB[1]
Gain Error	±4	LSB[1]
Gain Error Matching	±4	LSB[1]

[1] LSB = HADC0_VREFP ÷ 4096

HADC Timing Specifications

Table 26. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

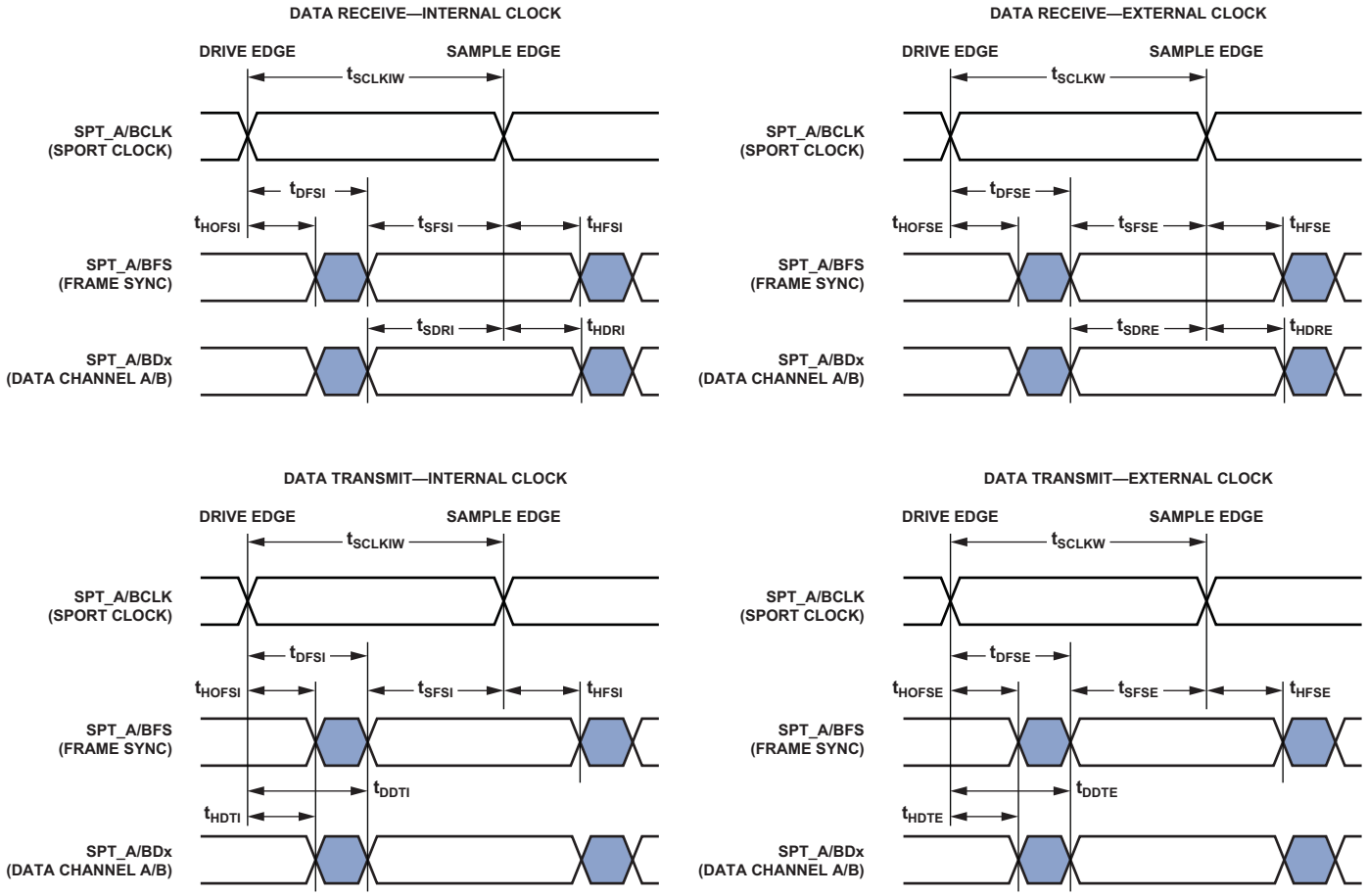

Figure 27. Serial Ports

Mobile Storage Interface (MSI) Controller Timing

Table 64 and Figure 49 show I/O timing, related to the mobile storage interface (MSI).

The MSI timing depends on the period of the input clock that has been routed to the MSI peripheral ($t_{MSICLKIN}$) by setting the MSI0_UHS_EXT register. See Table 63 for this information.

Table 63. $t_{MSICLKIN}$ Settings

EXT_CLK_MUX_CTRL[31:30]	$t_{MSICLKIN}$
00	$t_{SCLK0} \times 2$
01	t_{SCLK0}
10	$t_{SCLK1} \times 3$

$$t_{MSICLKIN} = \frac{1}{f_{MSICLKIN}}$$

($f_{MSICLKPROG}$) frequency in MHz is set by the following equation where DIV0 is a field in the MSI_CLKDIV register that can be set from 0 to 255. When DIV0 is set between 1 and 255, the following equation is used to determine $f_{MSICLKPROG}$:

$$f_{MSICLKPROG} = \frac{f_{MSICLKIN}}{DIV0 \times 2}$$

When DIV0 = 0,

$$f_{MSICLKPROG} = f_{MSICLKIN}$$

Also note the following:

$$t_{MSICLKPROG} = \frac{1}{f_{MSICLKPROG}}$$

Table 64. MSI Controller Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{ISU}	Input Setup Time	5.5		4.7		ns
t_{IH}	Input Hold Time	2		0.5		ns
Switching Characteristics						
t_{MSICLK}	Clock Period Data Transfer Mode[1]	$t_{MSICLKPROG} - 1.5$		$t_{MSICLKPROG} - 1.5$		ns
t_{WL}	Clock Low Time	7		7		ns
t_{WH}	Clock High Time	7		7		ns
t_{TLH}	Clock Rise Time		3		3	ns
t_{THL}	Clock Fall Time		3		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		$(0.5 \times t_{MSICLKIN}) + 3.2$		$(0.5 \times t_{MSICLKIN}) + 3$	ns
t_{OH}	Output Hold Time	$(0.5 \times t_{MSICLKIN}) - 4$		$(0.5 \times t_{MSICLKIN}) - 3$		ns

[1] See Table 18 on Page 52 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{MSICLKPROG}$.

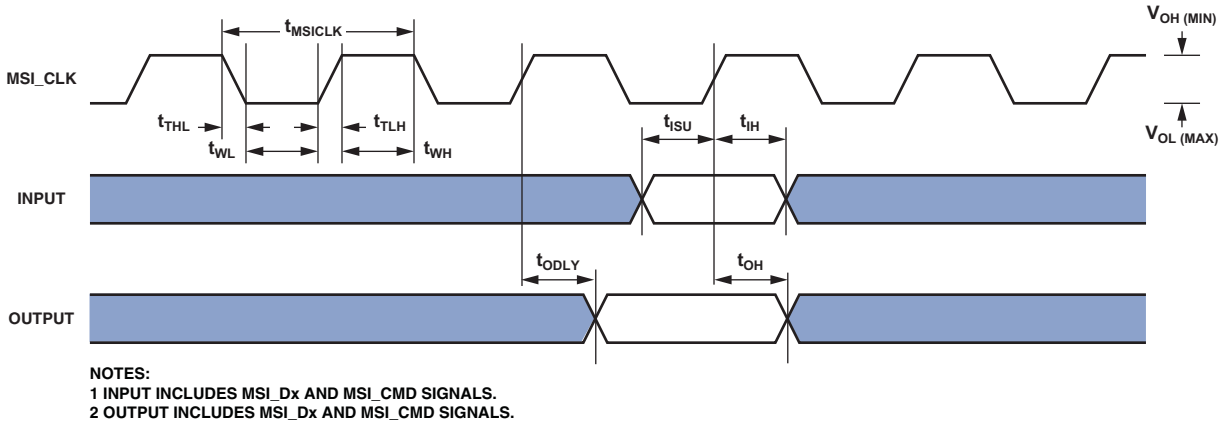

Figure 49. MSI Controller Timing

Table 68. ADSP-BF70x 184-Ball CSP_BGA Ball Assignments (Alphabetical by Signal Name)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
DMC0_A00	D01	DMC0_WE	B06	PA_08	D12	SYS_HWRST	C13
DMC0_A01	F01	GND	C08	PA_09	G12	SYS_NMI	C07
DMC0_A02	F02	GND	A01	PA_10	H12	SYS_RESOUT	J03
DMC0_A03	G01	GND	A14	PA_11	H13	SYS_XTAL	N14
DMC0_A04	D02	GND	F06	PA_12	K12	TWI0_SCL	L03
DMC0_A05	E02	GND	F07	PA_13	J12	TWI0_SDA	L02
DMC0_A06	E01	GND	F08	PA_14	P13	USB0_CLKIN	P06
DMC0_A07	B01	GND	F09	PA_15	N13	USB0_DM	P07
DMC0_A08	B02	GND	G05	PB_00	N10	USB0_DP	N07
DMC0_A09	A02	GND	G06	PB_01	M11	USB0_ID	N06
DMC0_A10	B04	GND	G07	PB_02	L12	USB0_VBC	M07
DMC0_A11	B03	GND	G08	PB_03	M12	USB0_VBUS	M06
DMC0_A12	B05	GND	G09	PB_04	M10	USB0_XTAL	P05
DMC0_A13	A08	GND	G10	PB_05	M09	VDD_DMC	D06
DMC0_BA0	A03	GND	H05	PB_06	N09	VDD_DMC	D07
DMC0_BA1	A04	GND	H06	PB_07	P08	VDD_DMC	D08
DMC0_BA2	A05	GND	H07	PB_08	N08	VDD_DMC	D09
DMC0_CAS	A06	GND	H08	PB_09	M08	VDD_DMC	E06
DMC0_CK	A10	GND	H09	PB_10	P03	VDD_DMC	E07
DMC0_CKE	B09	GND	H10	PB_11	N03	VDD_DMC	E08
DMC0_CK	A11	GND	J06	PB_12	M04	VDD_DMC	E09
DMC0_CS0	B07	GND	J07	PB_13	P02	VDD_DMC	F10
DMC0_DQ00	B10	GND	J08	PB_14	N02	VDD_DMC	F11
DMC0_DQ01	B12	GND	J09	PB_15	M03	VDD_DMC	G11
DMC0_DQ02	B11	GND	L14	PC_00	M01	VDD_DMC	H11
DMC0_DQ03	B14	GND	P01	PC_01	K02	VDD_EXT	K05
DMC0_DQ04	B13	GND	P14	PC_02	K03	VDD_EXT	K06
DMC0_DQ05	D14	GND_HADC	J10	PC_03	L01	VDD_EXT	K07
DMC0_DQ06	D13	HADC0_VIN0	P12	PC_04	K01	VDD_EXT	K08
DMC0_DQ07	E14	HADC0_VIN1	N12	PC_05	J01	VDD_EXT	K09
DMC0_DQ08	E13	HADC0_VIN2	N11	PC_06	J02	VDD_EXT	L07
DMC0_DQ09	F14	HADC0_VIN3	P11	PC_07	H01	VDD_EXT	L08
DMC0_DQ10	F13	HADC0_VREFN	P09	PC_08	G03	VDD_EXT	L09
DMC0_DQ11	G13	HADC0_VREFP	P10	PC_09	F03	VDD_HADC	K10
DMC0_DQ12	G14	JTG_TCK_SWCLK	C03	PC_10	H02	VDD_INT	E05
DMC0_DQ13	J13	JTG_TDI	E03	PC_11	N05	VDD_INT	F04
DMC0_DQ14	K14	JTG_TDO_SWO	C01	PC_12	M05	VDD_INT	F05
DMC0_DQ15	K13	JTG_TMS_SWDIO	C02	PC_13	P04	VDD_INT	G04
DMC0_LDM	M13	JTG_TRST	D03	PC_14	N04	VDD_INT	H04
DMC0_LDQS	A12	PA_00	G02	RTC0_CLKIN	M02	VDD_INT	J04
DMC0_LDQS	A13	PA_01	C04	RTC0_XTAL	N01	VDD_OTP	J11
DMC0_ODT	B08	PA_02	C06	SYS_BMODE0	E12	VDD_RTC	J05
DMC0_RAS	A07	PA_03	A09	SYS_BMODE1	C14	VDD_USB	L06
DMC0_UDM	L13	PA_04	C09	SYS_CLKIN	M14		
DMC0_UDQS	J14	PA_05	C10	SYS_CLKOUT	H03		
DMC0_UDQS	H14	PA_06	C11	SYS_EXTWAKE	C05		
DMC0_VREF	E10	PA_07	C12	SYS_FAULT	F12		

Dimensions for the 12 mm × 12 mm LFCSP_VQ package in Figure 72 are shown in millimeters.

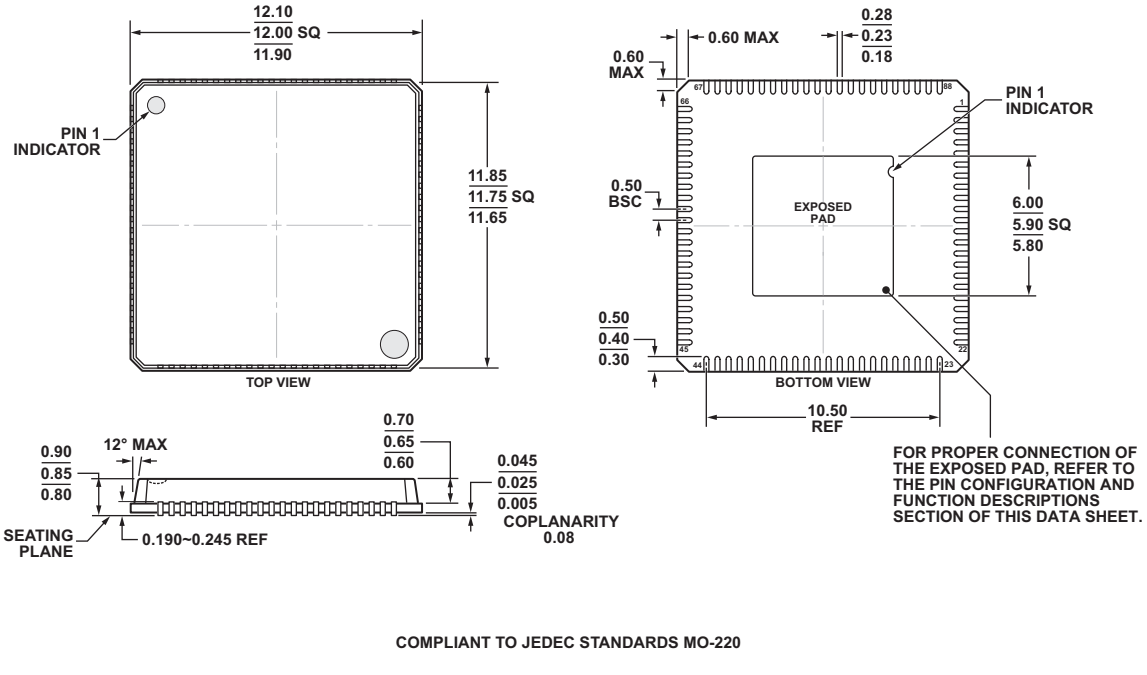

Figure 72. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
(CP-88-8)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 71 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 71. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-184-1	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter