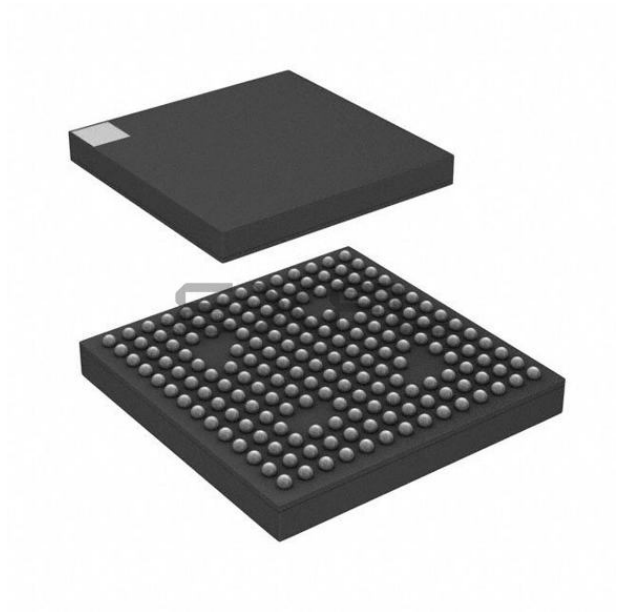

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	1MB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf707wcbcz311

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system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even L3 memories (DDR2, LPDDR). The processor features two CRC engines which are embedded in the memory-to-memory DMA controllers. CRC checksums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Memory Protection

The Blackfin+ core features a memory protection concept, which grants data and/or instruction accesses to enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

The system protection unit (SPU) guards against accidental or unwanted access to the MMR space of a peripheral by providing a write-protection mechanism. The user is able to choose and configure the peripherals that are protected as well as configure which ones of the four system MMR masters (core, memory DMA, the SPI host port, and Coresight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write-protection functionality, the SPU is employed to define which resources in the system are secure or non-secure and to block access to secure resources from non-secure masters.

Synonymously, the system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are two SMPU units in the ADSP-BF70x processors. One is for the L2 memory and the other is for the external DDR memory.

The SMPU is also part of the security infrastructure. It allows the user to not only protect against arbitrary read and/or write transactions, but it also allows regions of memory to be defined as secure and prevent non-secure masters from accessing those memory regions.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or the core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the fault management unit of the SEC.

Watchdog

The on-chip software watchdog timer can supervise the Blackfin+ core.

Bandwidth Monitor

Memory-to-memory DMA channels are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the GP counter can flag this to the processor or to the fault management unit of the SEC.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a fault. Additionally, the system events can be defined as an interrupt to the core. If defined as such, the SEC forwards the event to the fault management unit, which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken through a keyed sequence, to provide a final chance for the Blackfin+ core to resolve the issue and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core through several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processor contains high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not previously described.

Timers

The processor includes several timers which are described in the following sections.

Table 3. Clock Dividers

Clock Source	Divider (if Available on SYS_CLKOUT)
CCLK (Core Clock)	By 16
SYSCLK (System Clock)	By 8
SCLK0 (System Clock, All Peripherals not Covered by SCLK1)	Not available on SYS_CLKOUT
SCLK1 (System Clock for Crypto Engines and MDMA)	By 8
DCLK (LPDDR/DDR2 Clock)	By 8
OCLK (Output Clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports multiple power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
OTP Memory	V_{DD_OTP}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
All Other I/O (Includes SYS, JTAG, and Ports Pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

See Table 5 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core and to all of the peripherals. This setting signals the external voltage regulator supplying the VDD_INT pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation.

Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a nonvolatile storage device (or self-refreshed DRAM) prior to removing power if the processor state is to be preserved.

Because the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or the core and is the result of a hardware- or software-triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with the core being ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when the core is reset (programs must ensure that there is no pending system activity involving the core when it is being reset).

From a system perspective, reset is defined by both the reset target and the reset source described as follows in the following list.

Target defined:

- Hardware Reset—All functional units are set to their default states without exception. History is lost.
- System Reset—All functional units except the RCU are set to their default states.
- Core-only Reset—Affects the core only. The system software should guarantee that the core, while in reset state, is not accessed by any bus master.

Source defined:

- Hardware Reset—The $\overline{\text{SYS\_HWRST}}$ input signal is asserted active (pulled down).
- System Reset—May be triggered by software (writing to the RCU_CTL register) or by another functional unit such as the dynamic power management (DPM) unit (hibernate) or any of the system event controller (SEC), trigger routing unit (TRU), or emulator inputs.
- Core-only Reset—Triggered by software.
- Trigger request (peripheral).

Voltage Regulation

The processor requires an external voltage regulator to power the VDD_INT pins. To reduce standby power consumption, the external voltage regulator can be signaled through SYS_EXTWAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, all external supply pins (VDD_EXT, VDD_USB, and VDD_DMC) can still be powered, eliminating the need for external buffers. The external voltage regulator can be activated from this power down state by asserting the $\overline{\text{SYS\_HWRST}}$ pin, which then initiates a boot sequence. SYS_EXTWAKE indicates a wake-up to the external voltage regulator.

SYSTEM DEBUG

The processor includes various features that allow for easy system debug. These are described in the following sections.

System Watchpoint Unit

The system watchpoint unit (SWU) is a single module which connects to a single system bus and provides for transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently, but share common event (interrupt, trigger, and others) outputs.

Debug Access Port

The debug access port (DAP) provides IEEE-1149.1 JTAG interface support through its JTAG debug and serial wire debug port (SWJ-DP). SWJ-DP is a combined JTAG-DP and SW-DP that enables either serial wire debug (SWD) or a JTAG emulator to be connected to a target. SWD signals share the same pins as JTAG. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to MIPI System Trace Protocol version 2 (STPv2).

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (CrossCore® Embedded Studio), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information, visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE, a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

ADSP-BF706 EZ-KIT Mini

The ADSP-BF706 EZ-KIT Mini™ product (ADZS-BF706-EZMini) contains the ADSP-BF706 processor and is shipped with all of the necessary hardware. Users can start their evaluation immediately. The EZ-KIT Mini product includes the standalone evaluation board and USB cable. The EZ-KIT Mini ships with an on-board debug agent.

The evaluation board is designed to be used in conjunction with the CrossCore Embedded Studio (CCES) development tools to test capabilities of the ADSP-BF706 Blackfin processor.

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Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_12
SMC0_D13	SMC0 Data 13	B	PB_13
SMC0_D14	SMC0 Data 14	B	PB_14
SMC0_D15	SMC0 Data 15	B	PB_15
SPI0_CLK	SPI0 Clock	B	PB_00
SPI0_CLK	SPI0 Clock	C	PC_04
SPI0_D2	SPI0 Data 2	B	PB_03
SPI0_D2	SPI0 Data 2	C	PC_08
SPI0_D3	SPI0 Data 3	B	PB_07
SPI0_D3	SPI0 Data 3	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	B	PB_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_06
SPI0_MOSI	SPI0 Master Out, Slave In	B	PB_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_07
SPI0_RDY	SPI0 Ready	A	PA_06
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	A	PA_05
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	A	PA_06
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	B	PB_04
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	B	PB_05
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	B	PB_06
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	A	PA_05
SPI1_CLK	SPI1 Clock	A	PA_00
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_01
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_02
SPI1_RDY	SPI1 Ready	A	PA_03
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	A	PA_04
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	A	PA_03
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	C	PC_10
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	A	PA_14
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	A	PA_04
SPI2_CLK	SPI2 Clock	B	PB_10
SPI2_D2	SPI2 Data 2	B	PB_13
SPI2_D3	SPI2 Data 3	B	PB_14
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_11
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_12
SPI2_RDY	SPI2 Ready	A	PA_04
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	B	PB_15
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	B	PB_08
$\overline{\text{SPI2\_SEL3}}$	SPI2 Slave Select Output 3	B	PB_09
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	B	PB_15
SPT0_ACLK	SPORT0 Channel A Clock	A	PA_13
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	A	PA_14
SPT0_AD0	SPORT0 Channel A Data 0	C	PC_08
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_00

Table 14. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	$\overline{\text{UART1\_TX}}$	SPT0_AD1	PPI0_D15		
PC_01	$\overline{\text{UART1\_RX}}$	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	$\overline{\text{UART0\_RTS}}$	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	$\overline{\text{UART0\_CTS}}$	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	$\overline{\text{SPI1\_SEL3}}$		TM0_ACLK1

ADSP-BF70x DESIGNER QUICK REFERENCE

Table 15 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Pin Type: The Type column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (none), I/O (input/output), a (analog), s (supply), and g (ground).
- Driver Type: The Driver Type column in the table identifies the driver type used by the pin. The driver types are defined in the output drive currents section of this data sheet.
- Internal Termination: The Int Term column in the table specifies the termination present when the processor is not in the reset or hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Termination: The Reset Term column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Drive: The Reset Drive column in the table specifies the active drive on the signal when the processor is in the reset state.
- Hibernate Termination: The Hiber Term column in the table specifies the termination present when the processor is in the hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Hibernate Drive: The Hiber Drive column in the table specifies the active drive on the signal when the processor is in the hibernate state.
- Power Domain: The Power Domain column in the table specifies the power supply domain in which the signal resides.
- Description and Notes: The Description and Notes column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

If an external pull-up or pull-down resistor is required for any signal, 100 kΩ is the maximum value that can be used unless otherwise noted.

Note that for Port A, Port B, and Port C (PA_00 to PC_14), when $\overline{\text{SYS\_HWRST}}$ is low, these pads are three-state. After $\overline{\text{SYS\_HWRST}}$ is released, but before code execution begins, these pins are internally pulled up. Subsequently, the state depends on the input enable and output enable which are controlled by software.

Software control of internal pull-ups works according to the following settings in the PADS_PCFG0 register. When PADS_PCFG0 = 0: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled when both the input enable and output enable of a particular pin are deasserted. When PADS_PCFG0 = 1: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled as long as the output enable of a particular pin is deasserted.

There are some exceptions to this scheme:

- Internal pull-ups are always disabled if MSI mode is selected for that signal.
- The following signals enabled the internal pull-down when the output enable is de-asserted: $\overline{\text{SMC0\_AMS}}[1:0]$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, $\overline{\text{SMC0\_AOE}}$, SMC0_ARDY, $\overline{\text{SPI0\_SEL}}[6:1]$, $\overline{\text{SPI1\_SEL}}[4:1]$, and $\overline{\text{SPI2\_SEL}}[3:1]$.

Table 15. ADSP-BF70x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 0 Notes: No notes.
DMC0_A01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 1 Notes: No notes.
DMC0_A02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 2 Notes: No notes.
DMC0_A03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 3 Notes: No notes.
DMC0_A04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 4 Notes: No notes.
DMC0_A05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 5 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_DQ08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 8 Notes: No notes.
DMC0_DQ09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 9 Notes: No notes.
DMC0_DQ10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 10 Notes: No notes.
DMC0_DQ11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes.
DMC0_DQ12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes.
DMC0_DQ13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes.
DMC0_DQ14	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes.
DMC0_DQ15	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes.
DMC0_LDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes.
DMC0_LDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: For LPDDR, a pull-down is required.
$\overline{\text{DMC0\_LDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: For single ended DDR2, connect to DMC0_VREF. For LPDDR, leave unconnected.
DMC0_ODT	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 On-die termination Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_RAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes.
DMC0_UDM	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes.
DMC0_UDQS	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: For LPDDR, a pull-down is required.
$\overline{\text{DMC0\_UDQS}}$	I/O	C	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: For single ended DDR2, connect to DMC0_VREF. For LPDDR, leave unconnected.
DMC0_VREF	a	na	none	none	none	none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: For LPDDR, leave unconnected. If the DMC is not used, connect to ground.
$\overline{\text{DMC0\_WE}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes.
GND	g	na	none	none	none	none	none	na	Desc: Ground Notes: No notes.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 and Table 18 describe the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Core and System Clock Operating Conditions

Parameter		Ratio Restriction	PLLCLK Restriction	Min	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	PLLCLK = 800		400	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	600 ≤ PLLCLK < 800		390	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	380 ≤ PLLCLK < 600		380	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	230.2 ≤ PLLCLK < 380		PLLCLK	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		PLLCLK = 800	60	200	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		600 ≤ PLLCLK < 800	60	195	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		380 ≤ PLLCLK < 600	60	190	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		230.2 ≤ PLLCLK < 380	60	PLLCLK ÷ 2	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$		30	100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2 Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		125	200	MHz
f_{DCLK}	LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		10	200	MHz

[1] The minimum frequency for SYSCLK and SCLK0 applies only when the USB is used.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
I_{OZH_TWI}[14]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 5.5 V			10	µA
ADSP-BF701/703/705/707 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.2	6.0	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.9	7.4	pF
C_{IN_DDR}[16]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.1	6.9	pF
ADSP-BF700/702/704/706 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.0	5.3	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.8	7.4	pF
$I_{DD\_DEEPSLEEP}$[17, 18]	V_{DD_INT} Current in Deep Sleep Mode	Clocks disabled T_J = 25°C		1.4		mA
I_{DD_IDLE}[18]	V_{DD_INT} Current in Idle	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 0.05 (idle) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		13		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 800 MHz f_{CCLK} = 400 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		90		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 300 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		66		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 400 MHz f_{CCLK} = 200 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		49		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		30		mA

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0		33		µA
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current Without USB	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0, USB protection disabled (USB_PHY_CTLDIS = 1)		15		µA
I_{DD_INT}[18]	V_{DD_INT} Current	V_{DD_INT} within operating conditions table specifications			See I_{DDINT_TOT} equation on on Page 56	mA
I_{DD_RTC}	I_{DD_RTC} Current	V_{DD_RTC} = 3.3 V, T_J = 125°C			10	µA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals, and USB0 signals.

[2] Applies to DMC0_Axx, DMC0_CAS, DMC0_CKE, DMC0_CK, DMC0_CK, DMC0_CS, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, DMC0_LDQS, DMC0_ODT, DMC0_RAS, DMC0_UDM, DMC0_UDQS, DMC0_UDQS, and DMC0_WE signals.

[3] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.

[4] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TDI, and JTG_TMS_SWDIO signals.

[5] Applies to DMC0_VREF signal.

[6] Applies to JTG_TCK_SWCLK and JTG_TRST signals.

[7] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TCK, and JTG_TRST signals.

[8] Applies to JTG_TDI, JTG_TMS_SWDIO, PA_xx, PB_xx, and PC_xx signals when internal GPIO pull-ups are enabled. For information on when internal pull-ups are enabled for GPIOs. See ADSP-BF70x Designer Quick Reference on Page 38.

[9] Applies to USB0_CLKIN signal.

[10] Applies to PA_xx, PB_xx, PC_xx, SMC0_AMS0, SMC0_ARE, SMC0_AWE, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, and USB0_VBC signals.

[11] Applies to DMC0_Axx, DMC0_BAxx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, and DMC0_WE signals.

[12] Applies to PA_xx, PB_xx, PC_xx, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_Axx, DMC0_BAx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, DMC0_WE, and TWI signals.

[13] Applies to USB0_VBUS signals.

[14] Applies to all TWI signals.

[15] Applies to all signals, except DMC0 and TWI signals.

[16] Applies to all DMC0 signals.

[17] See the *ADSP-BF70x Blackfin+ Processor Hardware Reference* for definition of deep sleep and hibernate operating modes.

[18] Additional information can be found at Total Internal Power Dissipation.

[19] Applies to VDD_EXT, VDD_DMC, and VDD_USB supply signals only. Clock inputs are tied high or low.

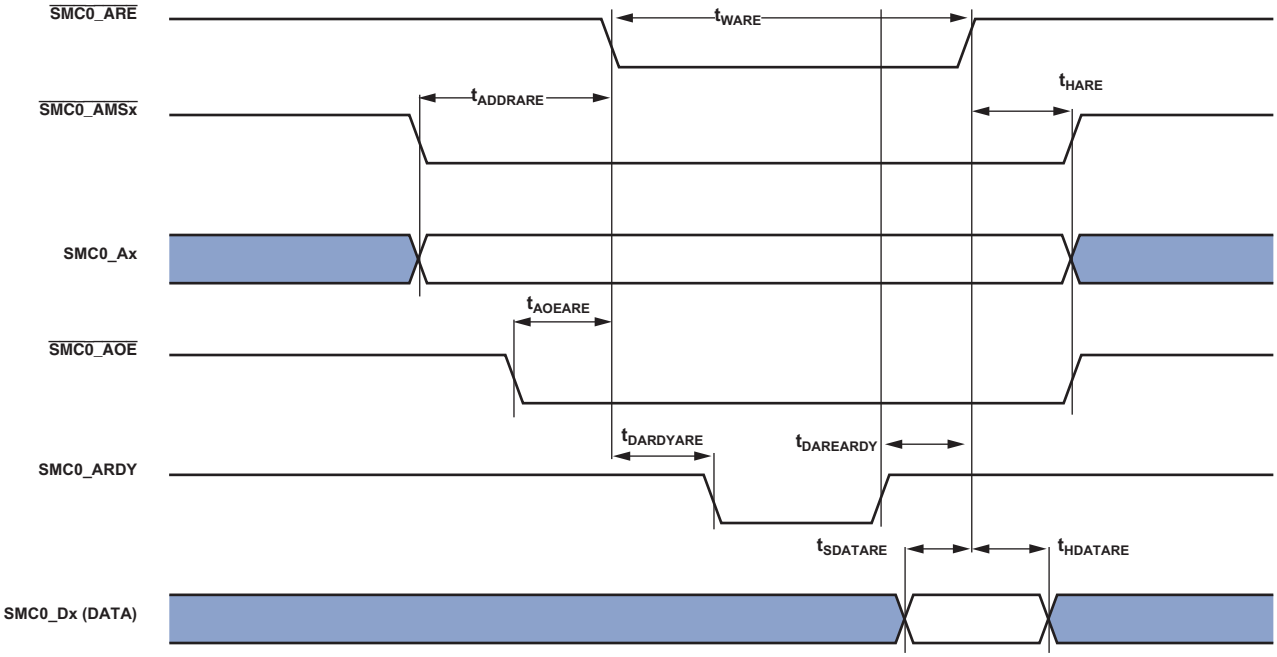

Figure 10. Asynchronous Read

Asynchronous Write

Table 35 and Figure 14 show asynchronous memory write timing, related to the static memory controller (SMC).

Table 35. Asynchronous Memory Write (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{SMC0\_AWE}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics						
t_{ENDAT}	DATA Enable After $\overline{SMC0\_AMSx}$ Assertion	–3		–2		ns
t_{DDAT}	DATA Disable After $\overline{SMC0\_AMSx}$ Deassertion		4.5		4	ns
t_{AMSAWE}	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_AWE}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		(PREST + WST + PREAT) × t_{SCLK0} – 4		ns
t_{HAWE}	Output[4] Hold After $\overline{SMC0\_AWE}$ High[5]	WHT × t_{SCLK0}		WHT × t_{SCLK0}		ns
t_{WAWE}[6]	$\overline{SMC0\_AWE}$ Active Low Width[6]	WAT × t_{SCLK0} – 2		WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{SMC0\_AWE}$ High Delay After SMC0_ARDY Assertion		3.5 × t_{SCLK0} + 17.5		3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{SMC0\_AMSx}$, $\overline{SMC0\_ABEx}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

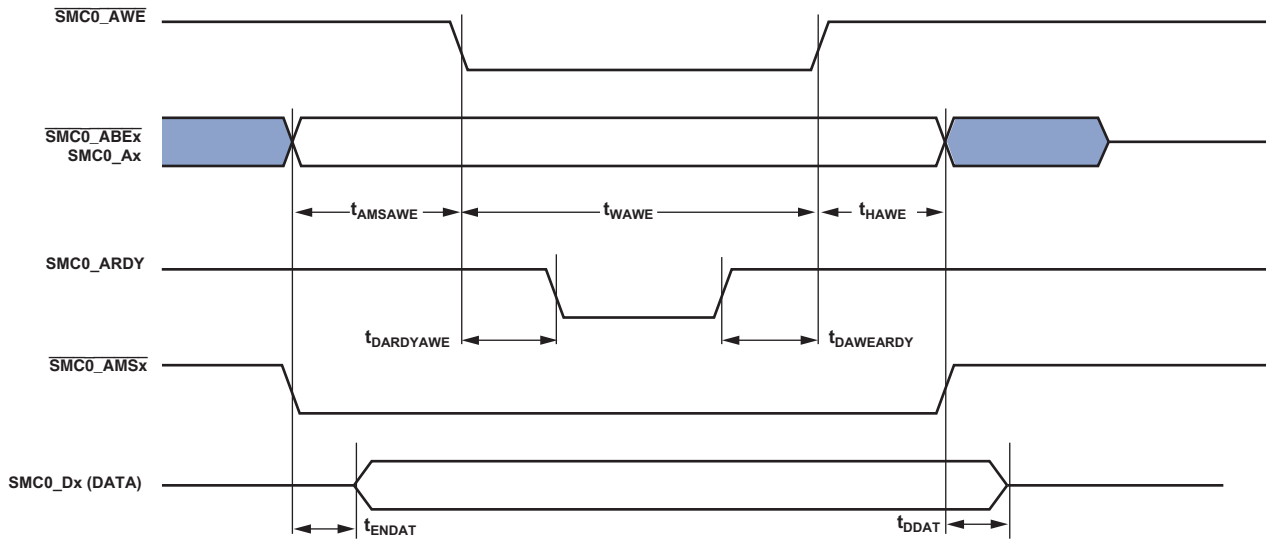

Figure 14. Asynchronous Write

SMC Write Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example WST = 0x2, WAT = 0x2, and WHT = 0x1.

Table 36. SMC Write Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		ns
Switching Characteristics				
t_{DDAT}	SMC0_Dx Disable After SYS_CLKOUT		7	ns
t_{ENDAT}	SMC0_Dx Enable After SYS_CLKOUT	–2.5		ns
t_{DO}	Output Delay After SYS_CLKOUT[1]		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		ns

[1] Output pins/balls include $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$, SMC0_Ax, SMC0_Dx, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_AWE}}$.

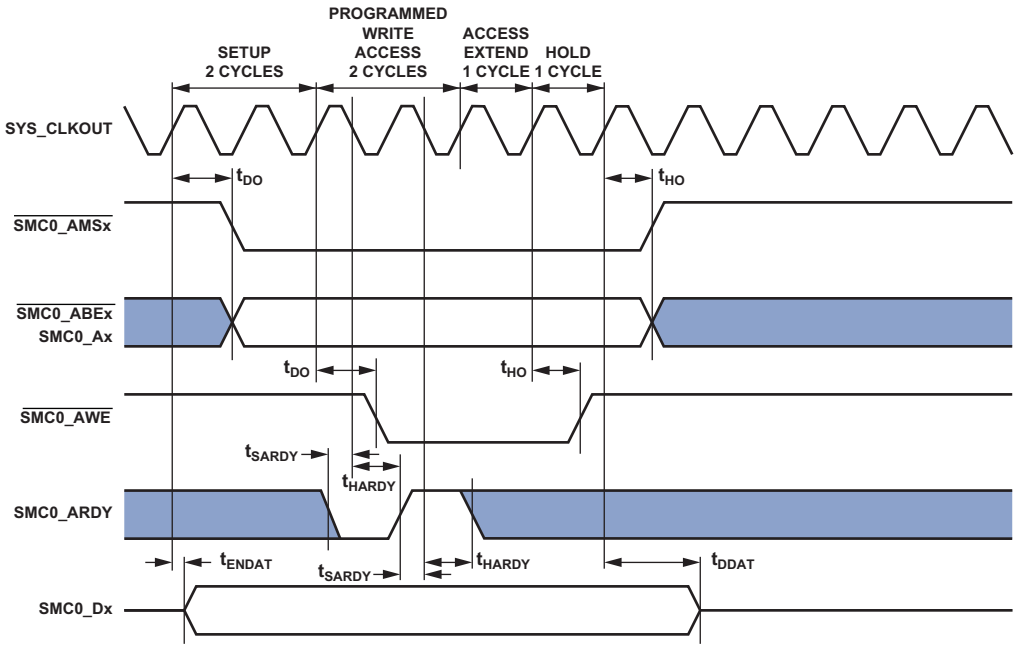

Figure 15. SMC Write Cycle Timing With Reference to SYS_CLKOUT Timing

General-Purpose I/O Port Timing (GPIO)

Table 45 and Figure 23 describe I/O timing, related to the general-purpose ports (PORT).

Table 45. General-Purpose I/O Port Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

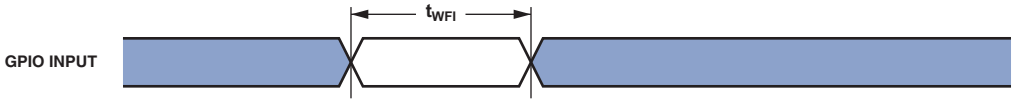

Figure 23. General-Purpose I/O Port Timing

Timer Cycle Timing

Table 46 and Figure 24 describe timer expired operations, related to the general-purpose timer (TIMER). The input signal is asynchronous in width capture mode and external clock mode and has an ideal maximum input frequency of (f_{SCLK0}/4) MHz. The Period Value (VALUE) is the timer period assigned in the TMx_TMRn_PER register and can range from 2 to $2^{32} - 1$.

Table 46. Timer Cycle Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	Max	V_{DD_EXT} 3.3 V Nominal Min	Max	Unit
Timing Requirements						
t_{WL}	Timer Pulse Width Input Low[1]	$2 \times t_{SCLK0} - 1.5$		$2 \times t_{SCLK0} - 1.5$		ns
t_{WH}	Timer Pulse Width Input High[1]	$2 \times t_{SCLK0} - 1.5$		$2 \times t_{SCLK0} - 1.5$		ns
Switching Characteristic						
t_{HTO}	Timer Pulse Width Output	$t_{SCLK0} \times VALUE - 1$		$t_{SCLK0} \times VALUE - 1$		ns

[1] This specification indicates the minimum instantaneous width that can be tolerated due to duty cycle variation or jitter for TMx signals in width capture and external clock modes. The ideal maximum frequency for TMx signals is listed in Timer Cycle Timing on this page.

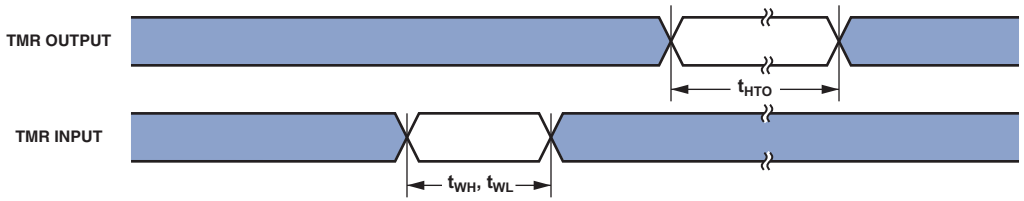

Figure 24. Timer Cycle Timing

Up/Down Counter/Rotary Encoder Timing

Table 47 and Figure 25 describe timing, related to the general-purpose counter (CNT).

Table 47. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

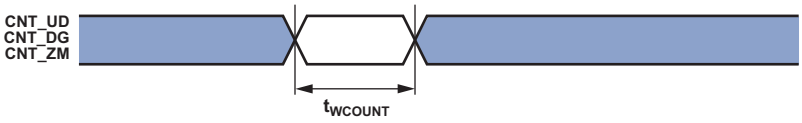

Figure 25. Up/Down Counter/Rotary Encoder Timing

Serial Ports

To determine whether serial port (SPORT) communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SPT_CLK) width. In Figure 27 either the rising edge or the falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65,535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK0}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 49. Serial Ports—External Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[1]	1.5		1		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[1]	3		3		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	1.5		1		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	3		3		ns
t_{SCLKW}	SPT_CLK Width[2]	$(0.5 \times t_{SPTCLKEXT}) - 1$		$(0.5 \times t_{SPTCLKEXT}) - 1$		ns
$t_{SPTCLKE}$	SPT_CLK Period[2]	$t_{SPTCLKEXT} - 1$		$t_{SPTCLKEXT} - 1$		ns
Switching Characteristics						
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[3]		18		15	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[3]	2.5		2.5		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		18		15	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	2.5		2.5		ns

[1] Referenced to sample edge.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK. For the external SPT_CLK ideal maximum frequency, see the $f_{SPTCLKEXT}$ specification in Table 18 on Page 52 in Clock Related Operating Conditions.

[3] Referenced to drive edge.

Table 53. Serial Ports—External Late Frame Sync

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0[1]		19		15.5	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as standard serial mode, and MCE = 1, MFD = 0.

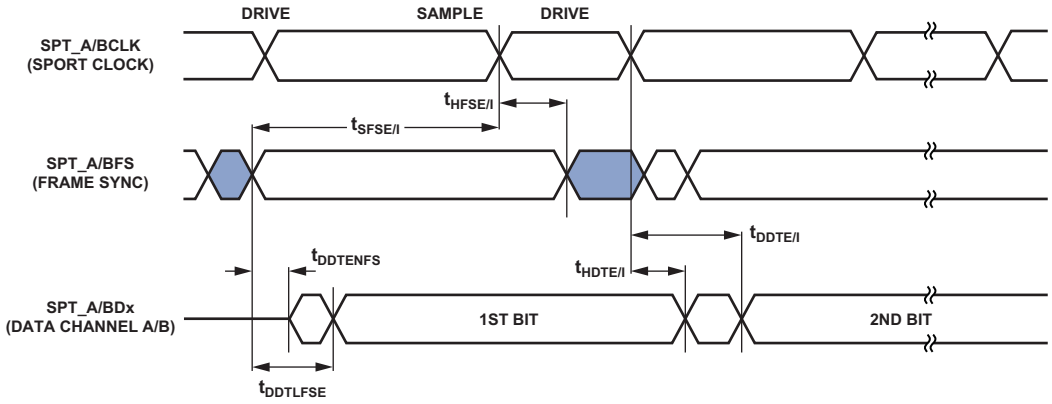

Figure 30. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

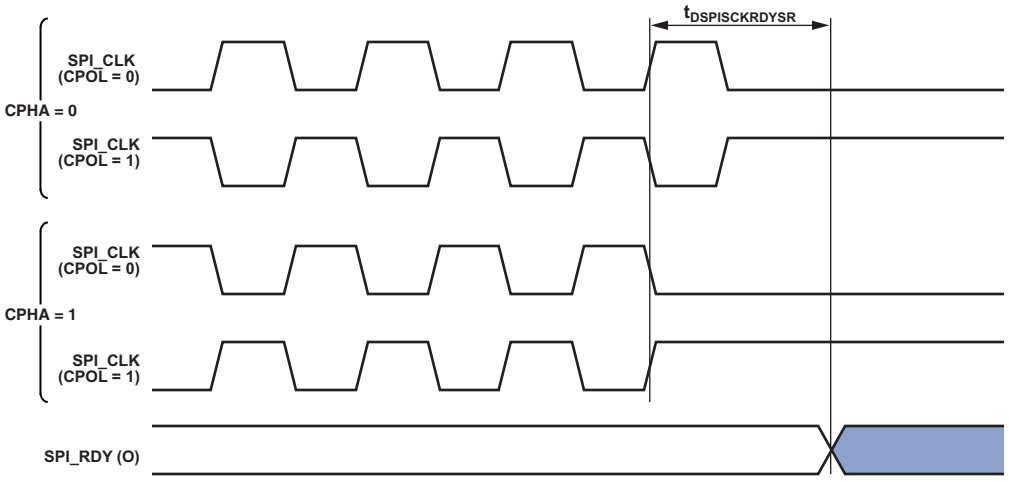

Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

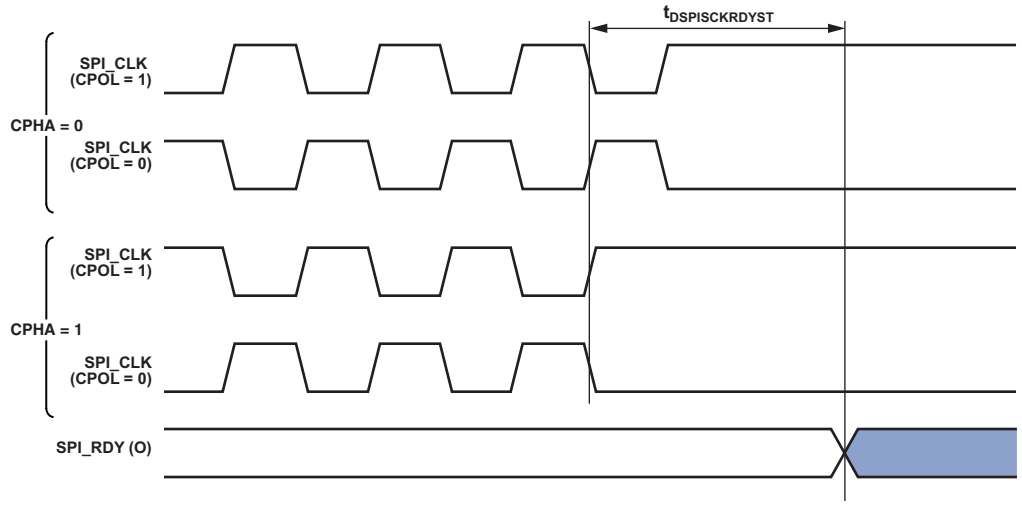

Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)