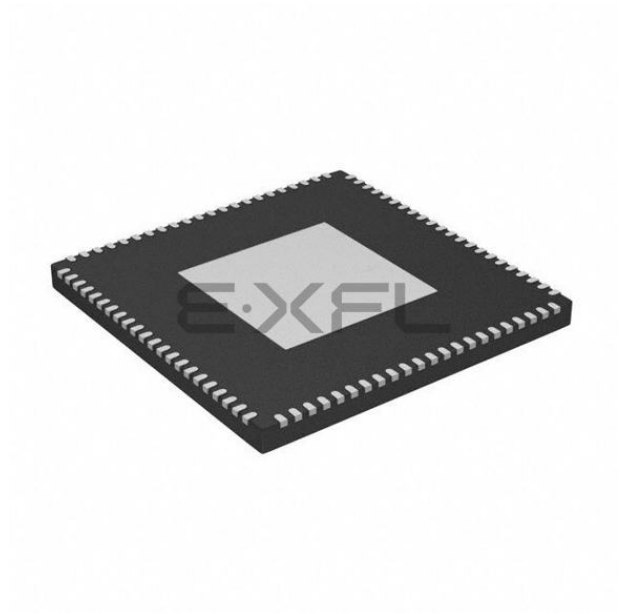

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	100MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	128kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf700kcpz-1

Table 3. Clock Dividers

Clock Source	Divider (if Available on SYS_CLKOUT)
CCLK (Core Clock)	By 16
SYSCLK (System Clock)	By 8
SCLK0 (System Clock, All Peripherals not Covered by SCLK1)	Not available on SYS_CLKOUT
SCLK1 (System Clock for Crypto Engines and MDMA)	By 8
DCLK (LPDDR/DDR2 Clock)	By 8
OCLK (Output Clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports multiple power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
OTP Memory	V_{DD_OTP}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
All Other I/O (Includes SYS, JTAG, and Ports Pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

See Table 5 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core and to all of the peripherals. This setting signals the external voltage regulator supplying the VDD_INT pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation.

Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a nonvolatile storage device (or self-refreshed DRAM) prior to removing power if the processor state is to be preserved.

Because the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or the core and is the result of a hardware- or software-triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with the core being ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when the core is reset (programs must ensure that there is no pending system activity involving the core when it is being reset).

From a system perspective, reset is defined by both the reset target and the reset source described as follows in the following list.

184-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_BA0	DMC0 Bank Address Input 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address Input 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address Input 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
$\overline{\text{DMC0\_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
$\overline{\text{MSI0\_INT}}$	MSI0 eSDIO Interrupt Input	C	PC_14
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_14	Position 00 through Position 14	C	PC_00-PC_14
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input/external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_AFS	SPORT0 Channel A Frame Sync	A	PA_12
SPT0_AFS	SPORT0 Channel A Frame Sync	C	PC_05
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	A	PA_15
SPT0_BCLK	SPORT0 Channel B Clock	B	PB_04
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_04
SPT0_BD0	SPORT0 Channel B Data 0	B	PB_05
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_06
SPT0_BD1	SPORT0 Channel B Data 1	B	PB_07
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_01
SPT0_BFS	SPORT0 Channel B Frame Sync	B	PB_06
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_07
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	A	PA_15
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_08
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_10
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_11
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_09
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	A	PA_07
SPT1_BCLK	SPORT1 Channel B Clock	B	PB_00
SPT1_BCLK	SPORT1 Channel B Clock	C	PC_10
SPT1_BD0	SPORT1 Channel B Data 0	B	PB_02
SPT1_BD1	SPORT1 Channel B Data 1	B	PB_03
SPT1_BFS	SPORT1 Channel B Frame Sync	B	PB_01
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	A	PA_07
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_EXTWAKE	External Wake Control	Not Muxed	SYS_EXTWAKE
$\overline{\text{SYS\_FAULT}}$	Active-Low Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Non-maskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04

Table 14. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	$\overline{\text{UART1\_TX}}$	SPT0_AD1	PPI0_D15		
PC_01	$\overline{\text{UART1\_RX}}$	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	$\overline{\text{UART0\_RTS}}$	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	$\overline{\text{UART0\_CTS}}$	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	$\overline{\text{SPI1\_SEL3}}$		TM0_ACLK1

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master Out, Slave In | TRACE0 Trace Data 5 | SMC0 Memory Select 1 Notes: May require a pull-up if used as an SMC memory select. Check the data sheet requirements of the IC it connects to.
PA_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 2 | SPI1 Ready | SMC0 Asynchronous Ready Notes: May require a pull-up or pull-down if used as an SMC asynchronous ready. Check the data sheet requirements of the IC it connects to and the programmed polarity.
PA_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 1 | TM0 Timer 7 | SPI2 Ready | SMC0 Address 8 | SPI1 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PA_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 0 | SPI0 Slave Select Output 1 | SMC0 Address 7 | SPI0 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PA_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 1 | SPI0 Slave Select Output 2 | SPI0 Ready | SMC0 Address 6 Notes: SPI slave select outputs require a pull-up when used.
PA_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 2 | SPT1 Channel B Transmit Data Valid | SPT1 Channel A Transmit Data Valid | SMC0 Address 5 | CNT0 Count Down and Gate Notes: No notes.
PA_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 11 | MSI0 Card Detect | SPT1 Channel A Clock | SMC0 Address 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PA_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 10 | TM0 Timer 4 | SPT1 Channel A Frame Sync | SMC0 Address 2 Notes: No notes.
PA_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 9 | TM0 Timer 5 | SPT1 Channel A Data 0 | SMC0 Address 3 Notes: No notes.
PA_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 8 | TM0 Timer 6 | SPT1 Channel A Data 1 | SMC0 Address 4 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master Out, Slave In | TRACE0 Trace Data 3 | SMC0 Data 12 | SYS Power Saving Mode Wakeup 2 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 2 | UART1 Request to Send | TRACE0 Trace Data 2 | SMC0 Data 13 Notes: No notes.
PB_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 3 | UART1 Clear to Send | TRACE0 Trace Data 1 | SMC0 Data 14 Notes: No notes.
PB_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Slave Select Output 1 | TRACE0 Trace Data 0 | SMC0 Data 15 | SPI2 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PC_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Transmit | SPT0 Channel A Data 1 | PPI0 Data 15 Notes: No notes.
PC_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Receive | SPT0 Channel B Data 1 | PPI0 Data 14 | SMC0 Address 9 | TM0 Alternate Capture Input 4 Notes: No notes.
PC_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Request to Send | CAN0 Receive | PPI0 Data 13 | SMC0 Address 10 | SYS Power Saving Mode Wakeup 3 | TM0 Alternate Capture Input 5 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PC_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Clear to Send | CAN0 Transmit | PPI0 Data 12 | SMC0 Address 11 | TM0 Alternate Capture Input 0 Notes: No notes.
PC_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Clock | SPI0 Clock | MSI0 Data 1 | SMC0 Address 12 | TM0 Alternate Clock 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input Notes: If USB is not used, connect to ground. Active during reset
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data – Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_ID	I/O	na	none	none	none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: If USB is not used connect to ground. When USB is being used, the internal pull-up that is present during hibernate is programmable. See the USB chapter in the HRM. Active during reset.
USB0_VBC	I/O	E	none	none	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: If USB is not, used pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: If USB is not used, connect to ground.
USB0_XTAL	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Crystal Notes: No notes.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD Notes: Must be powered.
VDD_HADC	s	na	none	none	none	none	none	na	Desc: VDD for HADC Notes: If HADC is not used, connect to ground.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD Notes: Must be powered.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 and Table 18 describe the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Core and System Clock Operating Conditions

Parameter		Ratio Restriction	PLLCLK Restriction	Min	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	PLLCLK = 800		400	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	600 ≤ PLLCLK < 800		390	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	380 ≤ PLLCLK < 600		380	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	230.2 ≤ PLLCLK < 380		PLLCLK	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		PLLCLK = 800	60	200	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		600 ≤ PLLCLK < 800	60	195	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		380 ≤ PLLCLK < 600	60	190	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		230.2 ≤ PLLCLK < 380	60	PLLCLK ÷ 2	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$		30	100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2 Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		125	200	MHz
f_{DCLK}	LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		10	200	MHz

[1] The minimum frequency for SYSCLK and SCLK0 applies only when the USB is used.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
I_{OZH_TWI}[14]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 5.5 V			10	µA
ADSP-BF701/703/705/707 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.2	6.0	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.9	7.4	pF
C_{IN_DDR}[16]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.1	6.9	pF
ADSP-BF700/702/704/706 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.0	5.3	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.8	7.4	pF
$I_{DD\_DEEPSLEEP}$[17, 18]	V_{DD_INT} Current in Deep Sleep Mode	Clocks disabled T_J = 25°C		1.4		mA
I_{DD_IDLE}[18]	V_{DD_INT} Current in Idle	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 0.05 (idle) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		13		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 800 MHz f_{CCLK} = 400 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		90		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 300 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		66		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 400 MHz f_{CCLK} = 200 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		49		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		30		mA

Power-Up Reset Timing

A power-up reset is required to place the processor in a known state after power-up. A power-up reset is initiated by asserting $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$. During power-up reset, all pins are high impedance except for those noted in the ADSP-BF70x Designer Quick Reference on Page 38.

Both $\overline{\text{JTG\_TRST}}$ and $\overline{\text{SYS\_HWRST}}$ need to be asserted upon power-up, but only $\overline{\text{SYS\_HWRST}}$ needs to be released for the device to boot properly. $\overline{\text{JTG\_TRST}}$ may be asserted indefinitely for normal operation. $\overline{\text{JTG\_TRST}}$ only needs to be released when using an emulator to connect to the DAP for debug or boundary scan. There is an internal pull-down on $\overline{\text{JTG\_TRST}}$ to ensure internal emulation logic will always be properly initialized during power-up reset.

Table 30 and Figure 9 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU). In Figure 9, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, and V_{DD_HADC}.

There is no power supply sequencing requirement for the ADSP-BF70x processor. However, if saving power during power-on is important, bringing up V_{DD_INT} last is recommended. This avoids a small current drain in the V_{DD_INT} domain during the transition period of I/O voltages from 0 V to within the voltage specification.

Table 30. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ Deasserted After V_{DD_INT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, V_{DD_HADC}, and SYS_CLKIN are Stable and Within Specification	$11 \times t_{CKIN}$		ns
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (No External Pull-Down on $\overline{\text{JTG\_TRST}}$)	10		µs
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (10k External Pull-Down on $\overline{\text{JTG\_TRST}}$)	1		µs

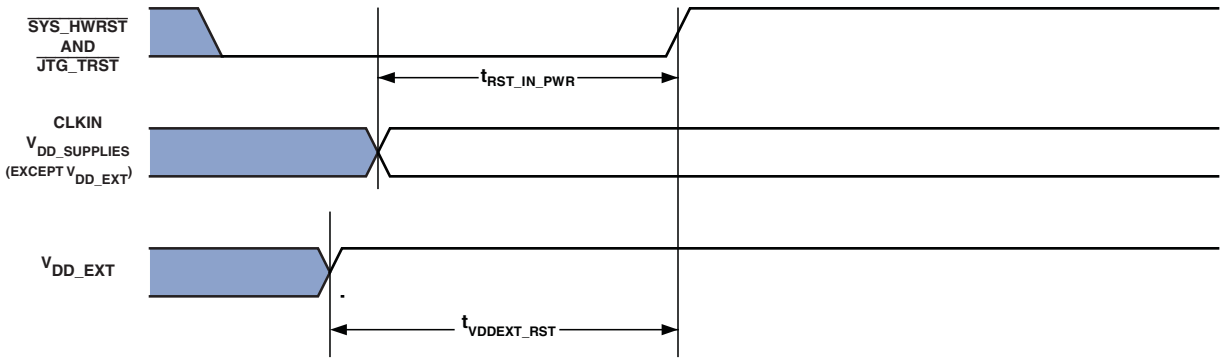

Figure 9. Power-Up Reset Timing

SMC Read Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example, RST = 0x2, RAT = 0x4, and RHT = 0x1.

Table 32. SMC Read Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SDAT}	SMC0_Dx Setup Before SYS_CLKOUT	5.3		4.3		ns
t_{HDAT}	SMC0_Dx Hold After SYS_CLKOUT	1.5		1.5		ns
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	16.6		14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		0.7		ns
Switching Characteristics						
t_{DO}	Output Delay After SYS_CLKOUT[1]		7		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		–2.5		ns

[1] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_ABEx}}$.

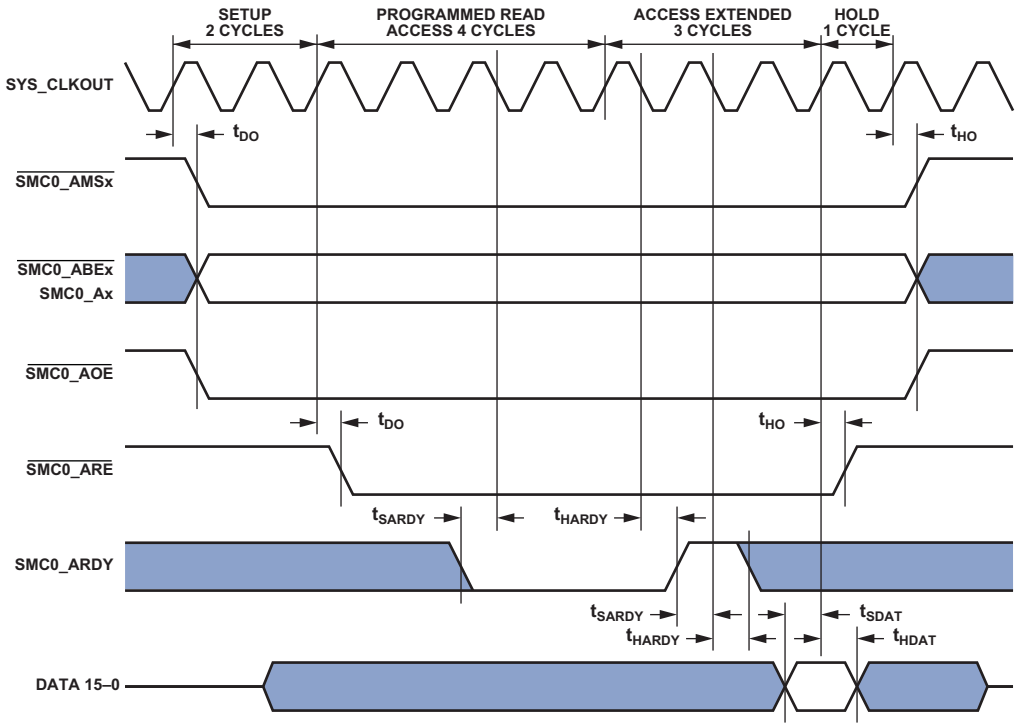

Figure 11. Asynchronous Memory Read Cycle Timing

DDR2 SDRAM Write Cycle Timing

Table 41 and Figure 19 show DDR2 SDRAM write cycle timing, related to the dynamic memory controller (DMC).

Table 41. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1] Min	200 MHz[1] Max	Unit
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	–0.25	+0.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.15		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.275		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Output High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Output Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

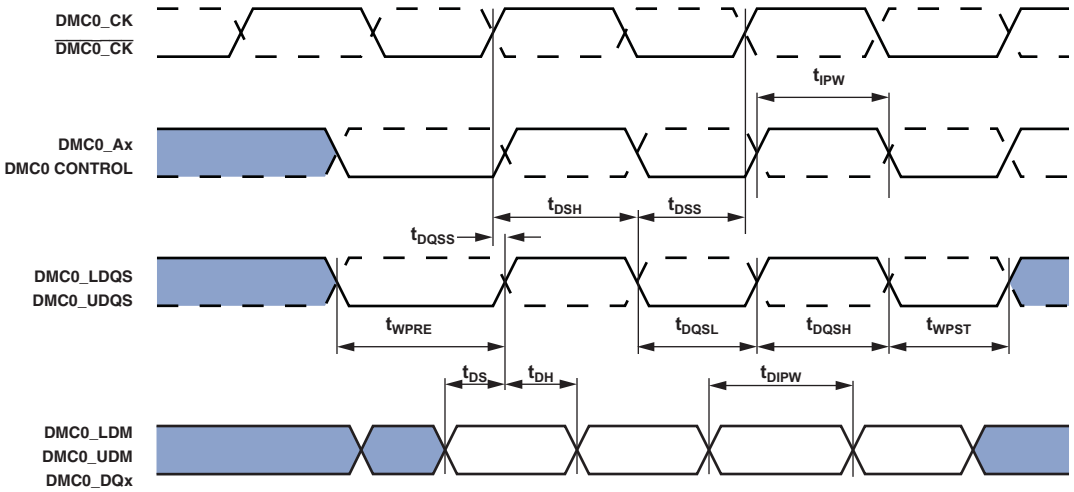

Figure 19. DDR2 SDRAM Controller Output AC Timing

Mobile DDR SDRAM Read Cycle Timing

Table 43 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 43. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz		Unit
		Min	Max	
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.5		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.7	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

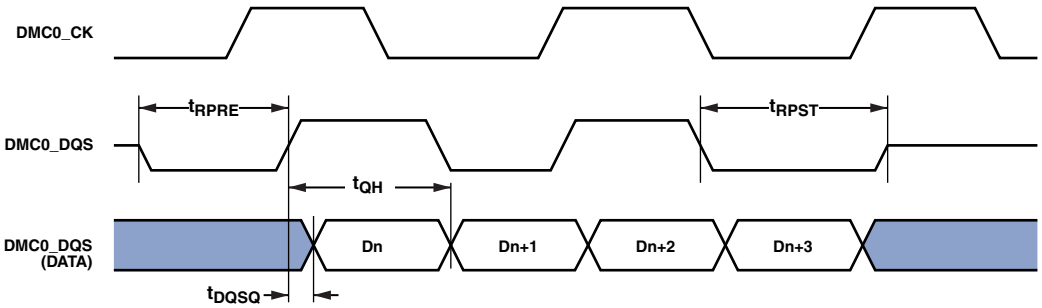

Figure 21. Mobile DDR SDRAM Controller Input AC Timing

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

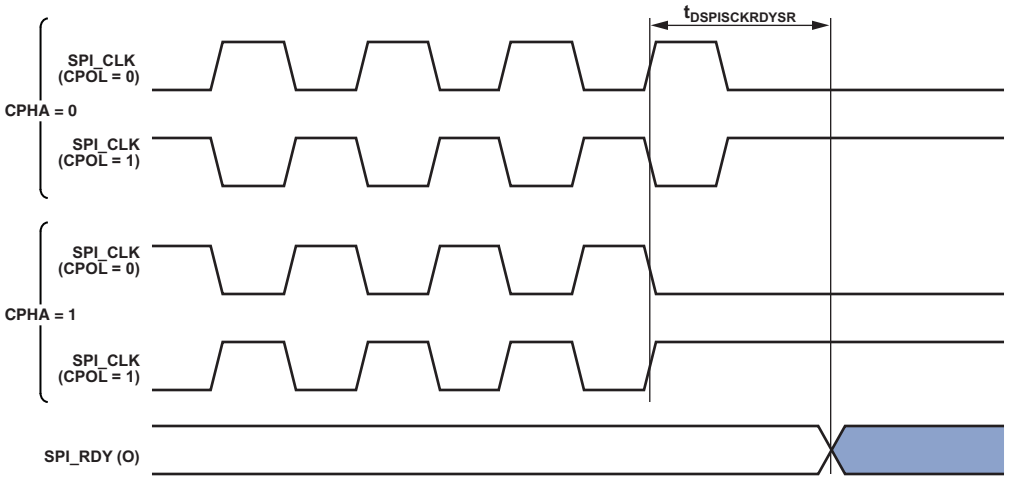

Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

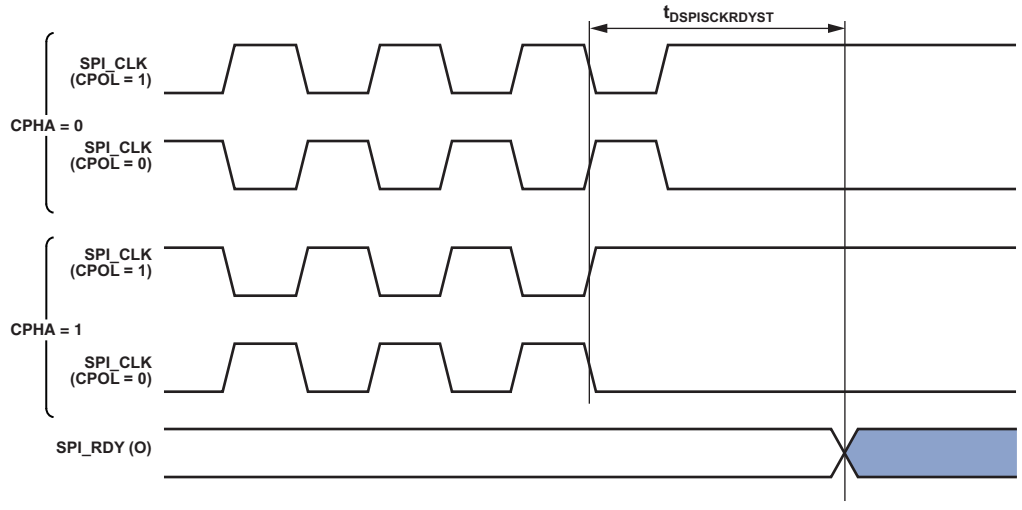

Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

Table 61. Enhanced Parallel Peripheral Interface—External Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{PCLKW}	EPPI_CLK Width[1]	$(0.5 \times t_{PCLKEXT}) - 1$		$(0.5 \times t_{PCLKEXT}) - 1$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKEXT} - 1$		$t_{PCLKEXT} - 1$		ns
t_{SFSPE}	External FS Setup Before EPPI_CLK	1.5		1		ns
t_{HFSPE}	External FS Hold After EPPI_CLK	3.3		3		ns
t_{SDRPE}	Receive Data Setup Before EPPI_CLK	1		1		ns
t_{HDRPE}	Receive Data Hold After EPPI_CLK	3		3		ns
Switching Characteristics						
t_{DFSPE}	Internal FS Delay After EPPI_CLK		17.5		14.5	ns
t_{HOFSPE}	Internal FS Hold After EPPI_CLK	2.5		2.5		ns
t_{DDTPE}	Transmit Data Delay After EPPI_CLK		17.5		14.5	ns
t_{HDTPE}	Transmit Data Hold After EPPI_CLK	2.5		2.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external EPPI_CLK. For the external EPPI_CLK ideal maximum frequency, see the $f_{PCLKEXT}$ specification in Table 18 on Page 52 in Clock Related Operating Conditions.

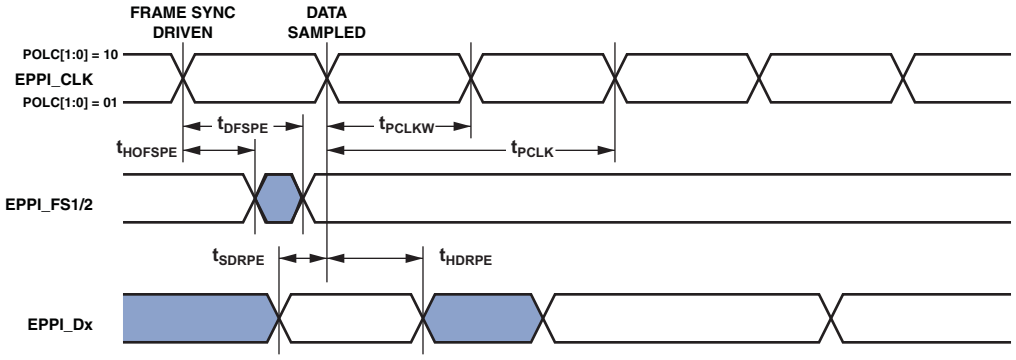

Figure 45. PPI External Clock GP Receive Mode with Internal Frame Sync Timing

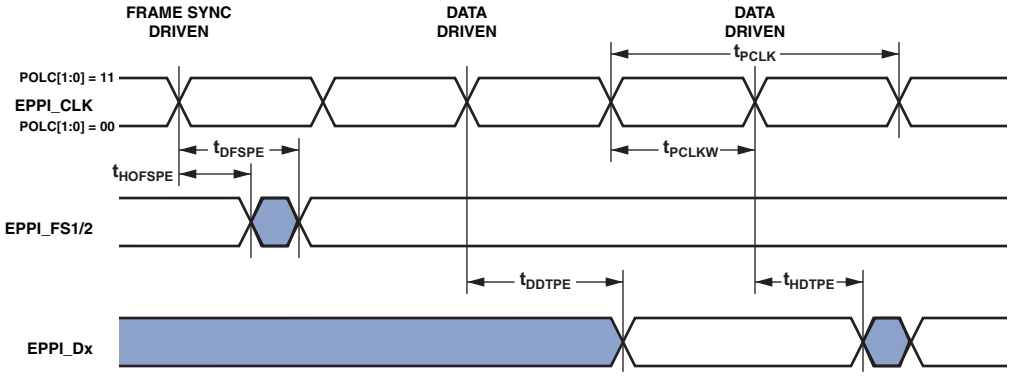

Figure 46. PPI External Clock GP Transmit Mode with Internal Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The universal asynchronous receiver-transmitter (UART) ports receive and transmit operations are described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Controller Area Network (CAN) Interface

The controller area network (CAN) interface timing is described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 62 describes the universal serial bus (USB) on-the-go receive and transmit operations.

Table 62. USB On-The-Go—Receive and Transmit Timing

		V_{DD_USB} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{USBS}	USB_XI Frequency	24	24	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

Mobile Storage Interface (MSI) Controller Timing

Table 64 and Figure 49 show I/O timing, related to the mobile storage interface (MSI).

The MSI timing depends on the period of the input clock that has been routed to the MSI peripheral ($t_{MSICLKIN}$) by setting the MSI0_UHS_EXT register. See Table 63 for this information.

Table 63. $t_{MSICLKIN}$ Settings

EXT_CLK_MUX_CTRL[31:30]	$t_{MSICLKIN}$
00	$t_{SCLK0} \times 2$
01	t_{SCLK0}
10	$t_{SCLK1} \times 3$

$$t_{MSICLKIN} = \frac{1}{f_{MSICLKIN}}$$

($f_{MSICLKPROG}$) frequency in MHz is set by the following equation where DIV0 is a field in the MSI_CLKDIV register that can be set from 0 to 255. When DIV0 is set between 1 and 255, the following equation is used to determine $f_{MSICLKPROG}$:

$$f_{MSICLKPROG} = \frac{f_{MSICLKIN}}{DIV0 \times 2}$$

When DIV0 = 0,

$$f_{MSICLKPROG} = f_{MSICLKIN}$$

Also note the following:

$$t_{MSICLKPROG} = \frac{1}{f_{MSICLKPROG}}$$

Table 64. MSI Controller Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{ISU}	Input Setup Time	5.5		4.7		ns
t_{IH}	Input Hold Time	2		0.5		ns
Switching Characteristics						
t_{MSICLK}	Clock Period Data Transfer Mode[1]	$t_{MSICLKPROG} - 1.5$		$t_{MSICLKPROG} - 1.5$		ns
t_{WL}	Clock Low Time	7		7		ns
t_{WH}	Clock High Time	7		7		ns
t_{TLH}	Clock Rise Time		3		3	ns
t_{THL}	Clock Fall Time		3		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		$(0.5 \times t_{MSICLKIN}) + 3.2$		$(0.5 \times t_{MSICLKIN}) + 3$	ns
t_{OH}	Output Hold Time	$(0.5 \times t_{MSICLKIN}) - 4$		$(0.5 \times t_{MSICLKIN}) - 3$		ns

[1] See Table 18 on Page 52 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{MSICLKPROG}$.

Table 67. 184-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A01	GND	D08	VDD_DMC	H03	SYS_CLKOUT	L14	GND
A02	DMC0_A09	D09	VDD_DMC	H04	VDD_INT	M01	PC_00
A03	DMC0_BA0	D12	PA_08	H05	GND	M02	RTC0_CLKIN
A04	DMC0_BA1	D13	DMC0_DQ06	H06	GND	M03	PB_15
A05	DMC0_BA2	D14	DMC0_DQ05	H07	GND	M04	PB_12
A06	$\overline{\text{DMC0\_CAS}}$	E01	DMC0_A06	H08	GND	M05	PC_12
A07	$\overline{\text{DMC0\_RAS}}$	E02	DMC0_A05	H09	GND	M06	USB0_VBUS
A08	DMC0_A13	E03	JTG_TDI	H10	GND	M07	USB0_VBC
A09	PA_03	E05	VDD_INT	H11	VDD_DMC	M08	PB_09
A10	DMC0_CK	E06	VDD_DMC	H12	PA_10	M09	PB_05
A11	$\overline{\text{DMC0\_CK}}$	E07	VDD_DMC	H13	PA_11	M10	PB_04
A12	DMC0_LDQS	E08	VDD_DMC	H14	$\overline{\text{DMC0\_UDQS}}$	M11	PB_01
A13	$\overline{\text{DMC0\_LDQS}}$	E09	VDD_DMC	J01	PC_05	M12	PB_03
A14	GND	E10	DMC0_VREF	J02	PC_06	M13	DMC0_LDM
B01	DMC0_A07	E12	SYS_BMODE0	J03	$\overline{\text{SYS\_RESOUT}}$	M14	SYS_CLKIN
B02	DMC0_A08	E13	DMC0_DQ08	J04	VDD_INT	N01	RTC0_XTAL
B03	DMC0_A11	E14	DMC0_DQ07	J05	VDD_RTC	N02	PB_14
B04	DMC0_A10	F01	DMC0_A01	J06	GND	N03	PB_11
B05	DMC0_A12	F02	DMC0_A02	J07	GND	N04	PC_14
B06	$\overline{\text{DMC0\_WE}}$	F03	PC_09	J08	GND	N05	PC_11
B07	$\overline{\text{DMC0\_CS0}}$	F04	VDD_INT	J09	GND	N06	USB0_ID
B08	DMC0_ODT	F05	VDD_INT	J10	GND_HADC	N07	USB0_DP
B09	DMC0_CKE	F06	GND	J11	VDD_OTP	N08	PB_08
B10	DMC0_DQ00	F07	GND	J12	PA_13	N09	PB_06
B11	DMC0_DQ02	F08	GND	J13	DMC0_DQ13	N10	PB_00
B12	DMC0_DQ01	F09	GND	J14	DMC0_UDQS	N11	HADC0_VIN2
B13	DMC0_DQ04	F10	VDD_DMC	K01	PC_04	N12	HADC0_VIN1
B14	DMC0_DQ03	F11	VDD_DMC	K02	PC_01	N13	PA_15
C01	JTG_TDO_SWO	F12	$\overline{\text{SYS\_FAULT}}$	K03	PC_02	N14	SYS_XTAL
C02	JTG_TMS_SWDIO	F13	DMC0_DQ10	K05	VDD_EXT	P01	GND
C03	JTG_TCK_SWCLK	F14	DMC0_DQ09	K06	VDD_EXT	P02	PB_13
C04	PA_01	G01	DMC0_A03	K07	VDD_EXT	P03	PB_10
C05	SYS_EXTWAKE	G02	PA_00	K08	VDD_EXT	P04	PC_13
C06	PA_02	G03	PC_08	K09	VDD_EXT	P05	USB0_XTAL
C07	$\overline{\text{SYS\_NMI}}$	G04	VDD_INT	K10	VDD_HADC	P06	USB0_CLKIN
C08	GND	G05	GND	K12	PA_12	P07	USB0_DM
C09	PA_04	G06	GND	K13	DMC0_DQ15	P08	PB_07
C10	PA_05	G07	GND	K14	DMC0_DQ14	P09	HADC0_VREFN
C11	PA_06	G08	GND	L01	PC_03	P10	HADC0_VREFP
C12	PA_07	G09	GND	L02	TWI0_SDA	P11	HADC0_VIN3
C13	$\overline{\text{SYS\_HWRST}}$	G10	GND	L03	TWI0_SCL	P12	HADC0_VIN0
C14	SYS_BMODE1	G11	VDD_DMC	L06	VDD_USB	P13	PA_14
D01	DMC0_A00	G12	PA_09	L07	VDD_EXT	P14	GND
D02	DMC0_A04	G13	DMC0_DQ11	L08	VDD_EXT		
D03	$\overline{\text{JTG\_TRST}}$	G14	DMC0_DQ12	L09	VDD_EXT		
D06	VDD_DMC	H01	PC_07	L12	PB_02		
D07	VDD_DMC	H02	PC_10	L13	DMC0_UDM		

Table 70. ADSP-BF70x 12 mm × 12 mm 88 -Lead LFCSP (QFN) Lead Assignments (Alphabetical by Signal Name)

Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.
GND	76	PB_00	52	PC_07	5	USB0_VBUS	34
GND	89	PB_01	48	PC_08	3	USB0_XTAL	31
JTG_TCK_SWCLK	85	PB_02	47	PC_09	2	VDD_EXT	4
JTG_TDI	86	PB_03	46	PC_10	1	VDD_EXT	11
JTG_TDO_SWO	83	PB_04	45	RTC0_CLKIN	21	VDD_EXT	17
JTG_TMS_SWDIO	84	PB_05	44	RTC0_XTAL	20	VDD_EXT	26
$\overline{\text{JTG\_TRST}}$	87	PB_06	43	SYS_BMODE0	66	VDD_EXT	41
PA_00	88	PB_07	42	SYS_BMODE1	67	VDD_EXT	50
PA_01	80	PB_08	40	SYS_CLKIN	57	VDD_EXT	55
PA_02	78	PB_09	39	SYS_CLKOUT	12	VDD_EXT	62
PA_03	75	PB_10	29	SYS_EXTWAKE	79	VDD_EXT	72
PA_04	74	PB_11	28	$\overline{\text{SYS\_FAULT}}$	65	VDD_EXT	82
PA_05	73	PB_12	27	$\overline{\text{SYS\_HWRST}}$	68	VDD_INT	14
PA_06	71	PB_13	25	$\overline{\text{SYS\_NMI}}$	77	VDD_INT	30
PA_07	70	PB_14	24	$\overline{\text{SYS\_RESOUT}}$	15	VDD_INT	51
PA_08	69	PB_15	23	SYS_XTAL	56	VDD_INT	61
PA_09	64	PC_00	16	TWI0_SCL	19	VDD_INT	81
PA_10	63	PC_01	13	TWI0_SDA	18	VDD_OTP	49
PA_11	60	PC_02	10	USB0_CLKIN	32	VDD_RTC	22
PA_12	59	PC_03	9	USB0_DM	37	VDD_USB	36
PA_13	58	PC_04	8	USB0_DP	35		
PA_14	54	PC_05	7	USB0_ID	33		
PA_15	53	PC_06	6	USB0_VBC	38		