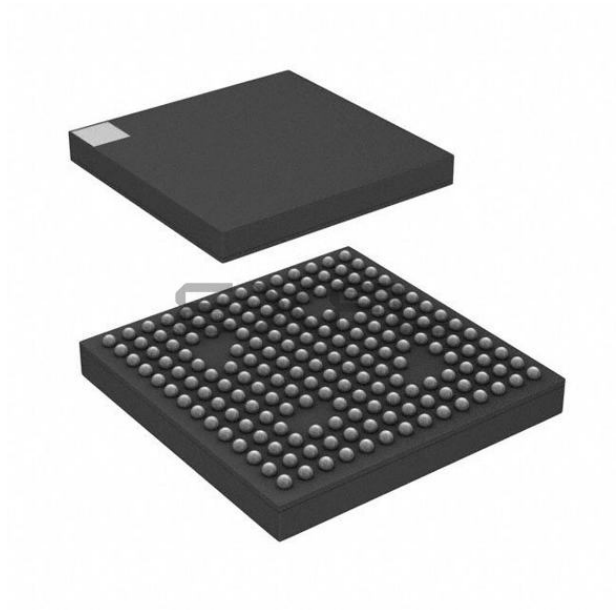

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	200MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	128kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf701kbcz-2

- A similar buffer that interrupts on fractional buffers (for example, 1/2, 1/4).
- 1D DMA—uses a set of identical ping-pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address.
- 1D DMA—uses a linked list of 4 word descriptor sets containing a link pointer, an address, a length, and a configuration.
- 2D DMA—uses an array of one-word descriptor sets, specifying only the base DMA address.
- 2D DMA—uses a linked list of multi-word descriptor sets, specifying everything.

Event Handling

The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The processor provides support for five different types of events:

- Emulation—An emulation event causes the processor to enter emulation mode, allowing command and control of the processor through the JTAG interface.
- Reset—This event resets the processor.
- Nonmaskable interrupt (NMI)—The NMI event can be generated either by the software watchdog timer, by the $\overline{\text{NMI}}$ input signal to the processor, or by software. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions—Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts —Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

The SEC manages the enabling, prioritization, and routing of events from each system interrupt or fault source. Additionally, it provides notification and identification of the highest priority active system interrupt request to the core and routes system fault sources to its integrated fault management unit. The SEC triggers core general-purpose interrupt IVG11. It is recommended that IVG11 be set to allow self-nesting. The four lower priority interrupts (IVG15-12) may be used for software interrupts.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register—Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers—A write one to modify mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers—Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers—Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Interrupts

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Three system-level interrupt channels (PINT0–3) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of 4 peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature—that is, when the

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- CAN wake-up from hibernation mode (lowest static power consumption mode)
- Interrupts, including: TX complete, RX complete, error and global

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from a system clock through a programmable divider.

USB 2.0 On-the-Go Dual-Role Device Controller

The USB 2.0 on-the-go (OTG) dual-role device controller provides a low-cost connectivity solution for the growing adoption of this bus standard in industrial applications, as well as consumer mobile devices such as cell phones, digital still cameras, and MP3 players. The USB 2.0 controller allows these devices to transfer data using a point-to-point USB connection without the need for a PC host. The module can operate in a traditional USB peripheral-only mode as well as the host mode presented in the OTG supplement to the USB 2.0 specification.

The USB clock is provided through a dedicated external crystal or crystal oscillator.

The USB OTG dual-role device controller includes a phase locked loop with programmable multipliers to generate the necessary internal clocking frequency for USB.

Housekeeping ADC (HADC)

The HADC provides a general-purpose, multichannel successive approximation analog-to-digital converter. It supports the following features:

- 12-bit ADC core (10-bit accuracy) with built-in sample and hold
- 4 single-ended input channels
- Throughput rates up to 1 MSPS
- Single external reference with analog inputs between 0 V and 3.3 V
- Selectable ADC clock frequency including the ability to program a prescaler
- Adaptable conversion type: allows single or continuous conversion with option of autoscan
- Auto sequencing capability with up to 4 autoconversions in a single session. Each conversion can be programmed to select any input channel.
- Four data registers (individually addressable) to store conversion values

System Crossbars (SCB)

The system crossbars (SCB) are the fundamental building blocks of a switch-fabric style for (on-chip) system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnect, which satisfies the performance and flexibility requirements of a specific system.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

POWER AND CLOCK MANAGEMENT

The processor provides three operating modes, each with a different performance/power profile. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 5 for a summary of the power settings for each mode.

System Crystal Oscillator and USB Crystal Oscillator

The processor can be clocked by an external crystal (see Figure 4), a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the SYS_CLKIN pin of the processor. When an external clock is used, the SYS_XTAL pin must be left unconnected. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used.

For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor grade crystal is connected across the SYS_CLKIN and SYS_XTAL pins. The on-chip resistance between SYS_CLKIN and the SYS_XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended.

The two capacitors and the series resistor shown in Figure 4 fine-tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the PCB physical layout. The resistor value depends on the drive

ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

GPIO MULTIPLEXING FOR 12 mm × 12 mm 88-LEAD LFCSP (QFN)

Table 12 through Table 14 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 12 mm × 12 mm 88-Lead LFCSP (QFN) package.

Table 12. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	SPI1_CLK		TRACE0_D07	SMC0_ABE0	
PA_01	SPI1_MISO		TRACE0_D06	SMC0_ABE1	
PA_02	SPI1_MOSI		TRACE0_D05	SMC0_AMS1	
PA_03	SPI1_SEL2	SPI1_RDY		SMC0_ARDY	
PA_04	SPI1_SEL1	TM0_TMR7	SPI2_RDY	SMC0_A08	SPI1_SS
PA_05	TM0_TMR0	SPI0_SEL1		SMC0_A07	SPI0_SS
PA_06	TM0_TMR1	SPI0_SEL2	SPI0_RDY	SMC0_A06	
PA_07	TM0_TMR2	SPT1_BTDV	SPT1_ATDV	SMC0_A05	CNT0_DG
PA_08	PPI0_D11	MSI0_CD	SPT1_ACLK	SMC0_A01	
PA_09	PPI0_D10	TM0_TMR4	SPT1_AFS	SMC0_A02	
PA_10	PPI0_D09	TM0_TMR5	SPT1_AD0	SMC0_A03	
PA_11	PPI0_D08	TM0_TMR6	SPT1_AD1	SMC0_A04	
PA_12	PPI0_FS1	CAN1_RX	SPT0_AFS	SMC0_AOE	TM0_ACI6/SYS_WAKE4
PA_13	PPI0_FS2	CAN1_TX	SPT0_ACLK	SMC0_ARE	CNT0_ZM
PA_14	PPI0_CLK	SPI1_SEL4	SPT0_AD0	SMC0_AWE	TM0_ACLK5
PA_15	PPI0_FS3	SPT0_ATDV	SPT0_BTDV	SMC0_AMS0	CNT0_UD

Table 13. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PPI0_D07	SPT1_BCLK	SPI0_CLK	SMC0_D07	TM0_ACLK3
PB_01	PPI0_D06	SPT1_BFS	SPI0_MISO	SMC0_D06	TM0_ACI1
PB_02	PPI0_D05	SPT1_BD0	SPI0_MOSI	SMC0_D05	
PB_03	PPI0_D04	SPT1_BD1	SPI0_D2	SMC0_D04	
PB_04	PPI0_D03	SPT0_BCLK	SPI0_SEL4	SMC0_D03	TM0_ACLK6
PB_05	PPI0_D02	SPT0_BD0	SPI0_SEL5	SMC0_D02	
PB_06	PPI0_D01	SPT0_BFS	SPI0_SEL6	SMC0_D01	TM0_CLK
PB_07	PPI0_D00	SPT0_BD1	SPI0_D3	SMC0_D00	SYS_WAKE0
PB_08	UART0_TX	PPI0_D16	SPI2_SEL2	SMC0_D08	SYS_WAKE1
PB_09	UART0_RX	PPI0_D17	SPI2_SEL3	SMC0_D09	TM0_ACI3
PB_10	SPI2_CLK		TRACE0_CLK	SMC0_D10	TM0_ACLK4
PB_11	SPI2_MISO		TRACE0_D04	SMC0_D11	
PB_12	SPI2_MOSI		TRACE0_D03	SMC0_D12	SYS_WAKE2
PB_13	SPI2_D2	UART1_RTS	TRACE0_D02	SMC0_D13	
PB_14	SPI2_D3	UART1_CTS	TRACE0_D01	SMC0_D14	
PB_15	SPI2_SEL1		TRACE0_D00	SMC0_D15	SPI2_SS

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master Out, Slave In | TRACE0 Trace Data 5 | SMC0 Memory Select 1 Notes: May require a pull-up if used as an SMC memory select. Check the data sheet requirements of the IC it connects to.
PA_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 2 | SPI1 Ready | SMC0 Asynchronous Ready Notes: May require a pull-up or pull-down if used as an SMC asynchronous ready. Check the data sheet requirements of the IC it connects to and the programmed polarity.
PA_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Slave Select Output 1 | TM0 Timer 7 | SPI2 Ready | SMC0 Address 8 | SPI1 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PA_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 0 | SPI0 Slave Select Output 1 | SMC0 Address 7 | SPI0 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PA_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 1 | SPI0 Slave Select Output 2 | SPI0 Ready | SMC0 Address 6 Notes: SPI slave select outputs require a pull-up when used.
PA_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: TM0 Timer 2 | SPT1 Channel B Transmit Data Valid | SPT1 Channel A Transmit Data Valid | SMC0 Address 5 | CNT0 Count Down and Gate Notes: No notes.
PA_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 11 | MSI0 Card Detect | SPT1 Channel A Clock | SMC0 Address 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PA_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 10 | TM0 Timer 4 | SPT1 Channel A Frame Sync | SMC0 Address 2 Notes: No notes.
PA_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 9 | TM0 Timer 5 | SPT1 Channel A Data 0 | SMC0 Address 3 Notes: No notes.
PA_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 8 | TM0 Timer 6 | SPT1 Channel A Data 1 | SMC0 Address 4 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Frame Sync | TM0 Timer 3 | MSI0 Command Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Data 0 | SPI0 Master In, Slave Out | MSI0 Data 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Frame Sync | SPI0 Master Out, Slave In | MSI0 Data 2 | TM0 Alternate Capture Input 2 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Data 0 | SPI0 Data 2 | MSI0 Data 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Clock | SPI0 Data 3 | MSI0 Clock | TM0 Alternate Clock 2 Notes: No notes.
PC_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Clock | MSI0 Data 4 | SPI1 Slave Select Output 3 | TM0 Alternate Clock 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Frame Sync | MSI0 Data 5 | SPI0 Slave Select Output 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 0 | MSI0 Data 6 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Internal Supply Voltage	CCLK ≤ 400 MHz	1.045	1.100	1.155	V
V_{DD_EXT}[1]	External Supply Voltage		1.7	1.8	1.9	V
V_{DD_EXT}[1]	External Supply Voltage		3.13	3.30	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.30	3.47	V
V_{DD_RTC}	Real-Time Clock Supply Voltage		2.00	3.30	3.47	V
V_{DD_HADC}	Housekeeping ADC Supply Voltage		3.13	3.30	3.47	V
V_{DD_OTP}[1]	OTP Supply Voltage					
	For Reads		2.25	3.30	3.47	V
	For Writes		3.13	3.30	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 1.9 V	0.7 × V_{DD_EXT}			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = maximum	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[7]		V_{DD_DMC} = 1.9 V	V_{DDR_REF} + 0.25			V
V_{IH_LPDDR}[8]		V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 1.075 V	0.50			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 0.725 V	0.55			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 1.7 V			0.3 × V_{DD_EXT}	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7]		V_{DD_DMC} = 1.7 V			V_{DDR_REF} – 0.25	V
V_{IL_LPDDR}[8]		V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0°C to +70°C	0		105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] If not used, connect to 1.8 V or 3.3 V.
[3] V_{HADC_VREF} should always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional signals except RTC signals, TWI signals, DMC0 signals, and USB0 signals.
[5] Parameter applies to TWI signals.
[6] TWI signals are pulled up to V_{BUSTWI}. See Table 16.
[7] Parameter applies to DMC0 signals in DDR2 mode.
[8] Parameter applies to DMC0 signals in LPDDR mode.
[9] Parameter applies to signals DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$ when used in DDR2 differential input mode.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 and Table 18 describe the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Core and System Clock Operating Conditions

Parameter		Ratio Restriction	PLLCLK Restriction	Min	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	PLLCLK = 800		400	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	600 ≤ PLLCLK < 800		390	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	380 ≤ PLLCLK < 600		380	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	230.2 ≤ PLLCLK < 380		PLLCLK	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		PLLCLK = 800	60	200	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		600 ≤ PLLCLK < 800	60	195	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		380 ≤ PLLCLK < 600	60	190	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		230.2 ≤ PLLCLK < 380	60	PLLCLK ÷ 2	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$		30	100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2 Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		125	200	MHz
f_{DCLK}	LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		10	200	MHz

[1] The minimum frequency for SYSCLK and SCLK0 applies only when the USB is used.

Table 18. Peripheral Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{OCLK}	Output Clock Frequency				50	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[1, 2]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				50	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				50	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{MSICLKPROG}$	Programmed MSI Clock				50	MHz

[1] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this typical specification for each end application.
[2] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[3] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications section for that peripheral. Pay particular attention to setup and hold times for VDD_EXT = 1.8 V which may preclude the maximum frequency listed here.
[4] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} that clocks the peripheral.

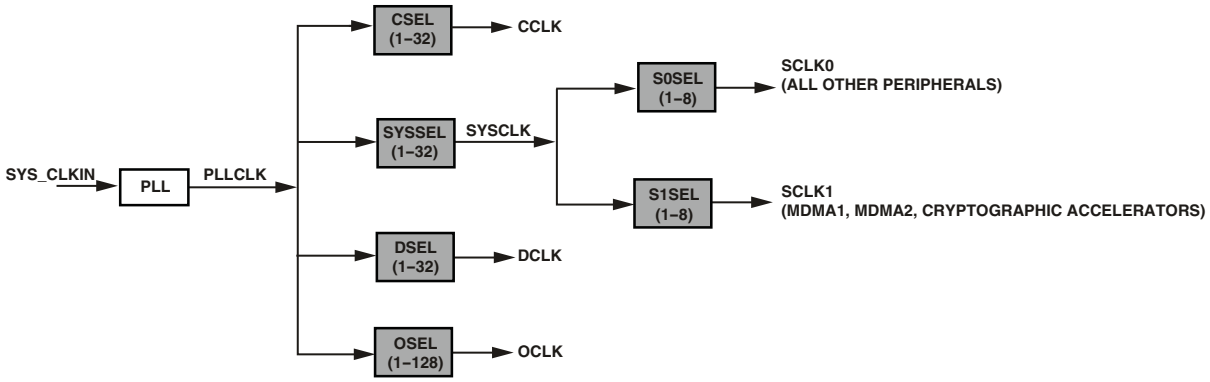


Figure 6. Clock Relationships and Divider Values

Table 19. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	230.2	800	MHz
CGU_CTL.MSEL[1]	PLL Multiplier	8	41	

[1] The CGU_CTL.MSEL setting must also be chosen to ensure that the f_{PLLCLK} specification is not violated.

Table 21. Static Current—$I_{DD\_DEEPSLEEP}$ (mA)

	Voltage (V_{DD_INT})												
T_J (°C)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
–40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
–20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

Table 22. Activity Scaling Factors (ASF)

I_{DDINT} Power Vector	ASF
$I_{DD-IDLE1}$	0.05
$I_{DD-IDLE2}$	0.05
$I_{DD-NOP1}$	0.56
$I_{DD-NOP2}$	0.59
$I_{DD-APP3}$	0.78
$I_{DD-APP1}$	0.79
$I_{DD-APP2}$	0.83
$I_{DD-TYP1}$	1.00
$I_{DD-TYP3}$	1.01
$I_{DD-TYP2}$	1.03
$I_{DD-HIGH1}$	1.39
$I_{DD-HIGH3}$	1.39
$I_{DD-HIGH2}$	1.54

Table 23. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})												
f_{CCLK} (MHz)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

Power-Up Reset Timing

A power-up reset is required to place the processor in a known state after power-up. A power-up reset is initiated by asserting $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$. During power-up reset, all pins are high impedance except for those noted in the ADSP-BF70x Designer Quick Reference on Page 38.

Both $\overline{\text{JTG\_TRST}}$ and $\overline{\text{SYS\_HWRST}}$ need to be asserted upon power-up, but only $\overline{\text{SYS\_HWRST}}$ needs to be released for the device to boot properly. $\overline{\text{JTG\_TRST}}$ may be asserted indefinitely for normal operation. $\overline{\text{JTG\_TRST}}$ only needs to be released when using an emulator to connect to the DAP for debug or boundary scan. There is an internal pull-down on $\overline{\text{JTG\_TRST}}$ to ensure internal emulation logic will always be properly initialized during power-up reset.

Table 30 and Figure 9 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU). In Figure 9, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, and V_{DD_HADC}.

There is no power supply sequencing requirement for the ADSP-BF70x processor. However, if saving power during power-on is important, bringing up V_{DD_INT} last is recommended. This avoids a small current drain in the V_{DD_INT} domain during the transition period of I/O voltages from 0 V to within the voltage specification.

Table 30. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ Deasserted After V_{DD_INT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, V_{DD_HADC}, and SYS_CLKIN are Stable and Within Specification	$11 \times t_{CKIN}$		ns
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (No External Pull-Down on $\overline{\text{JTG\_TRST}}$)	10		µs
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (10k External Pull-Down on $\overline{\text{JTG\_TRST}}$)	1		µs

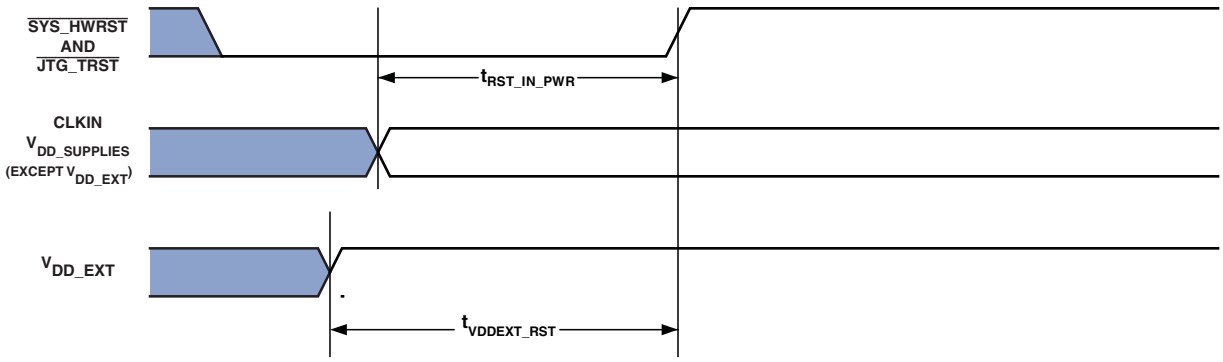


Figure 9. Power-Up Reset Timing

Asynchronous Flash Read

Table 33 and Figure 12 show asynchronous flash memory read timing, related to the static memory controller (SMC).

Table 33. Asynchronous Flash Read

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before SMC0_NORDV Low[1]	PREST × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From SMC0_NORDV High[3]	PREAT × t_{SCLK0} – 2		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK0} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$, $\overline{\text{SMC0\_AOE}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

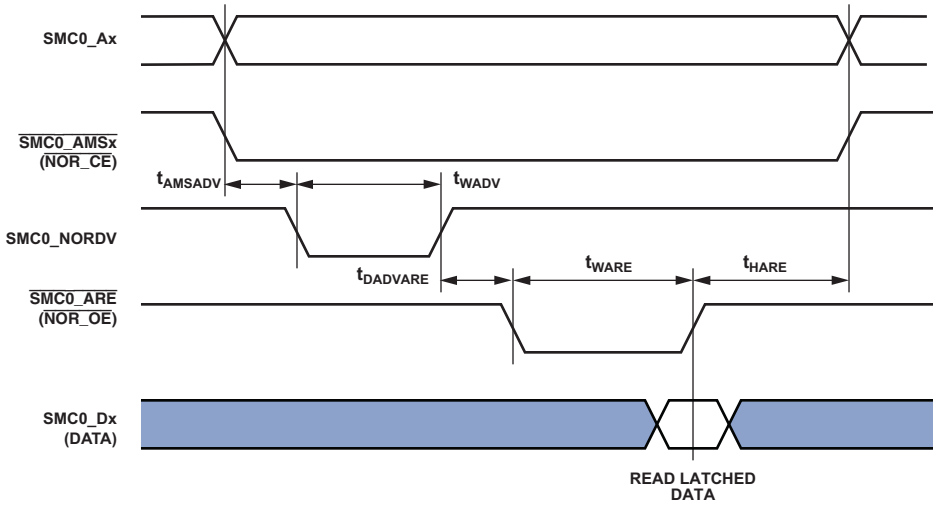


Figure 12. Asynchronous Flash Read

DDR2 SDRAM Read Cycle Timing

Table 40 and Figure 18 show DDR2 SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 40. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1] Min	Max	Unit
Timing Requirements				
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.35	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.8		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.

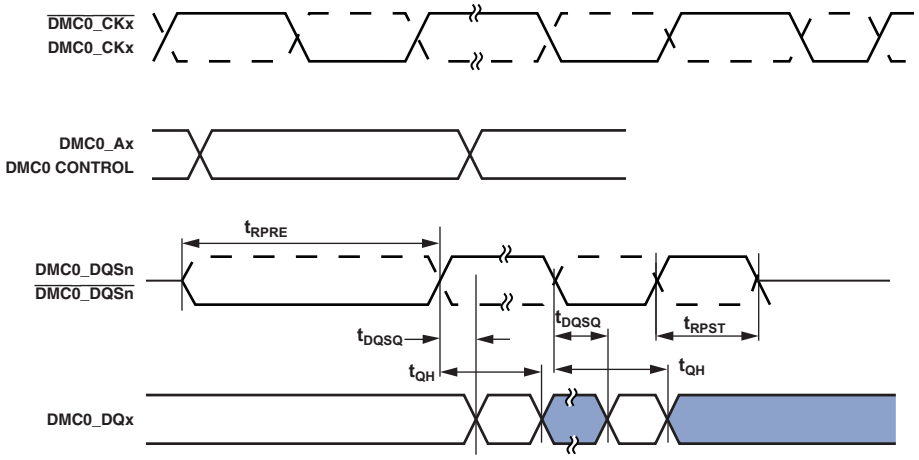


Figure 18. DDR2 SDRAM Controller Input AC Timing

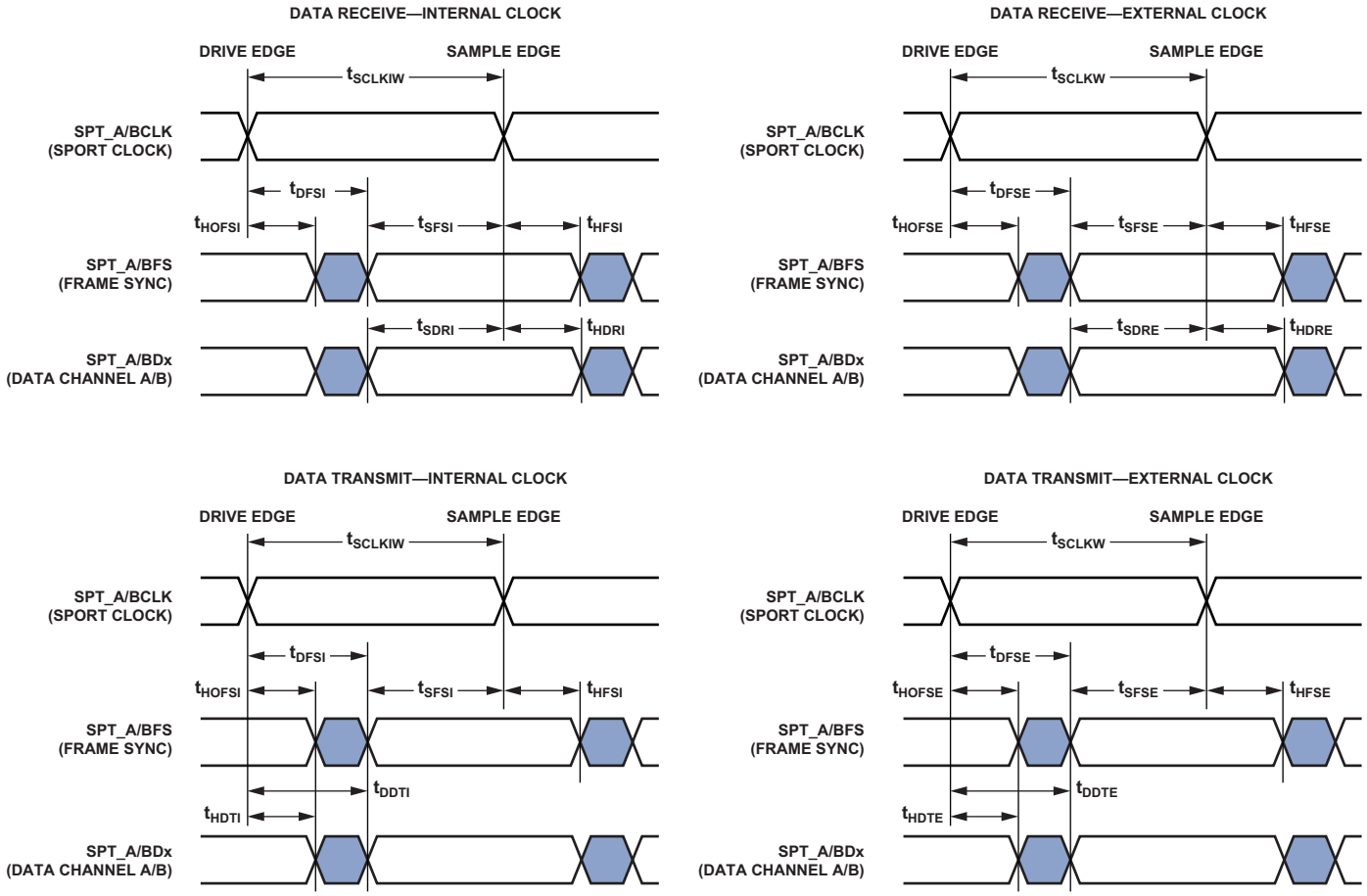


Figure 27. Serial Ports

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

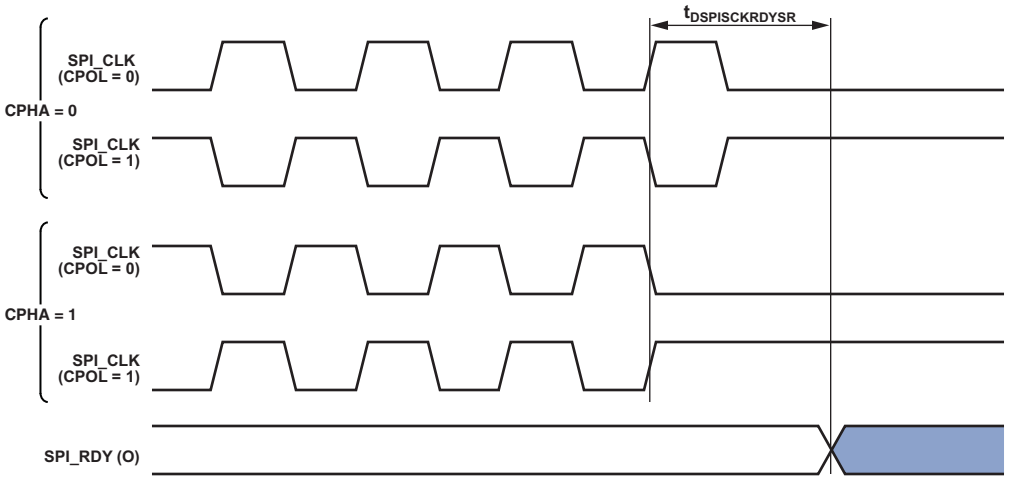


Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

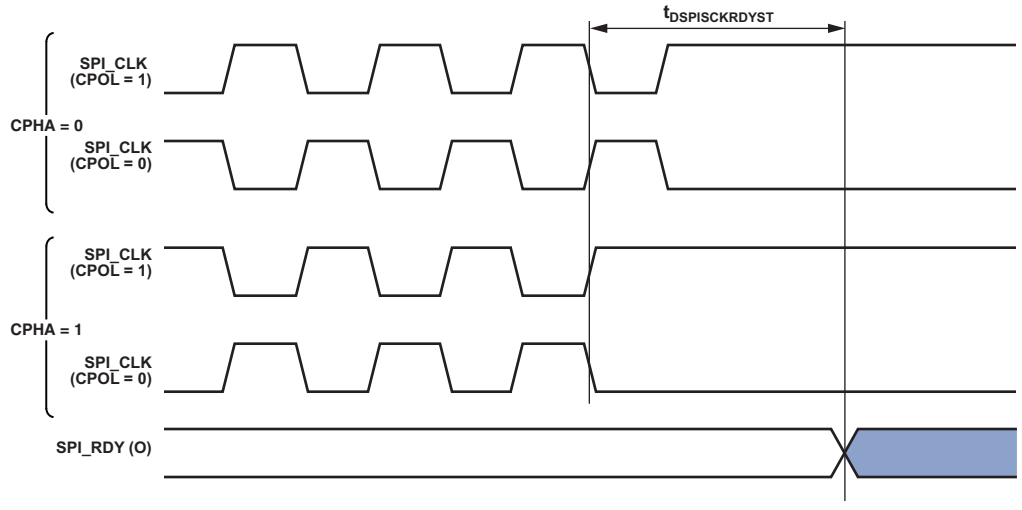


Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

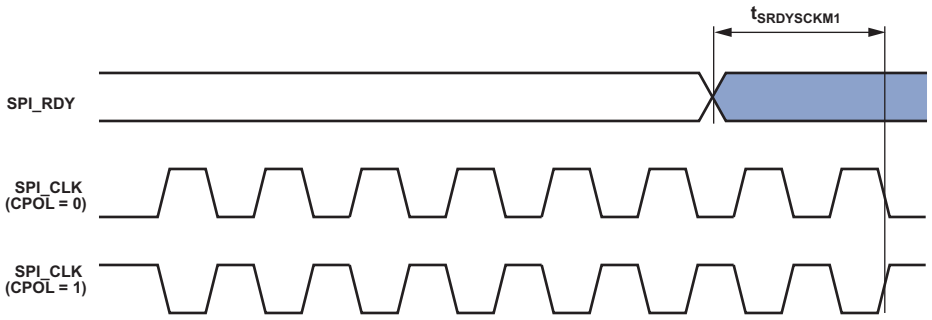


Figure 38. SPI_RDY Setup Before SPI_CLK with CPHA = 1

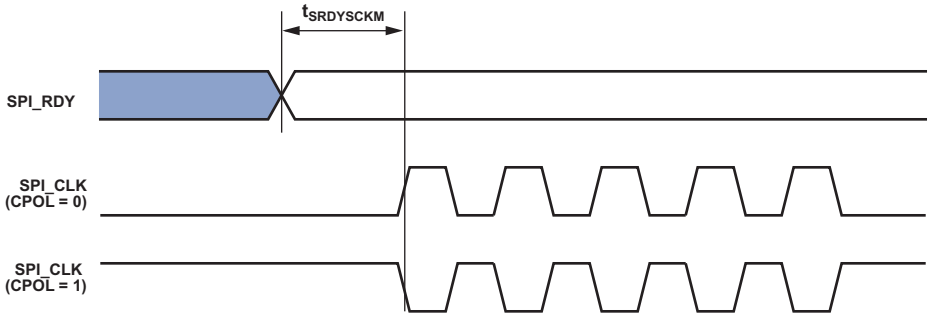
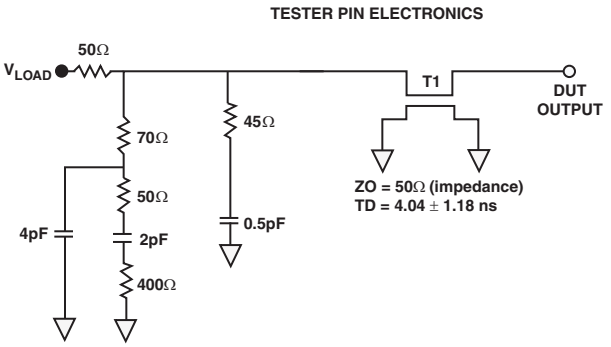


Figure 39. SPI_CLK Switching Diagram after SPI_RDY Assertion, CPHA = x

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 64). V_{LOAD} is equal to $V_{DD\_EXT}/2$. The graphs of Figure 65 through Figure 68 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 64. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

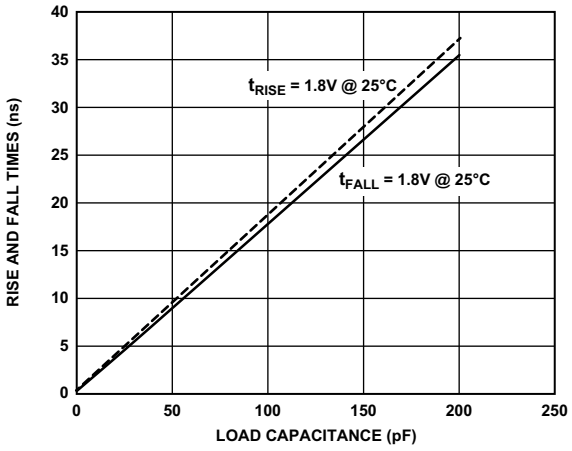


Figure 65. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 1.8 V)

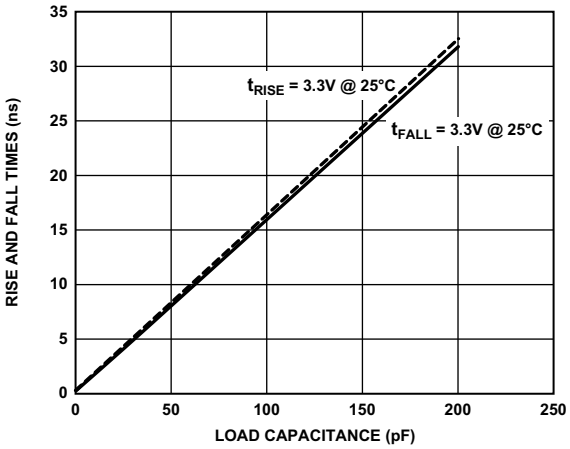


Figure 66. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

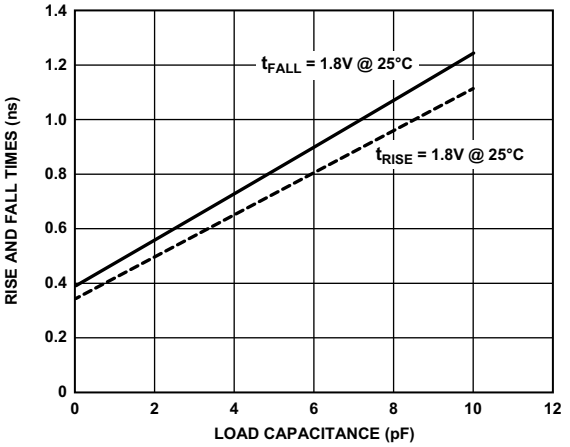


Figure 67. Driver Type B & C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V)

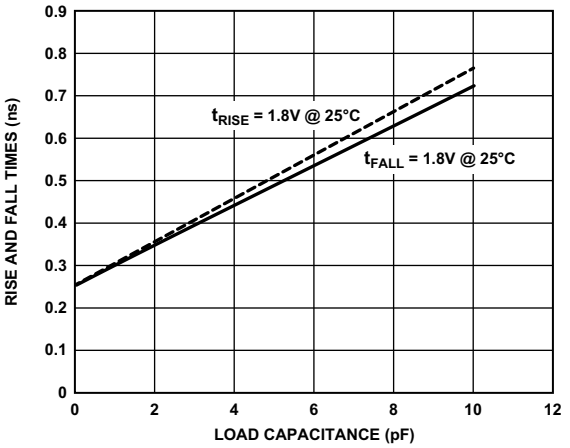


Figure 68. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for LPDDR

ADSP-BF70x 184-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Figure 69 shows an overview of signal placement on the 184-ball CSP_BGA.

Table 67 lists the 184-ball CSP_BGA package by ball number for the ADSP-BF70x. Table 68 lists the 184-ball CSP_BGA package by signal.

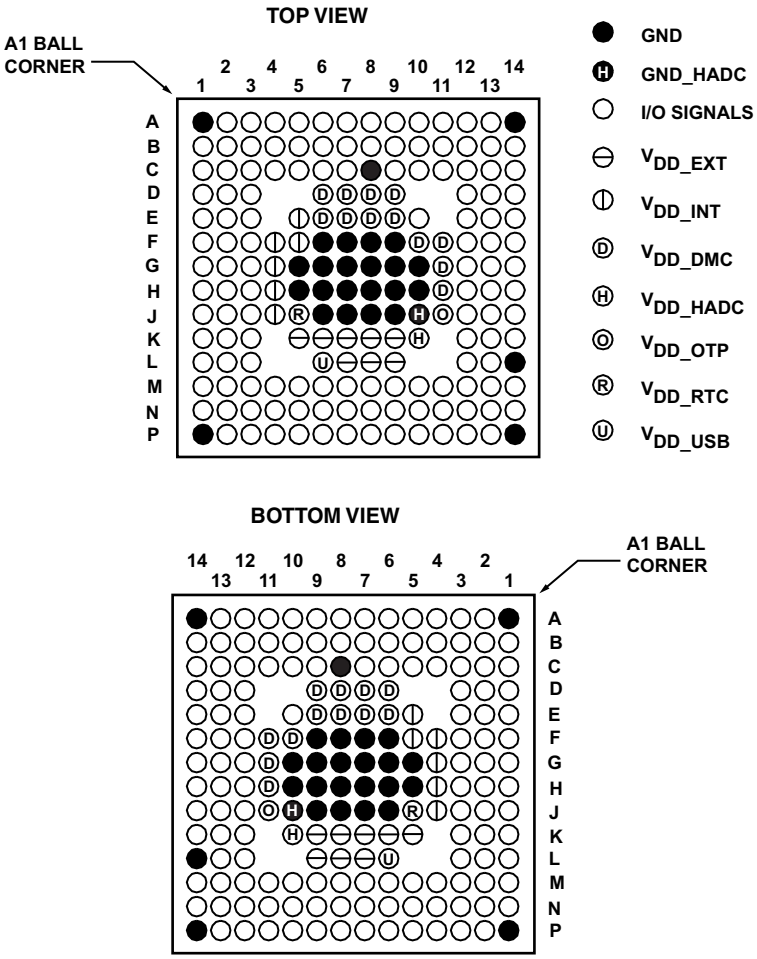


Figure 69. 184-Ball CSP_BGA Configuration

Table 69 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by lead number for the ADSP-BF70x. Table 70 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by signal.

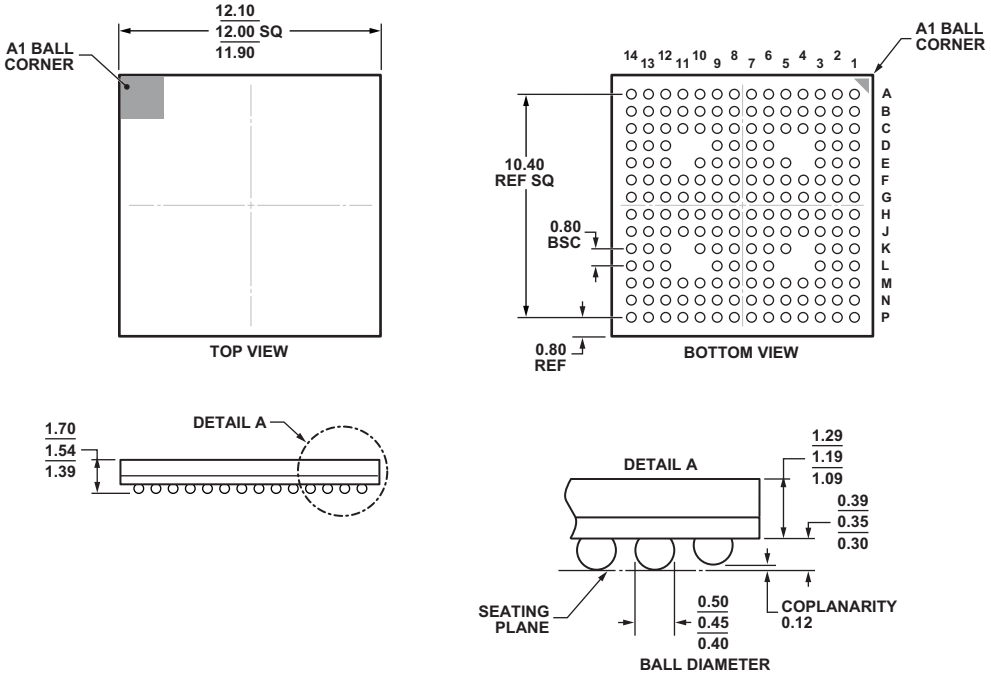
Table 69. 12 mm × 12 mm 88-Lead LFCSP (QFN) Lead Assignment (Numerical by Lead Number)

Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name
1	PC_10	24	PB_14	47	PB_02	70	PA_07
2	PC_09	25	PB_13	48	PB_01	71	PA_06
3	PC_08	26	VDD_EXT	49	VDD_OTP	72	VDD_EXT
4	VDD_EXT	27	PB_12	50	VDD_EXT	73	PA_05
5	PC_07	28	PB_11	51	VDD_INT	74	PA_04
6	PC_06	29	PB_10	52	PB_00	75	PA_03
7	PC_05	30	VDD_INT	53	PA_15	76	GND
8	PC_04	31	USB0_XTAL	54	PA_14	77	$\overline{\text{SYS\_NMI}}$
9	PC_03	32	USB0_CLKIN	55	VDD_EXT	78	PA_02
10	PC_02	33	USB0_ID	56	SYS_XTAL	79	SYS_EXTWAKE
11	VDD_EXT	34	USB0_VBUS	57	SYS_CLKIN	80	PA_01
12	SYS_CLKOUT	35	USB0_DP	58	PA_13	81	VDD_INT
13	PC_01	36	VDD_USB	59	PA_12	82	VDD_EXT
14	VDD_INT	37	USB0_DM	60	PA_11	83	JTG_TDO_SWO
15	$\overline{\text{SYS\_RESOUT}}$	38	USB0_VBC	61	VDD_INT	84	JTG_TMS_SWDIO
16	PC_00	39	PB_09	62	VDD_EXT	85	JTG_TCK_SWCLK
17	VDD_EXT	40	PB_08	63	PA_10	86	JTG_TDI
18	TWI0_SDA	41	VDD_EXT	64	PA_09	87	$\overline{\text{JTG\_TRST}}$
19	TWI0_SCL	42	PB_07	65	$\overline{\text{SYS\_FAULT}}$	88	PA_00
20	RTC0_XTAL	43	PB_06	66	SYS_BMODE0	89*	GND
21	RTC0_CLKIN	44	PB_05	67	SYS_BMODE1		
22	VDD_RTC	45	PB_04	68	$\overline{\text{SYS\_HWRST}}$		
23	PB_15	46	PB_03	69	PA_08		

*Pin no. 89 is the GND supply (see Figure 70) for the processor; this pad must connect to GND.

OUTLINE DIMENSIONS

Dimensions for the 12 mm × 12 mm CSP_BGA package in Figure 71 are shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MO-275-GGAA-1

Figure 71. 184-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-184-1)
Dimensions shown in millimeters