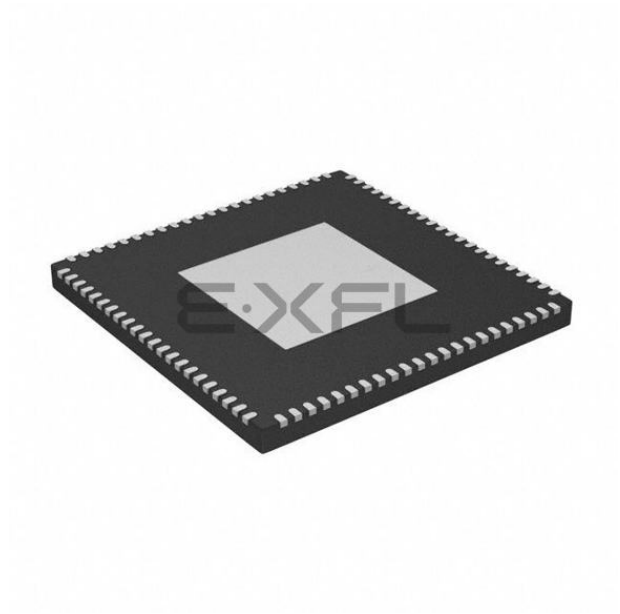

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf702bcpz-4

BLACKFIN+ PROCESSOR CORE

As shown in Figure 1, the processor integrates a Blackfin+ processor core. The core, shown in Figure 2, contains two 16-bit multipliers, one 32-bit multiplier, two 40-bit accumulators (which may be used together as a 72-bit accumulator), two 40-bit ALUs, one 72-bit ALU, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

The core can perform two 16-bit by 16-bit multiply-accumulates or one 32-bit multiply-accumulate in each cycle. Signed and unsigned formats, rounding, saturation, and complex multiplies are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If a second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

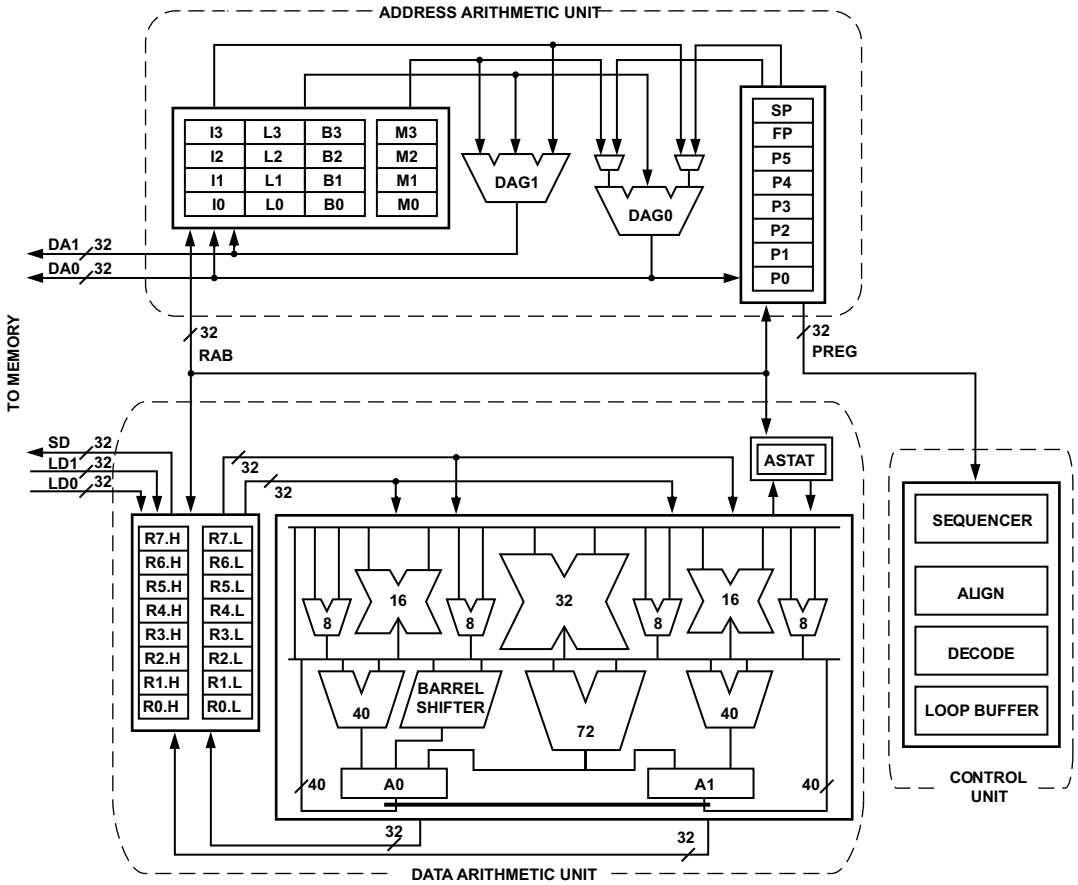

Figure 2. Blackfin+ Processor Core

Serial Peripheral Interface (SPI) Ports

The processors have three industry-standard SPI-compatible ports that allow it to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, four-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An additional two (optional) data pins are provided to support quad SPI operation. Enhanced modes of operation such as flow control, fast mode, and dual I/O mode (DIOM) are also supported. In addition, a direct memory access (DMA) mode allows for transferring several words with minimal CPU interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other devices, acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI Ready pin which flexibly controls the transfers.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

SPI Host Port (SPIHP)

The processor includes one SPI host port which may be used in conjunction with any available SPI port to enhance its SPI slave mode capabilities. The SPIHP allows a SPI host device access to memory-mapped resources of the processor through a SPI SRAM/FLASH style protocol. The following features are included:

- Direct read/write of memory and memory-mapped registers
- Support for pre-fetch for faster reads
- Support for SPI controllers that implement hardware-based SPI memory protocol
- Error capture and reporting for protocol errors, bus errors, and over/underflow

UART Ports

The processor provides two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion FIFO levels.

To help support the local interconnect network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Controller Interface (TWI)

The processor includes a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Mobile Storage Interface (MSI)

The mobile storage interface (MSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), and secure digital input/output cards (SDIO). The following list describes the main features of the MSI controller:

- Support for a single MMC, SD memory, and SDIO card
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for eMMC 4.5 embedded NAND flash devices
- Support for power management and clock control
- An eleven-signal external interface with clock, command, optional interrupt, and up to eight data lines
- Card interface clock generation from SCLK0 or SCLK1
- SDIO interrupt and read wait features

Controller Area Network (CAN)

A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

SECURITY FEATURES DISCLAIMER

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Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0\_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0\_LDQS}}$
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0\_RAS}}$	DMC0 Row Address Strobe	Not Muxed	$\overline{\text{DMC0\_RAS}}$
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0\_UDQS}}$	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0\_UDQS}}$
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
$\overline{\text{DMC0\_WE}}$	DMC0 Write Enable	Not Muxed	$\overline{\text{DMC0\_WE}}$
GND	Ground	Not Muxed	GND
GND_HADC	Ground HADC	Not Muxed	GND_HADC
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG\_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
MSI0_D5	MSI0 Data 5	C	PC_11
MSI0_D6	MSI0 Data 6	C	PC_12
MSI0_D7	MSI0 Data 7	C	PC_13

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
$\overline{\text{MSI0\_INT}}$	MSI0 eSDIO Interrupt Input	C	PC_14
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_14	Position 00 through Position 14	C	PC_00-PC_14
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input/external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_FAULT	Active-Low Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Nonmaskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
UART0_CTS	UART0 Clear to Send	C	PC_03
UART0_RTS	UART0 Request to Send	C	PC_02

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input/external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	A	PA_13
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 6 Notes: No notes.
DMC0_A07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 7 Notes: No notes.
DMC0_A08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 8 Notes: No notes.
DMC0_A09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 9 Notes: No notes.
DMC0_A10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 10 Notes: No notes.
DMC0_A11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 11 Notes: No notes.
DMC0_A12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 12 Notes: No notes.
DMC0_A13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 13 Notes: No notes.
DMC0_BA0	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 0 Notes: No notes.
DMC0_BA1	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 1 Notes: No notes.
DMC0_BA2	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 2 Notes: For LPDDR, leave unconnected.
$\overline{\text{DMC0\_CAS}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes.
DMC0_CK	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes.
$\overline{\text{DMC0\_CK}}$	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock (complement) Notes: No notes.
DMC0_CKE	I/O	B	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock enable Notes: No notes.
$\overline{\text{DMC0\_CS0}}$	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Chip Select 0 Notes: No notes.
DMC0_DQ00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 0 Notes: No notes.
DMC0_DQ01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 1 Notes: No notes.
DMC0_DQ02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 2 Notes: No notes.
DMC0_DQ03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 3 Notes: No notes.
DMC0_DQ04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 4 Notes: No notes.
DMC0_DQ05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 5 Notes: No notes.
DMC0_DQ06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 6 Notes: No notes.
DMC0_DQ07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 7 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
GND_HADC	g	na	none	none	none	none	none	na	Desc: Ground HADC Notes: If HADC is not used, connect to ground.
HADC0_VIN0	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: If HADC is not used, connect to ground.
HADC0_VIN1	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: If HADC is not used, connect to ground.
HADC0_VIN2	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: If HADC is not used, connect to ground.
HADC0_VIN3	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: If HADC is not used, connect to ground.
HADC0_VREFN	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: If HADC is not used, connect to ground.
HADC0_VREFP	a	na	none	none	none	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: If HADC is not used, connect to ground.
JTG_TCK_ SWCLK	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Clock | Serial Wire Clock Notes: Functional during reset.
JTG_TDI	I/O	na	pu	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data In Notes: Functional during reset.
JTG_TDO_SWO	I/O	A	none	none	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out | Serial Wire Out Notes: Functional during reset, three-state when $\overline{\text{JTG\_TRST}}$ is asserted.
JTG_TMS_ SWDIO	I/O	A	pu	none	none	none	none	VDD_EXT	Desc: JTAG Mode Select | Serial Wire DIO Notes: Functional during reset.
$\overline{\text{JTG\_TRST}}$	I/O	na	pd	none	none	none	none	VDD_EXT	Desc: JTAG Reset Notes: Functional during reset, a 10k external pull-down may be used to shorten the t_{VDDEXT_RST} timing requirement.
PA_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Clock | TRACE0 Trace Data 7 | SMC0 Byte Enable 0 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PA_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI1 Master In, Slave Out | TRACE0 Trace Data 6 | SMC0 Byte Enable 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 1 (HSYNC) | CAN1 Receive | SPORT0 Channel A Frame Sync |SMC0 Output Enable |SYS Power Saving Mode Wakeup 4 | TM0 Alternate Capture Input 6 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PA_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 2 (VSYNC) | CAN1 Transmit | SPORT0 Channel A Clock | SMC0 Read Enable | CNT0 Count Zero Marker Notes: No notes.
PA_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Clock | SPI1 Slave Select Output 4 | SPORT0 Channel A Data 0 | SMC0 Write Enable | TM0 Alternate Clock 5 Notes: SPI slave select outputs require a pull-up when used.
PA_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 3 (FIELD) | SPT0 Channel A Transmit Data Valid | SPT0 Channel B Transmit Data Valid | SMC0 Memory Select 0 | CNT0 Count Up and Direction Notes: May require a pull-up if used as an SMC memory select. Check the data sheet requirements of the IC it connects to.
PB_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 7 | SPT1 Channel B Clock | SPI0 Clock | SMC0 Data 7 | TM0 Alternate Clock 3 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PB_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 6 | SPT1 Channel B Frame Sync | SPI0 Master In, Slave Out | SMC0 Data 6 | TM0 Alternate Capture Input 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.
PB_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 5 | SPT1 Channel B Data 0 | SPI0 Master Out, Slave In | SMC0 Data 5 Notes: No notes.
PB_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 4 | SPT1 Channel B Data 1 | SPI0 Data 2 | SMC0 Data 4 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 3 | SPT0 Channel B Clock | SPI0 Slave Select Output 4 | SMC0 Data 3 | TM0 Alternate Clock 6 Notes: SPI slave select outputs require a pull-up when used.
PB_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 2 | SPT0 Channel B Data 0 | SPI0 Slave Select Output 5 | SMC0 Data 2 Notes: SPI slave select outputs require a pull-up when used.
PB_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 1 | SPT0 Channel B Frame Sync | SPI0 Slave Select Output 6 | SMC0 Data 1 | TM0 Clock Notes: SPI slave select outputs require a pull-up when used.
PB_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 0 | SPT0 Channel B Data 1 | SPI0 Data 3 | SMC0 Data 0 | SYS Power Saving Mode Wakeup 0 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Transmit | PPI0 Data 16 | SPI2 Slave Select Output 2 | SMC0 Data 8 | SYS Power Saving Mode Wakeup 1 Notes: SPI slave select outputs require a pull-up when used. If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Receive | PPI0 Data 17 | SPI2 Slave Select Output 3 | SMC0 Data 9 | TM0 Alternate Capture Input 3 Notes: SPI slave select outputs require a pull-up when used.
PB_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Clock | TRACE0 Trace Clock | SMC0 Data 10 | TM0 Alternate Clock 4 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PB_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master In, Slave Out | TRACE0 Trace Data 4 | SMC0 Data 11 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input Notes: If USB is not used, connect to ground. Active during reset
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data – Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_ID	I/O	na	none	none	none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: If USB is not used connect to ground. When USB is being used, the internal pull-up that is present during hibernate is programmable. See the USB chapter in the HRM. Active during reset.
USB0_VBC	I/O	E	none	none	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: If USB is not, used pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: If USB is not used, connect to ground.
USB0_XTAL	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Crystal Notes: No notes.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD Notes: Must be powered.
VDD_HADC	s	na	none	none	none	none	none	na	Desc: VDD for HADC Notes: If HADC is not used, connect to ground.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD Notes: Must be powered.

HADC

HADC Electrical Characteristics

Table 24. HADC Electrical Characteristics

Parameter	Test Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current Consumption on V_{DD_HADC}. HADC is powered on, but not converting.	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current Consumption on V_{DD_HADC} during a conversion.	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current Consumption on V_{DD_HADC}. Analog circuitry of the HADC is powered down	10	µA

HADC DC Accuracy

Table 25. HADC DC Accuracy

Parameter	Typ	Unit
Resolution	12	Bits
No Missing Codes (NMC)	10	Bits
Integral Nonlinearity (INL)	±2	LSB[1]
Differential Nonlinearity (DNL)	±2	LSB[1]
Offset Error	±8	LSB[1]
Offset Error Matching	±10	LSB[1]
Gain Error	±4	LSB[1]
Gain Error Matching	±4	LSB[1]

[1] LSB = HADC0_VREFP ÷ 4096

HADC Timing Specifications

Table 26. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

PACKAGE INFORMATION

The information presented in Figure 7 and Table 27 provides details about package branding. For a complete listing of product availability, see the Ordering Guide.

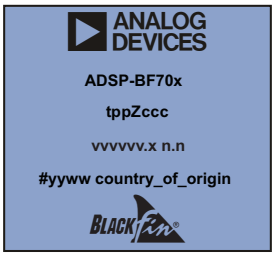


Figure 7. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 27. Package Brand Information

Brand Key	Field Description
ADSP-BF70x	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See Ordering Guide
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 28 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 28. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to +1.20 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
Real-Time Clock Supply Voltage (V_{DD_RTC})	–0.33 V to +3.60 V
Housekeeping ADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
One-Time Programmable Memory Supply Voltage (V_{DD_OTP})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V

Table 28. Absolute Maximum Ratings (Continued)

Parameter	Rating
DDR2 Reference Voltage (V_{DDR_REF})	–0.33 V to +1.90 V
Input Voltage[1, 2]	–0.33 V to +3.60 V
TWI Input Voltage[2, 3]	–0.33 V to +5.50 V
USB0_Dx Input Voltage[4]	–0.33 V to +5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to +6 V
DDR2 Input Voltage[5]	–0.33 V to +1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	4 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] Applies to balls TWI_SCL and TWI_SDA.
[4] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 38.
[5] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SMC Write Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example WST = 0x2, WAT = 0x2, and WHT = 0x1.

Table 36. SMC Write Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		ns
Switching Characteristics				
t_{DDAT}	SMC0_Dx Disable After SYS_CLKOUT		7	ns
t_{ENDAT}	SMC0_Dx Enable After SYS_CLKOUT	–2.5		ns
t_{DO}	Output Delay After SYS_CLKOUT[1]		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		ns

[1] Output pins/balls include $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$, SMC0_Ax, SMC0_Dx, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_AWE}}$.

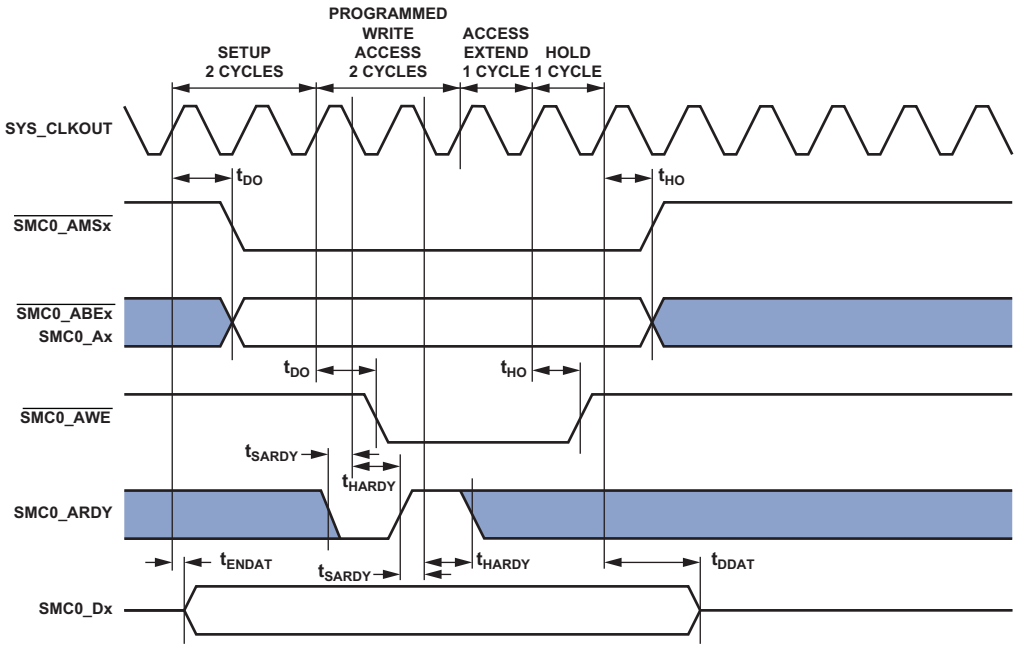


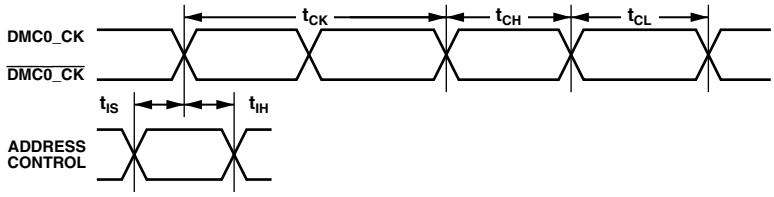
Figure 15. SMC Write Cycle Timing With Reference to SYS_CLKOUT Timing

DDR2 SDRAM Clock and Control Cycle Timing

Table 39 and Figure 17 show DDR2 SDRAM clock and control cycle timing, related to the dynamic memory controller (DMC).

Table 39. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	High Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Low Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	350		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	475		ps



NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–2.

Figure 17. DDR2 SDRAM Clock and Control Cycle Timing

DDR2 SDRAM Write Cycle Timing

Table 41 and Figure 19 show DDR2 SDRAM write cycle timing, related to the dynamic memory controller (DMC).

Table 41. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1] Min	200 MHz[1] Max	Unit
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	–0.25	+0.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.15		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.275		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Output High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Output Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

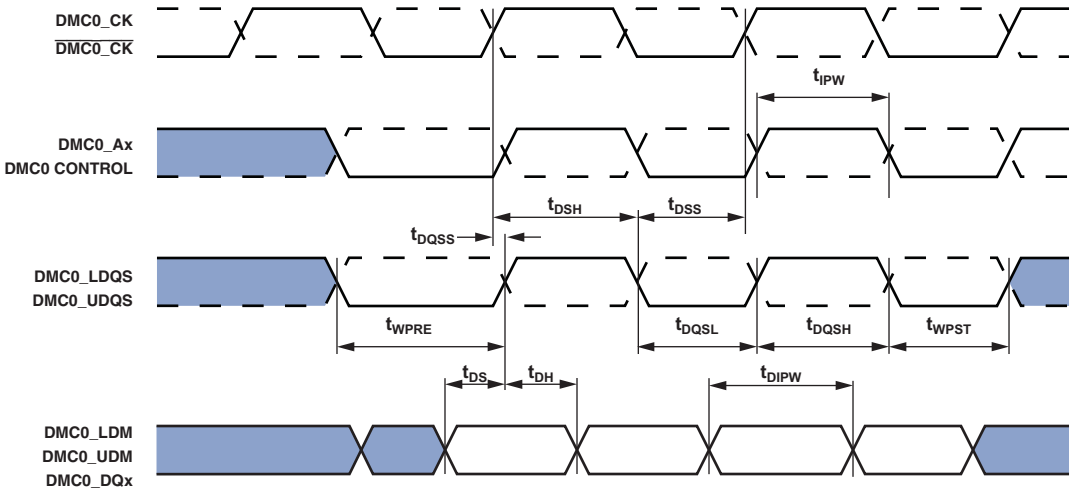


Figure 19. DDR2 SDRAM Controller Output AC Timing

Mobile DDR SDRAM Read Cycle Timing

Table 43 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 43. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz		Unit
		Min	Max	
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.5		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.7	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

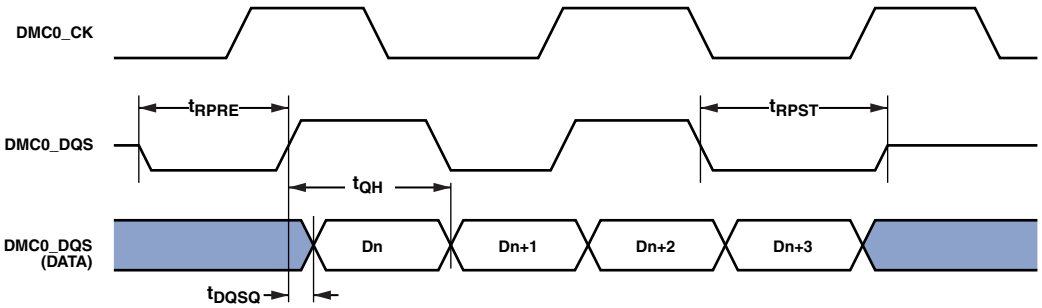


Figure 21. Mobile DDR SDRAM Controller Input AC Timing

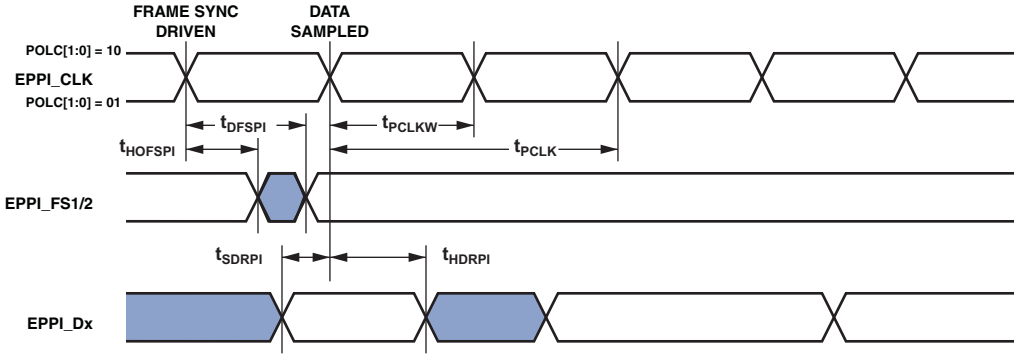


Figure 40. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

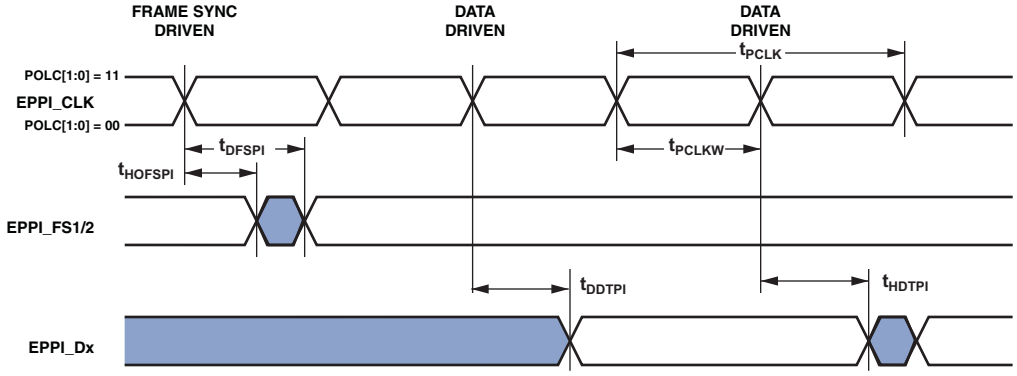


Figure 41. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

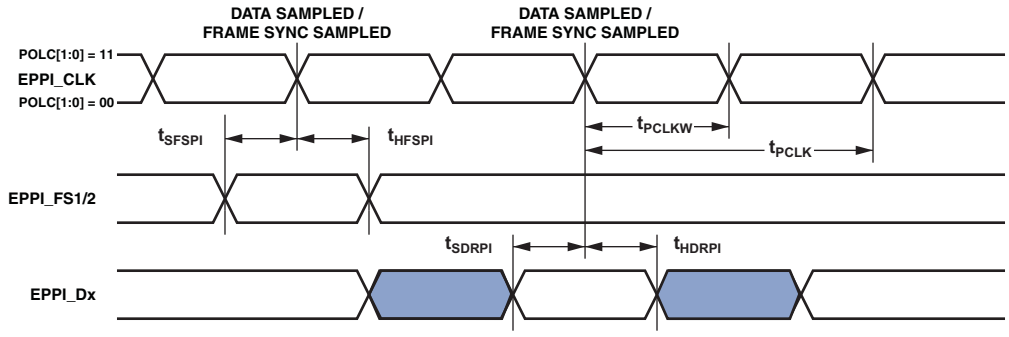


Figure 42. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

Table 68. ADSP-BF70x 184-Ball CSP_BGA Ball Assignments (Alphabetical by Signal Name)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
DMC0_A00	D01	DMC0_WE	B06	PA_08	D12	SYS_HWRST	C13
DMC0_A01	F01	GND	C08	PA_09	G12	SYS_NMI	C07
DMC0_A02	F02	GND	A01	PA_10	H12	SYS_RESOUT	J03
DMC0_A03	G01	GND	A14	PA_11	H13	SYS_XTAL	N14
DMC0_A04	D02	GND	F06	PA_12	K12	TWI0_SCL	L03
DMC0_A05	E02	GND	F07	PA_13	J12	TWI0_SDA	L02
DMC0_A06	E01	GND	F08	PA_14	P13	USB0_CLKIN	P06
DMC0_A07	B01	GND	F09	PA_15	N13	USB0_DM	P07
DMC0_A08	B02	GND	G05	PB_00	N10	USB0_DP	N07
DMC0_A09	A02	GND	G06	PB_01	M11	USB0_ID	N06
DMC0_A10	B04	GND	G07	PB_02	L12	USB0_VBC	M07
DMC0_A11	B03	GND	G08	PB_03	M12	USB0_VBUS	M06
DMC0_A12	B05	GND	G09	PB_04	M10	USB0_XTAL	P05
DMC0_A13	A08	GND	G10	PB_05	M09	VDD_DMC	D06
DMC0_BA0	A03	GND	H05	PB_06	N09	VDD_DMC	D07
DMC0_BA1	A04	GND	H06	PB_07	P08	VDD_DMC	D08
DMC0_BA2	A05	GND	H07	PB_08	N08	VDD_DMC	D09
DMC0_CAS	A06	GND	H08	PB_09	M08	VDD_DMC	E06
DMC0_CK	A10	GND	H09	PB_10	P03	VDD_DMC	E07
DMC0_CKE	B09	GND	H10	PB_11	N03	VDD_DMC	E08
DMC0_CK	A11	GND	J06	PB_12	M04	VDD_DMC	E09
DMC0_CS0	B07	GND	J07	PB_13	P02	VDD_DMC	F10
DMC0_DQ00	B10	GND	J08	PB_14	N02	VDD_DMC	F11
DMC0_DQ01	B12	GND	J09	PB_15	M03	VDD_DMC	G11
DMC0_DQ02	B11	GND	L14	PC_00	M01	VDD_DMC	H11
DMC0_DQ03	B14	GND	P01	PC_01	K02	VDD_EXT	K05
DMC0_DQ04	B13	GND	P14	PC_02	K03	VDD_EXT	K06
DMC0_DQ05	D14	GND_HADC	J10	PC_03	L01	VDD_EXT	K07
DMC0_DQ06	D13	HADC0_VIN0	P12	PC_04	K01	VDD_EXT	K08
DMC0_DQ07	E14	HADC0_VIN1	N12	PC_05	J01	VDD_EXT	K09
DMC0_DQ08	E13	HADC0_VIN2	N11	PC_06	J02	VDD_EXT	L07
DMC0_DQ09	F14	HADC0_VIN3	P11	PC_07	H01	VDD_EXT	L08
DMC0_DQ10	F13	HADC0_VREFN	P09	PC_08	G03	VDD_EXT	L09
DMC0_DQ11	G13	HADC0_VREFP	P10	PC_09	F03	VDD_HADC	K10
DMC0_DQ12	G14	JTG_TCK_SWCLK	C03	PC_10	H02	VDD_INT	E05
DMC0_DQ13	J13	JTG_TDI	E03	PC_11	N05	VDD_INT	F04
DMC0_DQ14	K14	JTG_TDO_SWO	C01	PC_12	M05	VDD_INT	F05
DMC0_DQ15	K13	JTG_TMS_SWDIO	C02	PC_13	P04	VDD_INT	G04
DMC0_LDM	M13	JTG_TRST	D03	PC_14	N04	VDD_INT	H04
DMC0_LDQS	A12	PA_00	G02	RTC0_CLKIN	M02	VDD_INT	J04
DMC0_LDQS	A13	PA_01	C04	RTC0_XTAL	N01	VDD_OTP	J11
DMC0_ODT	B08	PA_02	C06	SYS_BMODE0	E12	VDD_RTC	J05
DMC0_RAS	A07	PA_03	A09	SYS_BMODE1	C14	VDD_USB	L06
DMC0_UDM	L13	PA_04	C09	SYS_CLKIN	M14		
DMC0_UDQS	J14	PA_05	C10	SYS_CLKOUT	H03		
DMC0_UDQS	H14	PA_06	C11	SYS_EXTWAKE	C05		
DMC0_VREF	E10	PA_07	C12	SYS_FAULT	F12		