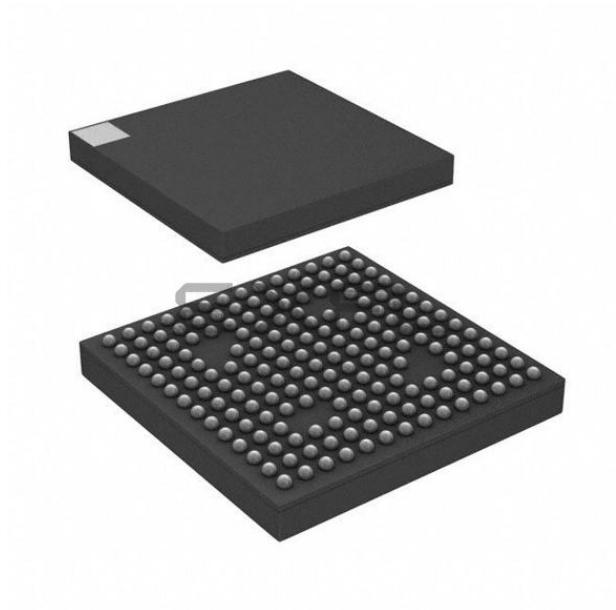

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf703bbcz-3

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system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even L3 memories (DDR2, LPDDR). The processor features two CRC engines which are embedded in the memory-to-memory DMA controllers. CRC checksums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Memory Protection

The Blackfin+ core features a memory protection concept, which grants data and/or instruction accesses to enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

The system protection unit (SPU) guards against accidental or unwanted access to the MMR space of a peripheral by providing a write-protection mechanism. The user is able to choose and configure the peripherals that are protected as well as configure which ones of the four system MMR masters (core, memory DMA, the SPI host port, and Coresight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write-protection functionality, the SPU is employed to define which resources in the system are secure or non-secure and to block access to secure resources from non-secure masters.

Synonymously, the system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are two SMPU units in the ADSP-BF70x processors. One is for the L2 memory and the other is for the external DDR memory.

The SMPU is also part of the security infrastructure. It allows the user to not only protect against arbitrary read and/or write transactions, but it also allows regions of memory to be defined as secure and prevent non-secure masters from accessing those memory regions.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or the core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the fault management unit of the SEC.

Watchdog

The on-chip software watchdog timer can supervise the Blackfin+ core.

Bandwidth Monitor

Memory-to-memory DMA channels are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the GP counter can flag this to the processor or to the fault management unit of the SEC.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a fault. Additionally, the system events can be defined as an interrupt to the core. If defined as such, the SEC forwards the event to the fault management unit, which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken through a keyed sequence, to provide a final chance for the Blackfin+ core to resolve the issue and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core through several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processor contains high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not previously described.

Timers

The processor includes several timers which are described in the following sections.

ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_FAULT	Active-Low Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Nonmaskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
UART0_CTS	UART0 Clear to Send	C	PC_03
UART0_RTS	UART0 Request to Send	C	PC_02

Table 10. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	UART1_TX	SPT0_AD1	PPI0_D15		
PC_01	UART1_RX	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	UART0_RTS	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	UART0_CTS	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	SPI1_SEL3		TM0_ACLK1
PC_11	SPT1_BFS	MSI0_D5	SPI0_SEL3		
PC_12	SPT1_BD0	MSI0_D6			
PC_13	SPT1_BD1	MSI0_D7			
PC_14	SPT1_BTDV	MSI0_INT			

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 1 | MSI0 Data 7 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Transmit Data Valid | MSI0 eSDIO Interrupt Input Notes: No notes.
RTC0_CLKIN	a	na	none	none	none	none	none	VDD_RTC	Desc: RTC0 Crystal input / external oscillator connection Notes: If RTC is not used, connect to ground.
RTC0_XTAL	a	na	none	none	none	none	none	VDD_RTC	Desc: RTC0 Crystal output Notes: No notes.
SYS_BMODE0	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 0 Notes: A pull-down is required for setting to 0 and a pull-up is required for setting to 1.
SYS_BMODE1	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Boot Mode Control 1 Notes: A pull-down is required for setting to 0 and a pull-up is required for setting to 1.
SYS_CLKIN	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Clock/Crystal Input Notes: No notes.
SYS_CLKOUT	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Processor Clock Output Notes: During reset, SYS_CLKOUT drives out SYS_CLKIN Frequency.
SYS_EXTWAKE	I/O	A	none	none	H	none	L	VDD_EXT	Desc: SYS External Wake Control Notes: Drives low during hibernate and high all other times including reset.
$\overline{\text{SYS\_FAULT}}$	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SYS Complementary Fault Output Notes: Open drain, requires an external pull-up resistor.
$\overline{\text{SYS\_HWRST}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Processor Hardware Reset Control Notes: Active during reset, must be externally driven.
$\overline{\text{SYS\_NMI}}$	I/O	na	none	none	none	none	none	VDD_EXT	Desc: SYS Non-maskable Interrupt Notes: Requires an external pull-up resistor.
$\overline{\text{SYS\_RESOUT}}$	I/O	A	none	none	L	none	none	VDD_EXT	Desc: SYS Reset Output Notes: Active during reset.
SYS_XTAL	a	na	none	none	none	none	none	VDD_EXT	Desc: SYS Crystal Output Notes: Leave unconnected if an oscillator is used to provide SYS_CLKIN. Active during reset. State during hibernate is controlled by DPM_HIB_DIS.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
VDD_OTP	s	na	none	none	none	none	none	na	Desc: VDD for OTP Notes: Must be powered.
VDD_RTC	s	na	none	none	none	none	none	na	Desc: VDD for RTC Notes: If RTC is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB Notes: If USB is not used, connect to VDD_EXT.

Table 16. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI001	1.80	1.70	1.80	1.90	V
TWI011	1.80	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 17 and Table 18 describe the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades (found in the Ordering Guide) except where expressly noted. Figure 6 provides a graphical representation of the various clocks and their available divider values.

Table 17. Core and System Clock Operating Conditions

Parameter		Ratio Restriction	PLLCLK Restriction	Min	Max	Unit
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	PLLCLK = 800		400	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	600 ≤ PLLCLK < 800		390	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	380 ≤ PLLCLK < 600		380	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SYSCLK}$	230.2 ≤ PLLCLK < 380		PLLCLK	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		PLLCLK = 800	60	200	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		600 ≤ PLLCLK < 800	60	195	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		380 ≤ PLLCLK < 600	60	190	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		230.2 ≤ PLLCLK < 380	60	PLLCLK ÷ 2	MHz
f_{SCLK0}	SCLK0 Frequency[1]	$f_{SYSCLK} \geq f_{SCLK0}$		30	100	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			200	MHz
f_{DCLK}	DDR2 Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		125	200	MHz
f_{DCLK}	LPDDR Clock Frequency	$f_{SYSCLK} \geq f_{DCLK}$		10	200	MHz

[1] The minimum frequency for SYSCLK and SCLK0 applies only when the USB is used.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OH} = –1.0 mA	0.8 × V_{DD_EXT}			V
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OH} = –2.0 mA	0.9 × V_{DD_EXT}			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 34 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –7.1 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 40 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –5.8 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 50 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –4.1 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 60 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –3.4 mA	V_{DD_DMC} – 0.320			V
V_{OH_LPDDR}[2]	High Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OH} = –2.0 mA	V_{DD_DMC} – 0.320			V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OL} = 1.0 mA			0.400	V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OL} = 2.0 mA			0.400	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 34 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 7.1 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 40 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 5.8 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 50 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 4.1 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 60 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 3.4 mA			0.320	V
V_{OL_LPDDR}[2]	Low Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OL} = 2.0 mA			0.320	V
I_{IH}[4]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
$I_{IH\_DMC0\_VREF}$[5]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			1	µA
I_{IH_PD}[6]	High Level Input Current with Pull-down Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			100	µA
R_{PD}[6]	Internal Pull-down Resistance	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V	57		130	kΩ
I_{IL}[7]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
$I_{IL\_DMC0\_VREF}$[5]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			1	µA
I_{IL_PU}[8]	Low Level Input Current with Pull-up Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			100	µA
R_{PU}[8]	Internal Pull-up Resistance	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V	53		129	kΩ
I_{IH_USB0}[9]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{IL_USB0}[9]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{OZH}[10]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{OZH}[11]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 1.9 V			10	µA
I_{OZL}[12]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{OZH_PD}[13]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			100	µA

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 29 and Figure 8 describe clock and reset operations related to the clock generation unit (CGU). Per the CCLK, SYSCLK, SCLK0, SCLK1, DCLK, and OCLK timing specifications in Table 17 on Page 51 and Table 18 on Page 52, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the processor's maximum instruction rate.

Table 29. Clock and Reset Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
f_{CKIN}	SYS_CLKIN Crystal Frequency (CGU_CTL.DF = 0)[1, 2, 3]	19.2	35	19.2	50	MHz
f_{CKIN}	SYS_CLKIN Crystal Frequency (CGU_CTL.DF = 1)[1, 2, 3]	N/A	N/A	38.4	50	MHz
f_{CKIN}	SYS_CLKIN External Source Frequency (CGU_CTL.DF = 0)[1, 2, 3]	19.2	60	19.2	60	MHz
f_{CKIN}	SYS_CLKIN External Source Frequency (CGU_CTL.DF = 1)[1, 2, 3]	38.4	60	38.4	60	MHz
t_{CKINL}	SYS_CLKIN Low Pulse[1]	8.33		8.33		ns
t_{CKINH}	SYS_CLKIN High Pulse[1]	8.33		8.33		ns
t_{WRST}	$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 8) equals $1/f_{CKIN}$.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{PLLCLK} setting discussed in Table 19.
[4] Applies after power-up sequence is complete. See Table 30 and Figure 9 for power-up reset timing.

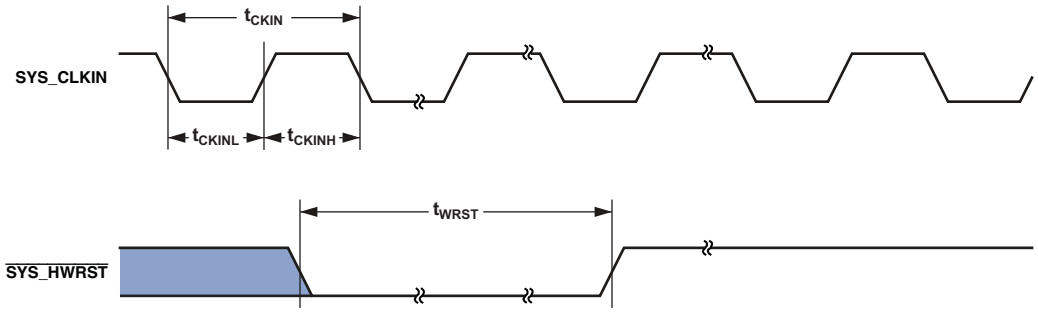


Figure 8. Clock and Reset Timing

SMC Read Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example, RST = 0x2, RAT = 0x4, and RHT = 0x1.

Table 32. SMC Read Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SDAT}	SMC0_Dx Setup Before SYS_CLKOUT	5.3		4.3		ns
t_{HDAT}	SMC0_Dx Hold After SYS_CLKOUT	1.5		1.5		ns
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	16.6		14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		0.7		ns
Switching Characteristics						
t_{DO}	Output Delay After SYS_CLKOUT[1]		7		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		–2.5		ns

[1] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_ABEx}}$.

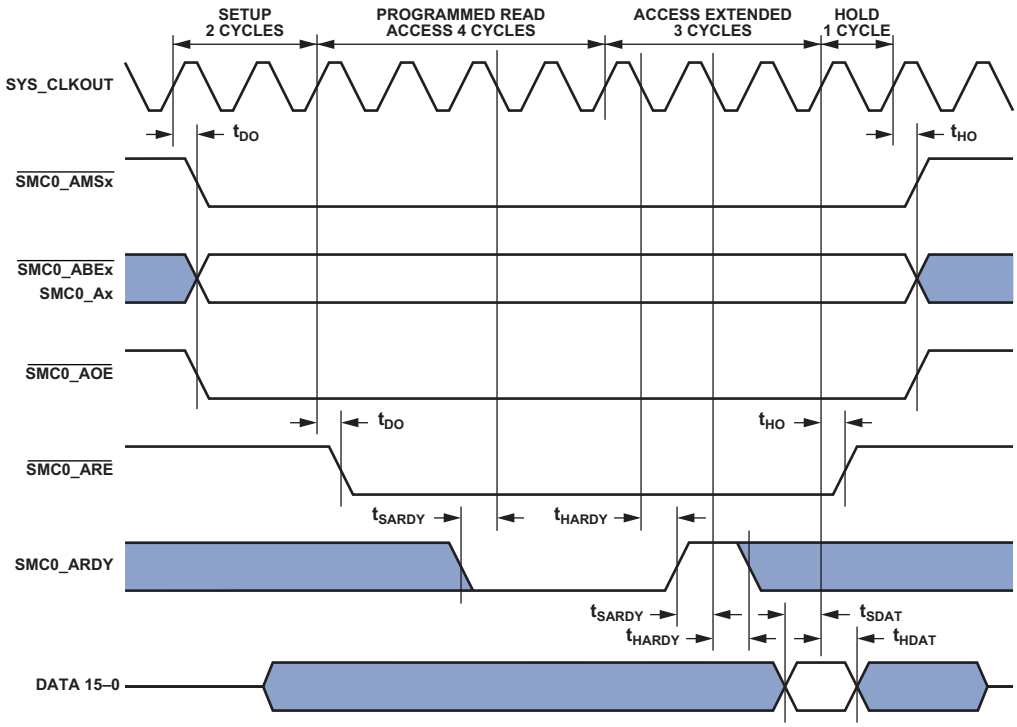


Figure 11. Asynchronous Memory Read Cycle Timing

Asynchronous Page Mode Read

Table 34 and Figure 13 show asynchronous memory page mode read timing, related to the static memory controller (SMC).

Table 34. Asynchronous Page Mode Read

Parameter		V_{DD_EXT} 1.8 V /3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{AV}	SMC0_Ax (Address) Valid for First Address Min Width[1]	(PREST + RST + PREAT + RAT) × t_{SCLK0} – 2		ns
t_{AV1}	SMC0_Ax (Address) Valid for Subsequent SMC0_Ax (Address) Min Width	PGWS × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
t_{HARE}	Output[3] Hold After $\overline{\text{SMC0\_ARE}}$ High[4]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[5]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[6]	(RAT + (Nw – 1) × PGWS) × t_{SCLK0} – 2		ns

[1] PREST, RST, PREAT and RAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$.
[4] RHT value set using the SMC_BxTIM.RHT bits.
[5] SMC_BxCTL.ARDYEN bit = 0.
[6] RAT value set using the SMC_BxTIM.RAT bits.

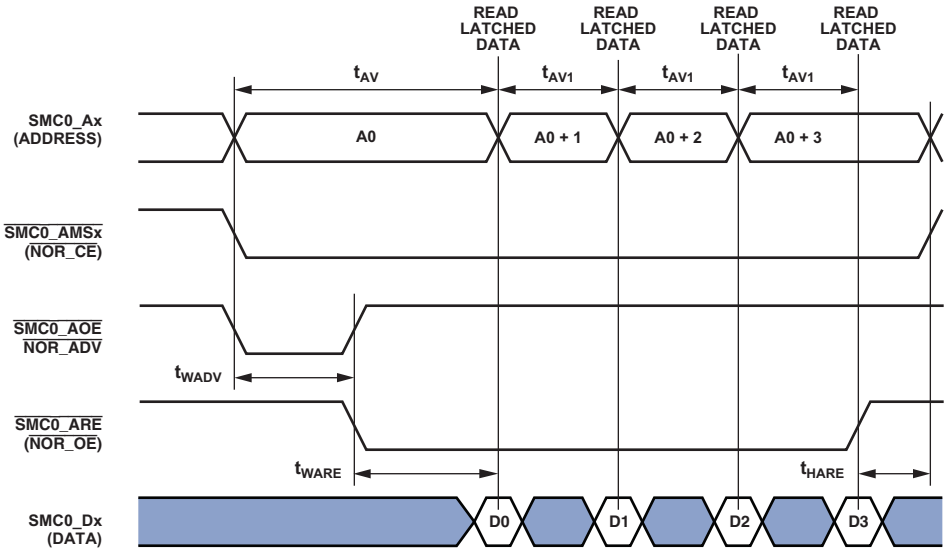


Figure 13. Asynchronous Page Mode Read

Asynchronous Write

Table 35 and Figure 14 show asynchronous memory write timing, related to the static memory controller (SMC).

Table 35. Asynchronous Memory Write (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{SMC0\_AWE}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics						
t_{ENDAT}	DATA Enable After $\overline{SMC0\_AMSx}$ Assertion	–3		–2		ns
t_{DDAT}	DATA Disable After $\overline{SMC0\_AMSx}$ Deassertion		4.5		4	ns
t_{AMSAWE}	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_AWE}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		(PREST + WST + PREAT) × t_{SCLK0} – 4		ns
t_{HAWE}	Output[4] Hold After $\overline{SMC0\_AWE}$ High[5]	WHT × t_{SCLK0}		WHT × t_{SCLK0}		ns
t_{WAWE}[6]	$\overline{SMC0\_AWE}$ Active Low Width[6]	WAT × t_{SCLK0} – 2		WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{SMC0\_AWE}$ High Delay After SMC0_ARDY Assertion		3.5 × t_{SCLK0} + 17.5		3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{SMC0\_AMSx}$, $\overline{SMC0\_ABEx}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

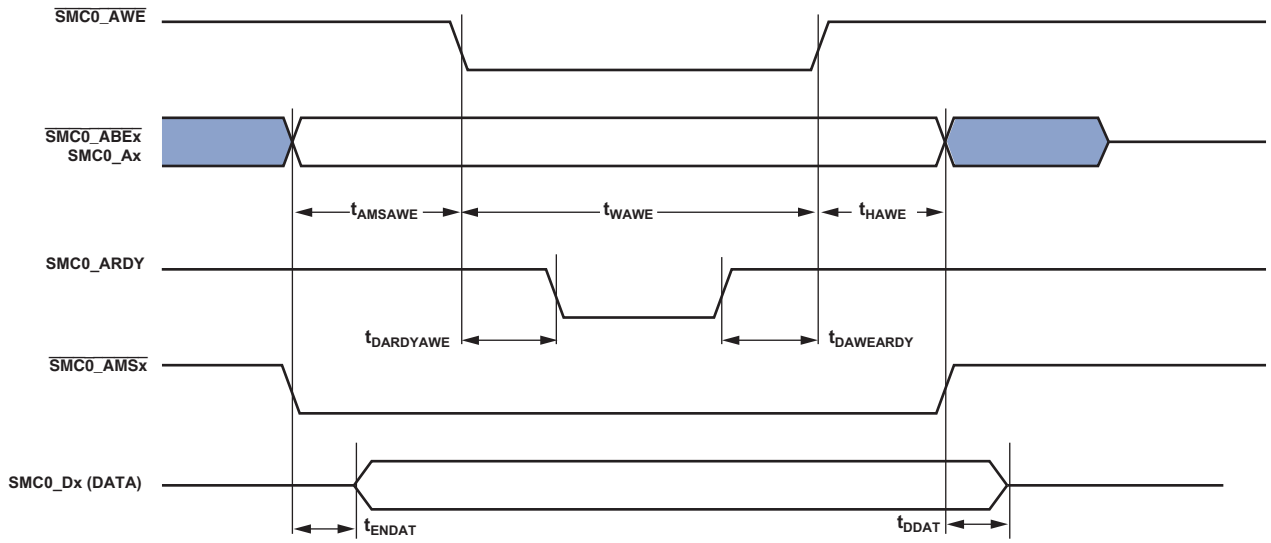


Figure 14. Asynchronous Write

Mobile DDR SDRAM Read Cycle Timing

Table 43 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 43. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz		Unit
		Min	Max	
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.5		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.7	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

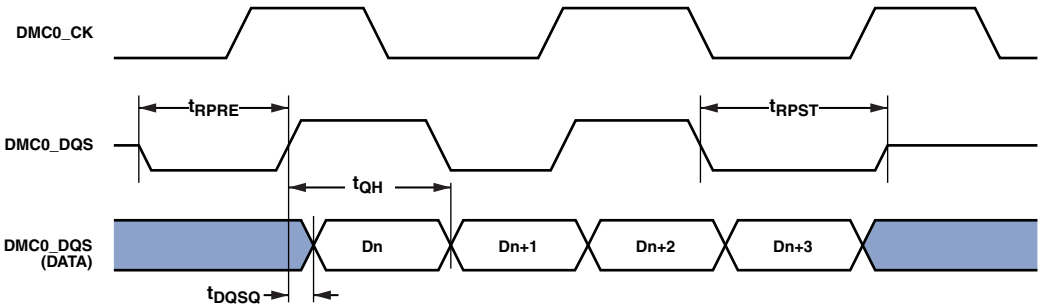


Figure 21. Mobile DDR SDRAM Controller Input AC Timing

Up/Down Counter/Rotary Encoder Timing

Table 47 and Figure 25 describe timing, related to the general-purpose counter (CNT).

Table 47. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

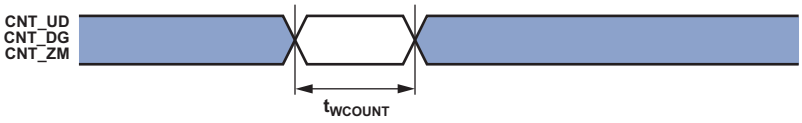


Figure 25. Up/Down Counter/Rotary Encoder Timing

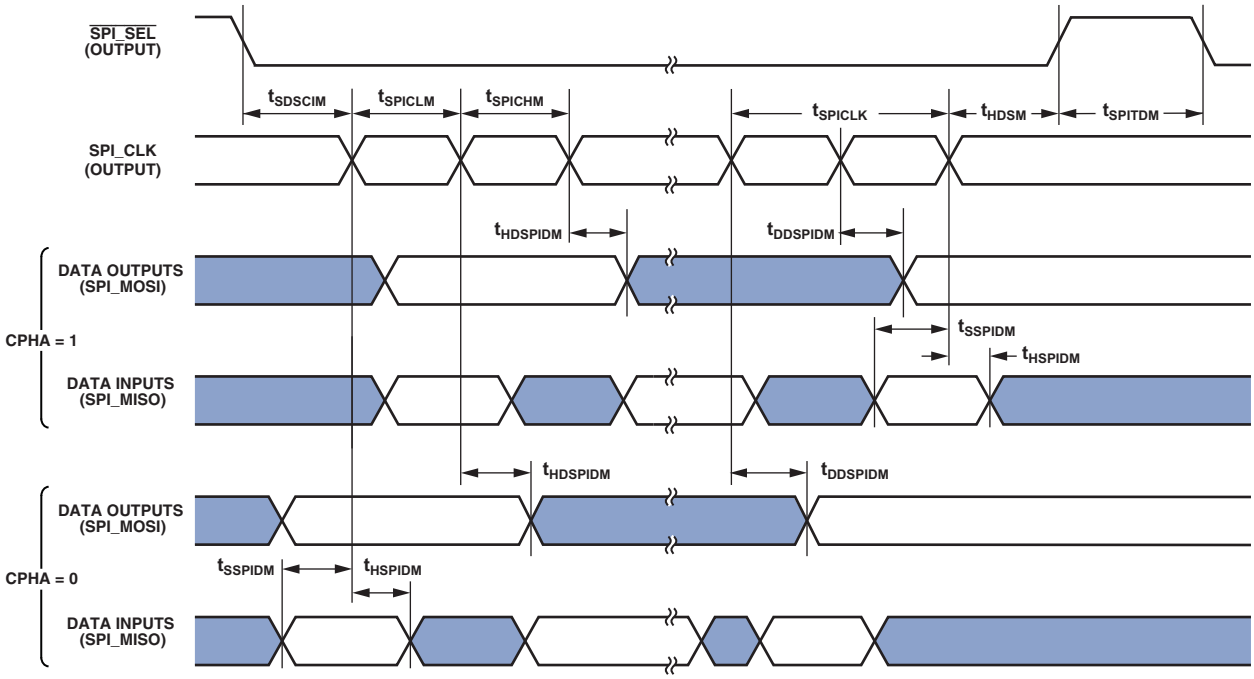


Figure 31. Serial Peripheral Interface (SPI) Port—Master Timing

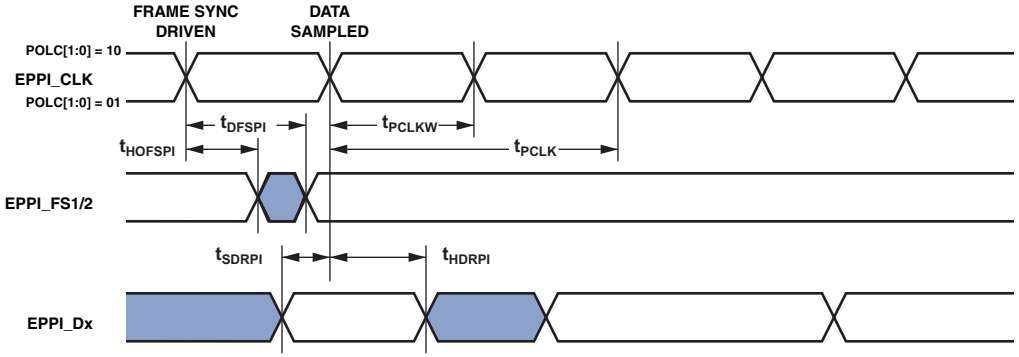


Figure 40. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

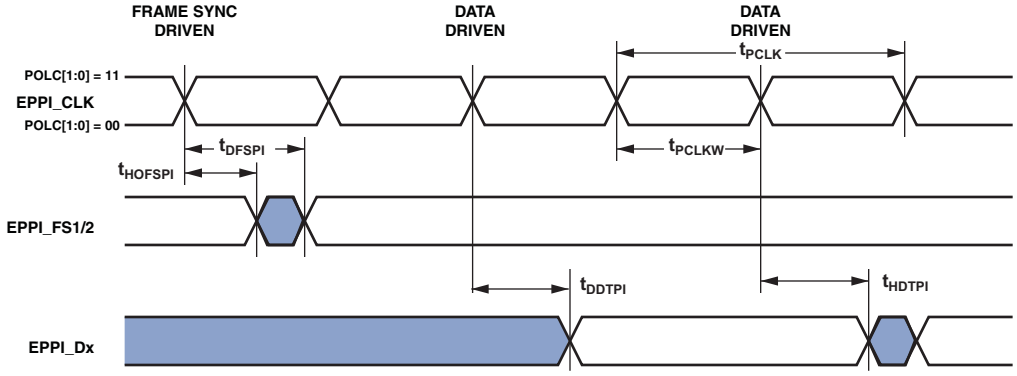


Figure 41. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

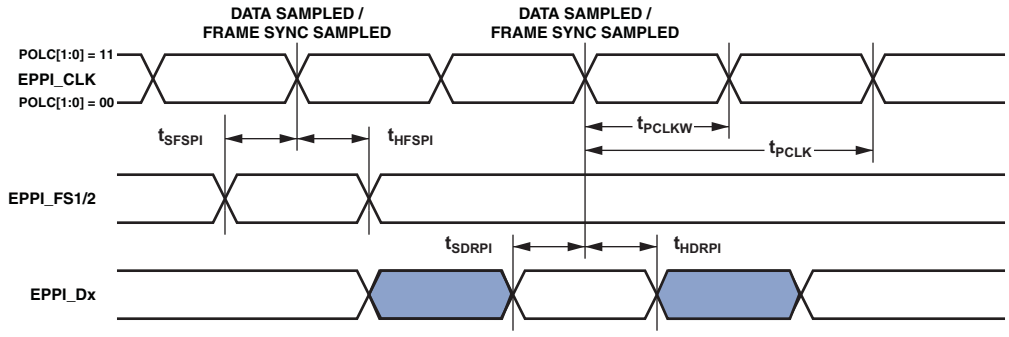
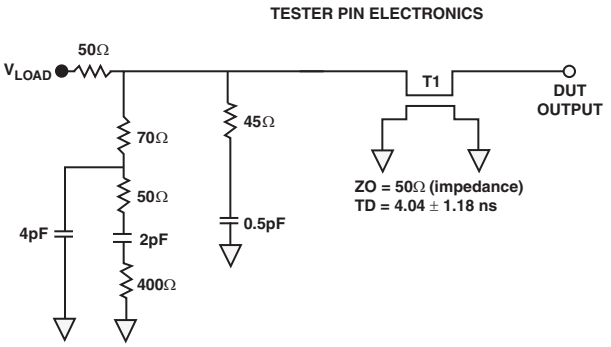


Figure 42. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 64). V_{LOAD} is equal to $V_{DD\_EXT}/2$. The graphs of Figure 65 through Figure 68 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 64. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

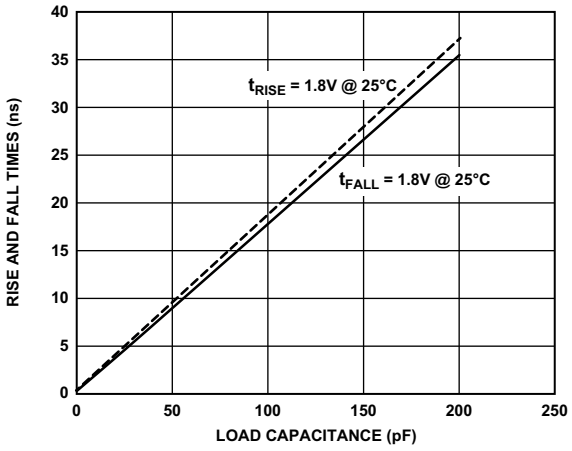


Figure 65. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 1.8 V)

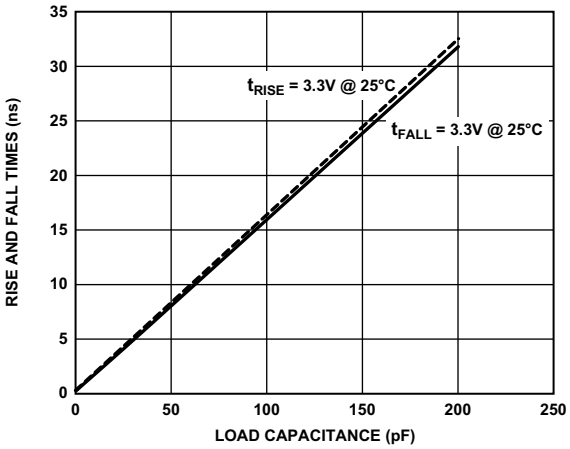


Figure 66. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

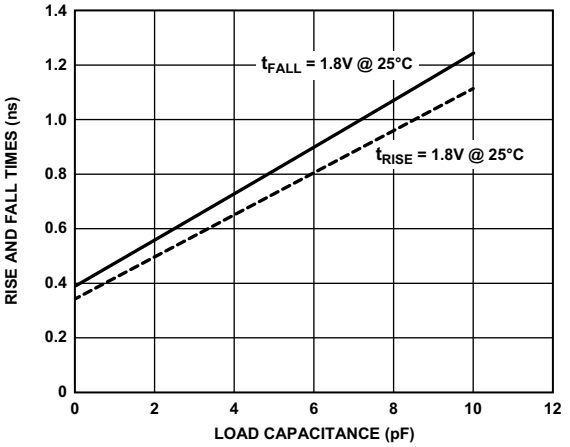


Figure 67. Driver Type B & C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V)

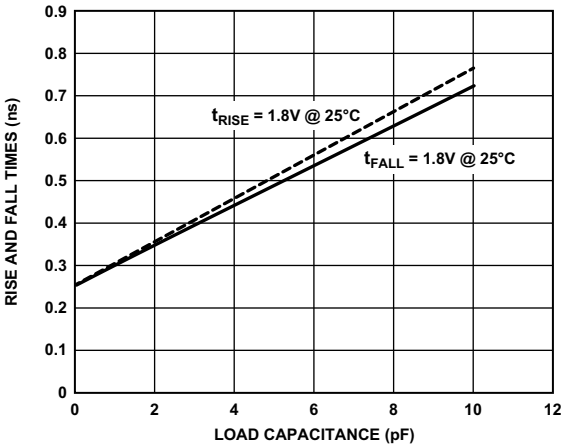


Figure 68. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for LPDDR

Table 70. ADSP-BF70x 12 mm × 12 mm 88 -Lead LFCSP (QFN) Lead Assignments (Alphabetical by Signal Name)

Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.
GND	76	PB_00	52	PC_07	5	USB0_VBUS	34
GND	89	PB_01	48	PC_08	3	USB0_XTAL	31
JTG_TCK_SWCLK	85	PB_02	47	PC_09	2	VDD_EXT	4
JTG_TDI	86	PB_03	46	PC_10	1	VDD_EXT	11
JTG_TDO_SWO	83	PB_04	45	RTC0_CLKIN	21	VDD_EXT	17
JTG_TMS_SWDIO	84	PB_05	44	RTC0_XTAL	20	VDD_EXT	26
$\overline{\text{JTG\_TRST}}$	87	PB_06	43	SYS_BMODE0	66	VDD_EXT	41
PA_00	88	PB_07	42	SYS_BMODE1	67	VDD_EXT	50
PA_01	80	PB_08	40	SYS_CLKIN	57	VDD_EXT	55
PA_02	78	PB_09	39	SYS_CLKOUT	12	VDD_EXT	62
PA_03	75	PB_10	29	SYS_EXTWAKE	79	VDD_EXT	72
PA_04	74	PB_11	28	$\overline{\text{SYS\_FAULT}}$	65	VDD_EXT	82
PA_05	73	PB_12	27	$\overline{\text{SYS\_HWRST}}$	68	VDD_INT	14
PA_06	71	PB_13	25	$\overline{\text{SYS\_NMI}}$	77	VDD_INT	30
PA_07	70	PB_14	24	$\overline{\text{SYS\_RESOUT}}$	15	VDD_INT	51
PA_08	69	PB_15	23	SYS_XTAL	56	VDD_INT	61
PA_09	64	PC_00	16	TWI0_SCL	19	VDD_INT	81
PA_10	63	PC_01	13	TWI0_SDA	18	VDD_OTP	49
PA_11	60	PC_02	10	USB0_CLKIN	32	VDD_RTC	22
PA_12	59	PC_03	9	USB0_DM	37	VDD_USB	36
PA_13	58	PC_04	8	USB0_DP	35		
PA_14	54	PC_05	7	USB0_ID	33		
PA_15	53	PC_06	6	USB0_VBC	38		

ORDERING GUIDE

Model[1]	Max. Core Clock	L2 SRAM	Temperature Grade[2]	Package Description	Package Option
ADSP-BF700KCPZ-1	100 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700KCPZ-2	200 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700BCPZ-2	200 MHz	128K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF701KBCZ-1	100 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701KBCZ-2	200 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701BBCZ-2	200 MHz	128K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF702KCPZ-3	300 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-3	300 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702KCPZ-4	400 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-4	400 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF703KBCZ-3	300 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-3	300 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703KBCZ-4	400 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-4	400 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF704KCPZ-3	300 MHz	512K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-3	300 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704KCPZ-4	400 MHz	512K bytes	0C to +70C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-4	400 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF705KBCZ-3	300 MHz	512K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-3	300 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705KBCZ-4	400 MHz	512K bytes	0C to +70C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-4	400 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF706KCPZ-3	300 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-3	300 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706KCPZ-4	400 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-4	400 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF707KBCZ-3	300 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-3	300 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707KBCZ-4	400 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-4	400 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 50 for the junction temperature (T_J) specification which is the only temperature specification.

D12396-0-9/15(A)