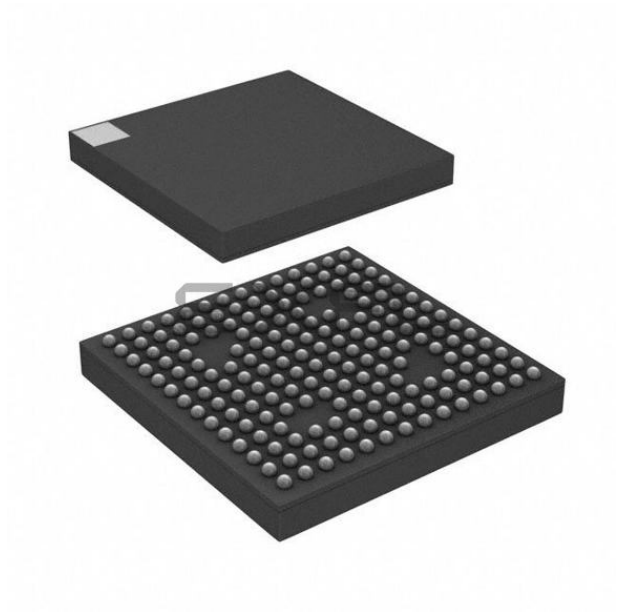


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	512kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf705bbcz-3

GENERAL DESCRIPTION

The ADSP-BF70x processor is a member of the Blackfin® family of products. The Blackfin processor combines a dual-MAC 16-bit state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture. New enhancements to the Blackfin+ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements—all while maintaining instruction set compatibility to previous Blackfin products.

The processor offers performance up to 400 MHz, as well as low static power consumption. Produced with a low-power and low-voltage design methodology, they provide world-class power management and performance.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the Blackfin processor is the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package. These applications span a wide array of markets, from automotive systems to embedded industrial, instrumentation, video/image analysis, biometric and power/motor control applications.

Table 1. Processor Comparison

Processor Feature		ADSP-BF700	ADSP-BF701	ADSP-BF702	ADSP-BF703	ADSP-BF704	ADSP-BF705	ADSP-BF706	ADSP-BF707
Maximum Speed Grade (MHz)[1]		200		400					
Maximum SYSCLK (MHz)		100		200					
Package Options		88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA
GPIOs		43	47	43	47	43	47	43	47
Memory (bytes)	L1 Instruction SRAM	48K							
	L1 Instruction SRAM/Cache	16K							
	L1 Data SRAM	32K							
	L1 Data SRAM/Cache	32K							
	L1 Scratchpad (L1 Data C)	8K							
	L2 SRAM	128K		256K		512K		1024K	
	L2 ROM	512K							
	DDR2/LPDDR (16-bit)	No	Yes	No	Yes	No	Yes	No	Yes
I^2C		1							
Up/Down/Rotary Counter		1							
GP Timer		8							
Watchdog Timer		1							
GP Counter		1							
SPORTs		2							
Quad SPI		2							
Dual SPI		1							
SPI Host Port		1							
USB 2.0 HS OTG		1							
Parallel Peripheral Interface		1							
CAN		2							
UART		2							
Real-Time Clock		1							
Static Memory Controller (SMC)		Yes							
Security Crypto Engine		Yes							
SD/SDIO (MSI)		4-bit	8-bit	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit
4-Channel 12-Bit ADC		No	Yes	No	Yes	No	Yes	No	Yes

[1] Other speed grades available.

output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

MEMORY ARCHITECTURE

The processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency core-accessible memory as cache or SRAM, and larger, lower-cost and performance interface-accessible memory systems. See Figure 3.

Internal (Core-Accessible) Memory

The L1 memory system is the highest-performance memory available to the Blackfin+ processor core.

The core has its own private L1 memory. The modified Harvard architecture supports two concurrent 32-bit data accesses along with an instruction fetch at full processor speed which provides high-bandwidth processor performance. In the core, a 64K byte block of data memory partners with an 64K byte memory block for instruction storage. Each data block is multibanked for efficient data exchange through DMA and can be configured as SRAM. Alternatively, 16K bytes of each block can be configured in L1 cache mode. The four-way set-associative instruction cache and the 2 two-way set-associative data caches greatly accelerate memory access performance, especially when accessing external memories.

The L1 memory domain also features a 8K byte data SRAM block which is ideal for storing local variables and the software stack. All L1 memory is protected by a multi-parity-bit concept, regardless of whether the memory is operating in SRAM or cache mode.

Outside of the L1 domain, L2 and L3 memories are arranged using a Von Neumann topology. The L2 memory domain is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The L2 memory domain is accessible by the Blackfin+ core through a dedicated 64-bit interface. It operates at SYSCLK frequency.

The processor features up to 1M byte of L2 SRAM, which is ECC-protected and organized in eight banks. Individual banks can be made private to any system master. There is also a 512K byte single-bank ROM in the L2 domain. It contains boot code, security code, and general-purpose ROM space.

OTP Memory

The processor features 4 kB of one-time-programmable (OTP) memory which is memory-map accessible. This memory stores a unique chip identification and is used to support secure-boot and secure operation.

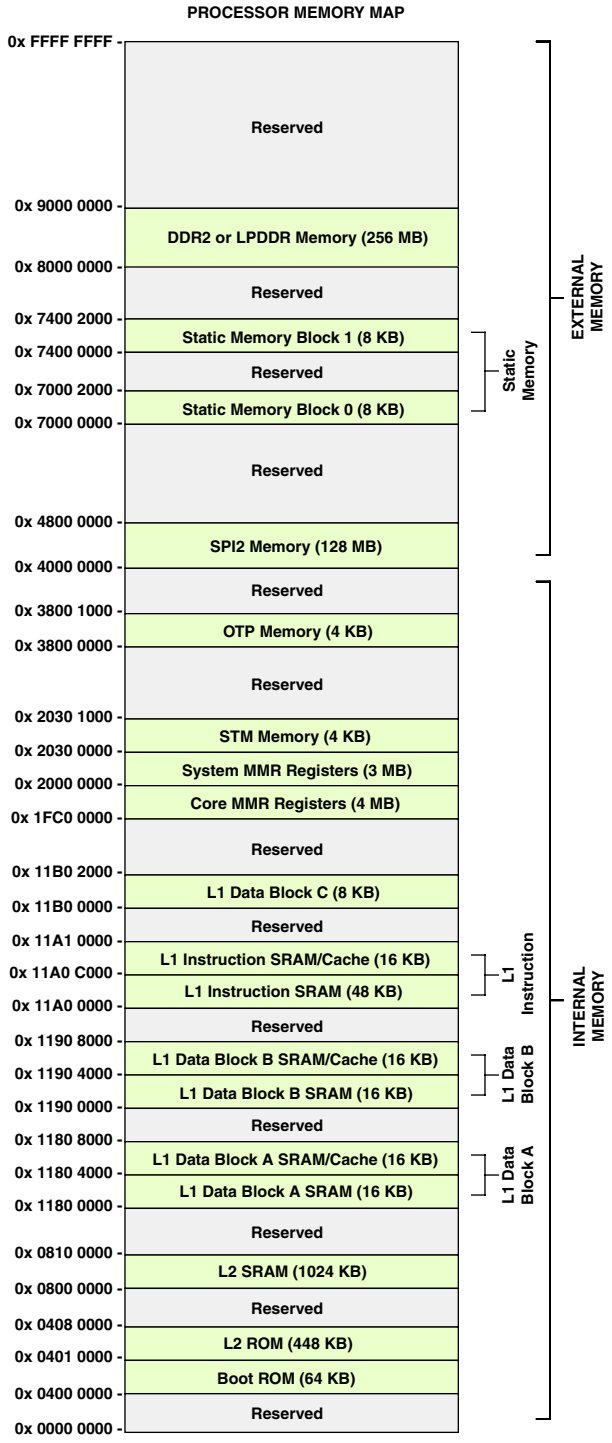


Figure 3. ADSP-BF706/ADSP-BF707 Internal/External Memory Map

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
HADC_VREFN	Input	**Ground Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
HADC_VREFP	Input	**External Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
$\overline{\text{MSI\_CD}}$	Input	**Card Detect.** Connects to a pull-up resistor and to the card detect output of an SD socket.
MSI_CLK	Output	**Clock.** The clock signal applied to the connected device from the MSI.
MSI_CMD	I/O	**Command.** Used to send commands to and receive responses from the connected device.
MSI_Dn	I/O	**Data n.** Bidirectional data bus.
$\overline{\text{MSI\_INT}}$	Input	**eSDIO Interrupt Input.** Used only for eSDIO. Connects to an eSDIO card's interrupt output. An interrupt may be sampled even when the MSI clock to the card is switched off.
Px_nn	I/O	**Position n.** General purpose input/output. See the GP Ports chapter of the HRM for programming information.
RTC_CLKIN	Input	**Crystal input/external oscillator connection.** Connect to an external clock source or crystal.
RTC_XTAL	Output	**Crystal output.** Drives an external crystal. Must be left unconnected if an external clock is driving RTC_CLKIN.
$\overline{\text{SMC\_ABEn}}$	Output	**Byte Enable n.** Indicate whether the lower or upper byte of a memory is being accessed. When an asynchronous write is made to the upper byte of a 16-bit memory, SMC_ABE1b=0 and SMC_ABE0b=1. When an asynchronous write is made to the lower byte of a 16-bit memory, SMC_ABE1b=1 and SMC_ABE0b=0.
$\overline{\text{SMC\_AMSn}}$	Output	**Memory Select n.** Typically connects to the chip select of a memory device.
$\overline{\text{SMC\_AOE}}$	Output	**Output Enable.** Asserts at the beginning of the setup period of a read access.
SMC_ARDY	Input	**Asynchronous Ready.** Flow control signal used by memory devices to indicate to the SMC when further transactions may proceed.
$\overline{\text{SMC\_ARE}}$	Output	**Read Enable.** Asserts at the beginning of a read access.
$\overline{\text{SMC\_AWE}}$	Output	**Write Enable.** Asserts for the duration of a write access period.
SMC_Ann	Output	**Address n.** Address bus.
SMC_Dnn	I/O	**Data n.** Bidirectional data bus.
SPI_CLK	I/O	**Clock.** Input in slave mode, output in master mode.
SPI_D2	I/O	**Data 2.** Used to transfer serial data in Quad mode. Open-drain when ODM mode is enabled.
SPI_D3	I/O	**Data 3.** Used to transfer serial data in Quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	I/O	**Master In, Slave Out.** Used to transfer serial data. Operates in the same direction as SPI_MOSI in Dual and Quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	I/O	**Master Out, Slave In.** Used to transfer serial data. Operates in the same direction as SPI_MISO in Dual and Quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	I/O	**Ready.** Optional flow signal. Output in slave mode, input in master mode.
$\overline{\text{SPI\_SELn}}$	Output	**Slave Select Output n.** Used in Master mode to enable the desired slave.
$\overline{\text{SPI\_SS}}$	Input	**Slave Select Input.** Slave mode - Acts as the slave select input. Master mode- Optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	I/O	**Channel A Clock.** Data and Frame Sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	I/O	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AD1	I/O	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_AFS	I/O	**Channel A Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
SPT_BCLK	I/O	**Channel B Clock.** Data and Frame Sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BD1	I/O	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BFS	I/O	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SYS_BMODEn	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN	Input	**Clock/Crystal Input.** Connect to an external clock source or crystal.
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the HRM for more details.
SYS_EXTWAKE	Output	**External Wake Control.** Drives low during hibernate and high all other times. Typically connected to the enable input of the voltage regulator controlling the VDD_INT supply.
$\overline{\text{SYS\_FAULT}}$	I/O	**Active-Low Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_NMI}}$	Input	**Non-maskable Interrupt.** See the processor hardware and programming references for more details.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates that the device is in the reset or hibernate state.
SYS_WAKEn	Input	**Power Saving Mode Wakeup n.** Wake-up source input for deep sleep and/or hibernate mode.
SYS_XTAL	Output	**Crystal Output.** Drives an external crystal. Must be left unconnected if an external clock is driving CLKIN.
JTG_SWCLK	I/O	**Serial Wire Clock.** Clocks data into and out of the target during debug.
JTG_SWDIO	I/O	**Serial Wire DIO.** Sends and receives serial data to and from the target during debug.
JTG_SWO	Output	**Serial Wire Out.** Provides trace data to the emulator.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
TM_ACIn	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLKn	Input	**Alternate Clock n.** Provides an additional time base for use by an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for use by all the GP timers.
TM_TMRn	I/O	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_Dnn	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	I/O	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	I/O	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receive input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmit output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input.** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0\_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0\_LDQS}}$
DMC0_ODT	DMC0 On-die termination	Not Muxed	DMC0_ODT
$\overline{\text{DMC0\_RAS}}$	DMC0 Row Address Strobe	Not Muxed	$\overline{\text{DMC0\_RAS}}$
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
$\overline{\text{DMC0\_UDQS}}$	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	$\overline{\text{DMC0\_UDQS}}$
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
$\overline{\text{DMC0\_WE}}$	DMC0 Write Enable	Not Muxed	$\overline{\text{DMC0\_WE}}$
GND	Ground	Not Muxed	GND
GND_HADC	Ground HADC	Not Muxed	GND_HADC
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG\_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
MSI0_D5	MSI0 Data 5	C	PC_11
MSI0_D6	MSI0 Data 6	C	PC_12
MSI0_D7	MSI0 Data 7	C	PC_13

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 3 | SPT0 Channel B Clock | SPI0 Slave Select Output 4 | SMC0 Data 3 | TM0 Alternate Clock 6 Notes: SPI slave select outputs require a pull-up when used.
PB_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 2 | SPT0 Channel B Data 0 | SPI0 Slave Select Output 5 | SMC0 Data 2 Notes: SPI slave select outputs require a pull-up when used.
PB_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 1 | SPT0 Channel B Frame Sync | SPI0 Slave Select Output 6 | SMC0 Data 1 | TM0 Clock Notes: SPI slave select outputs require a pull-up when used.
PB_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 0 | SPT0 Channel B Data 1 | SPI0 Data 3 | SMC0 Data 0 | SYS Power Saving Mode Wakeup 0 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Transmit | PPI0 Data 16 | SPI2 Slave Select Output 2 | SMC0 Data 8 | SYS Power Saving Mode Wakeup 1 Notes: SPI slave select outputs require a pull-up when used. If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Receive | PPI0 Data 17 | SPI2 Slave Select Output 3 | SMC0 Data 9 | TM0 Alternate Capture Input 3 Notes: SPI slave select outputs require a pull-up when used.
PB_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Clock | TRACE0 Trace Clock | SMC0 Data 10 | TM0 Alternate Clock 4 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PB_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master In, Slave Out | TRACE0 Trace Data 4 | SMC0 Data 11 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master Out, Slave In | TRACE0 Trace Data 3 | SMC0 Data 12 | SYS Power Saving Mode Wakeup 2 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 2 | UART1 Request to Send | TRACE0 Trace Data 2 | SMC0 Data 13 Notes: No notes.
PB_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 3 | UART1 Clear to Send | TRACE0 Trace Data 1 | SMC0 Data 14 Notes: No notes.
PB_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Slave Select Output 1 | TRACE0 Trace Data 0 | SMC0 Data 15 | SPI2 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PC_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Transmit | SPT0 Channel A Data 1 | PPI0 Data 15 Notes: No notes.
PC_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Receive | SPT0 Channel B Data 1 | PPI0 Data 14 | SMC0 Address 9 | TM0 Alternate Capture Input 4 Notes: No notes.
PC_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Request to Send | CAN0 Receive | PPI0 Data 13 | SMC0 Address 10 | SYS Power Saving Mode Wakeup 3 | TM0 Alternate Capture Input 5 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PC_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Clear to Send | CAN0 Transmit | PPI0 Data 12 | SMC0 Address 11 | TM0 Alternate Capture Input 0 Notes: No notes.
PC_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Clock | SPI0 Clock | MSI0 Data 1 | SMC0 Address 12 | TM0 Alternate Clock 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Internal Supply Voltage	CCLK ≤ 400 MHz	1.045	1.100	1.155	V
V_{DD_EXT}[1]	External Supply Voltage		1.7	1.8	1.9	V
V_{DD_EXT}[1]	External Supply Voltage		3.13	3.30	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.30	3.47	V
V_{DD_RTC}	Real-Time Clock Supply Voltage		2.00	3.30	3.47	V
V_{DD_HADC}	Housekeeping ADC Supply Voltage		3.13	3.30	3.47	V
V_{DD_OTP}[1]	OTP Supply Voltage					
	For Reads		2.25	3.30	3.47	V
	For Writes		3.13	3.30	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 1.9 V	0.7 × V_{DD_EXT}			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = maximum	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[7]		V_{DD_DMC} = 1.9 V	V_{DDR_REF} + 0.25			V
V_{IH_LPDDR}[8]		V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 1.075 V	0.50			V
V_{ID_DDR2}[9]	Differential Input Voltage	V_{IX} = 0.725 V	0.55			V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 1.7 V			0.3 × V_{DD_EXT}	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = minimum			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7]		V_{DD_DMC} = 1.7 V			V_{DDR_REF} – 0.25	V
V_{IL_LPDDR}[8]		V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0°C to +70°C	0		105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] If not used, connect to 1.8 V or 3.3 V.
[3] V_{HADC_VREF} should always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional signals except RTC signals, TWI signals, DMC0 signals, and USB0 signals.
[5] Parameter applies to TWI signals.
[6] TWI signals are pulled up to V_{BUSTWI}. See Table 16.
[7] Parameter applies to DMC0 signals in DDR2 mode.
[8] Parameter applies to DMC0 signals in LPDDR mode.
[9] Parameter applies to signals DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$ when used in DDR2 differential input mode.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
I_{OZH_TWI}[14]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 5.5 V			10	µA
ADSP-BF701/703/705/707 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.2	6.0	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.9	7.4	pF
C_{IN_DDR}[16]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.1	6.9	pF
ADSP-BF700/702/704/706 Input Capacitance						
C_{IN} (GPIO)[15]	Input Capacitance	$T_{AMBIENT}$ = 25°C		5.0	5.3	pF
C_{IN_TWI}[14]	Input Capacitance	$T_{AMBIENT}$ = 25°C		6.8	7.4	pF
$I_{DD\_DEEPSLEEP}$[17, 18]	V_{DD_INT} Current in Deep Sleep Mode	Clocks disabled T_J = 25°C		1.4		mA
I_{DD_IDLE}[18]	V_{DD_INT} Current in Idle	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 0.05 (idle) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		13		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 800 MHz f_{CCLK} = 400 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		90		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 300 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		66		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 400 MHz f_{CCLK} = 200 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		49		mA
I_{DD_TYP}[18]	V_{DD_INT} Current	f_{PLLCLK} = 300 MHz f_{CCLK} = 100 MHz ASF = 1.0 (full-on typical) f_{SYSCLK} = f_{SCLK0} = 25 MHz USBCLK = DCLK = OUTCLK = SCLK1 = DISABLED Peripherals disabled T_J = 25°C		30		mA

PACKAGE INFORMATION

The information presented in Figure 7 and Table 27 provides details about package branding. For a complete listing of product availability, see the Ordering Guide.

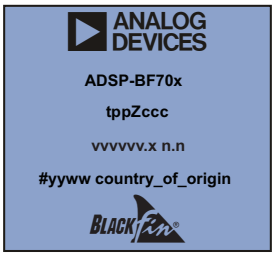


Figure 7. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 27. Package Brand Information

Brand Key	Field Description
ADSP-BF70x	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See Ordering Guide
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 28 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 28. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to +1.20 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
Real-Time Clock Supply Voltage (V_{DD_RTC})	–0.33 V to +3.60 V
Housekeeping ADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
One-Time Programmable Memory Supply Voltage (V_{DD_OTP})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V

Table 28. Absolute Maximum Ratings (Continued)

Parameter	Rating
DDR2 Reference Voltage (V_{DDR_REF})	–0.33 V to +1.90 V
Input Voltage[1, 2]	–0.33 V to +3.60 V
TWI Input Voltage[2, 3]	–0.33 V to +5.50 V
USB0_Dx Input Voltage[4]	–0.33 V to +5.25 V
USB0_VBUS Input Voltage[5]	–0.33 V to +6 V
DDR2 Input Voltage[5]	–0.33 V to +1.90 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
I_{OH}/I_{OL} Current per Signal[1]	4 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies to 100% transient duty cycle.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] Applies to balls TWI_SCL and TWI_SDA.
[4] If the USB is not used, connect USB0_Dx and USB0_VBUS according to Table 15 on Page 38.
[5] Applies only when V_{DD_DMC} is within specifications. When V_{DD_DMC} is outside specifications, the range is V_{DD_DMC} ± 0.2 V.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Power-Up Reset Timing

A power-up reset is required to place the processor in a known state after power-up. A power-up reset is initiated by asserting $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$. During power-up reset, all pins are high impedance except for those noted in the ADSP-BF70x Designer Quick Reference on Page 38.

Both $\overline{\text{JTG\_TRST}}$ and $\overline{\text{SYS\_HWRST}}$ need to be asserted upon power-up, but only $\overline{\text{SYS\_HWRST}}$ needs to be released for the device to boot properly. $\overline{\text{JTG\_TRST}}$ may be asserted indefinitely for normal operation. $\overline{\text{JTG\_TRST}}$ only needs to be released when using an emulator to connect to the DAP for debug or boundary scan. There is an internal pull-down on $\overline{\text{JTG\_TRST}}$ to ensure internal emulation logic will always be properly initialized during power-up reset.

Table 30 and Figure 9 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU). In Figure 9, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, and V_{DD_HADC}.

There is no power supply sequencing requirement for the ADSP-BF70x processor. However, if saving power during power-on is important, bringing up V_{DD_INT} last is recommended. This avoids a small current drain in the V_{DD_INT} domain during the transition period of I/O voltages from 0 V to within the voltage specification.

Table 30. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ Deasserted After V_{DD_INT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, V_{DD_HADC}, and SYS_CLKIN are Stable and Within Specification	$11 \times t_{CKIN}$		ns
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (No External Pull-Down on $\overline{\text{JTG\_TRST}}$)	10		µs
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (10k External Pull-Down on $\overline{\text{JTG\_TRST}}$)	1		µs

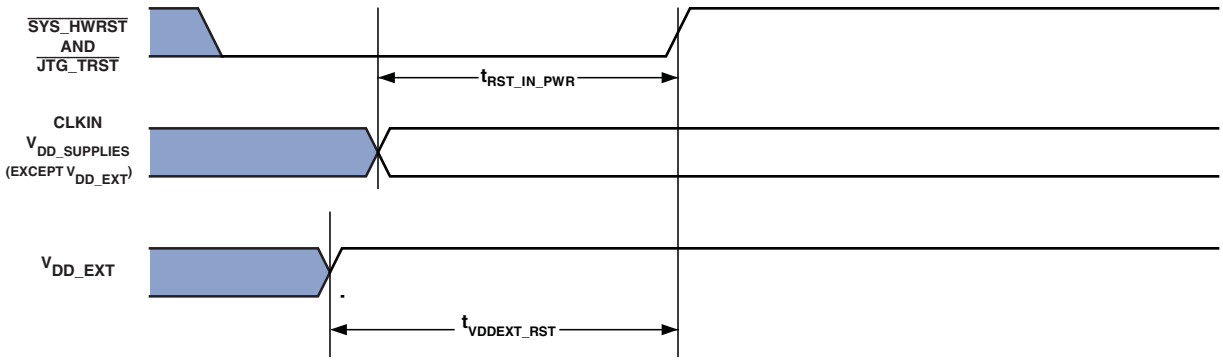


Figure 9. Power-Up Reset Timing

SMC Read Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example, RST = 0x2, RAT = 0x4, and RHT = 0x1.

Table 32. SMC Read Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SDAT}	SMC0_Dx Setup Before SYS_CLKOUT	5.3		4.3		ns
t_{HDAT}	SMC0_Dx Hold After SYS_CLKOUT	1.5		1.5		ns
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	16.6		14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		0.7		ns
Switching Characteristics						
t_{DO}	Output Delay After SYS_CLKOUT[1]		7		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		–2.5		ns

[1] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_ABEx}}$.

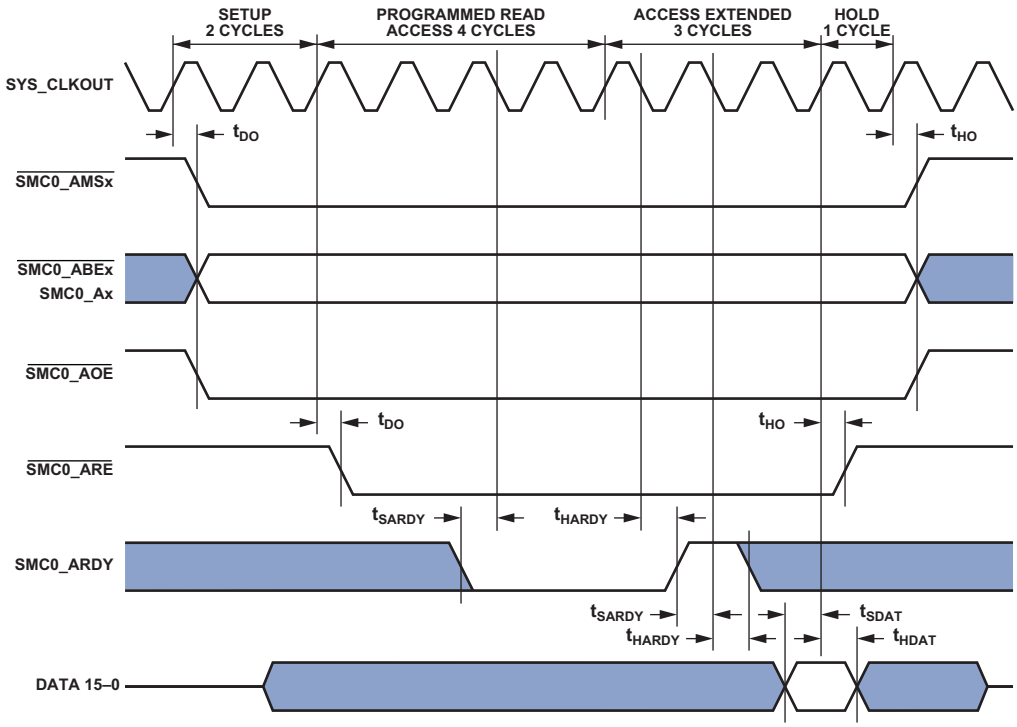


Figure 11. Asynchronous Memory Read Cycle Timing

Asynchronous Write

Table 35 and Figure 14 show asynchronous memory write timing, related to the static memory controller (SMC).

Table 35. Asynchronous Memory Write (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{SMC0\_AWE}$ Low[2]		(WAT – 2.5) × t_{SCLK0} – 17.5		(WAT – 2.5) × t_{SCLK0} – 17.5	ns
Switching Characteristics						
t_{ENDAT}	DATA Enable After $\overline{SMC0\_AMSx}$ Assertion	–3		–2		ns
t_{DDAT}	DATA Disable After $\overline{SMC0\_AMSx}$ Deassertion		4.5		4	ns
t_{AMSAWE}	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_AWE}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK0} – 2		(PREST + WST + PREAT) × t_{SCLK0} – 4		ns
t_{HAWE}	Output[4] Hold After $\overline{SMC0\_AWE}$ High[5]	WHT × t_{SCLK0}		WHT × t_{SCLK0}		ns
t_{WAWE}[6]	$\overline{SMC0\_AWE}$ Active Low Width[6]	WAT × t_{SCLK0} – 2		WAT × t_{SCLK0} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{SMC0\_AWE}$ High Delay After SMC0_ARDY Assertion		3.5 × t_{SCLK0} + 17.5		3.5 × t_{SCLK0} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{SMC0\_AMSx}$, $\overline{SMC0\_ABEx}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

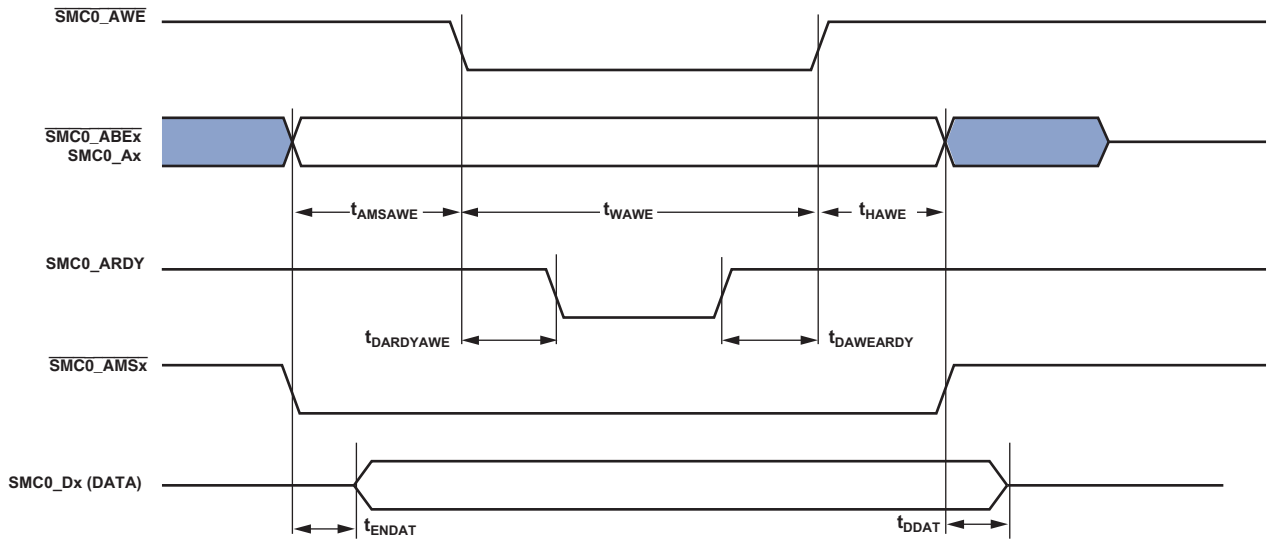


Figure 14. Asynchronous Write

DDR2 SDRAM Read Cycle Timing

Table 40 and Figure 18 show DDR2 SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 40. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1] Min	Max	Unit
Timing Requirements				
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.35	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.8		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.

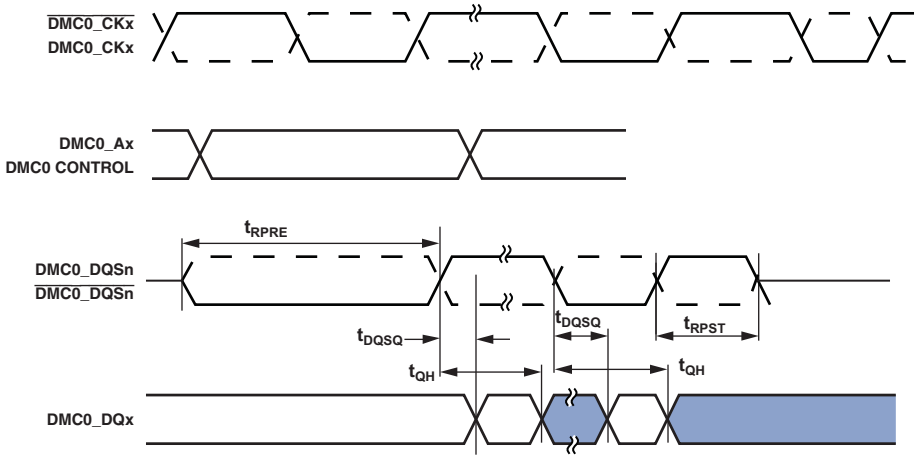


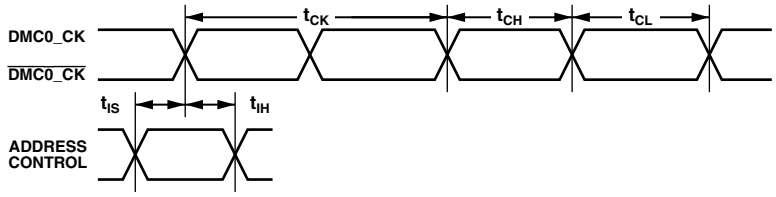
Figure 18. DDR2 SDRAM Controller Input AC Timing

Mobile DDR SDRAM Clock and Control Cycle Timing

Table 42 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the dynamic memory controller (DMC).

Table 42. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1.5		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1.5		ns



NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–2.

Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

Serial Ports

To determine whether serial port (SPORT) communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SPT_CLK) width. In Figure 27 either the rising edge or the falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65,535:

$$f_{SPTCLKPROG} = \frac{f_{SCLK0}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 49. Serial Ports—External Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[1]	1.5		1		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[1]	3		3		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	1.5		1		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	3		3		ns
t_{SCLKW}	SPT_CLK Width[2]	$(0.5 \times t_{SPTCLKEXT}) - 1$		$(0.5 \times t_{SPTCLKEXT}) - 1$		ns
$t_{SPTCLKE}$	SPT_CLK Period[2]	$t_{SPTCLKEXT} - 1$		$t_{SPTCLKEXT} - 1$		ns
Switching Characteristics						
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[3]		18		15	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[3]	2.5		2.5		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		18		15	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	2.5		2.5		ns

[1] Referenced to sample edge.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK. For the external SPT_CLK ideal maximum frequency, see the $f_{SPTCLKEXT}$ specification in Table 18 on Page 52 in Clock Related Operating Conditions.

[3] Referenced to drive edge.

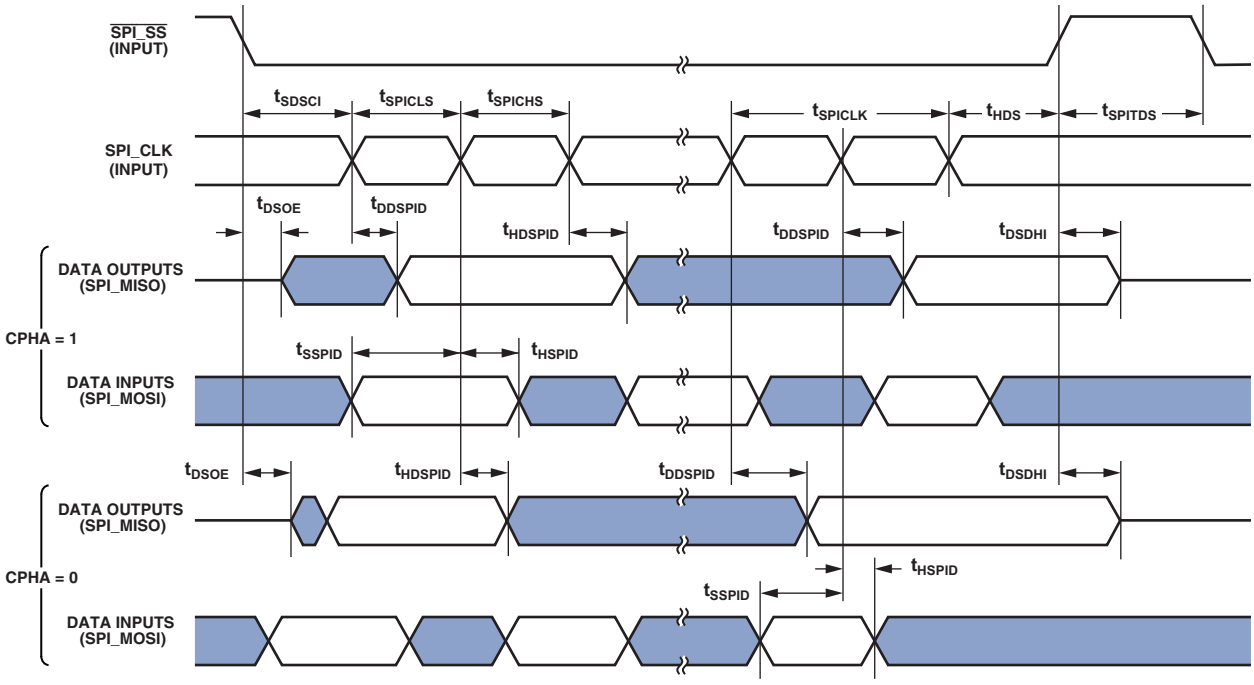


Figure 32. Serial Peripheral Interface (SPI) Port—Slave Timing

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

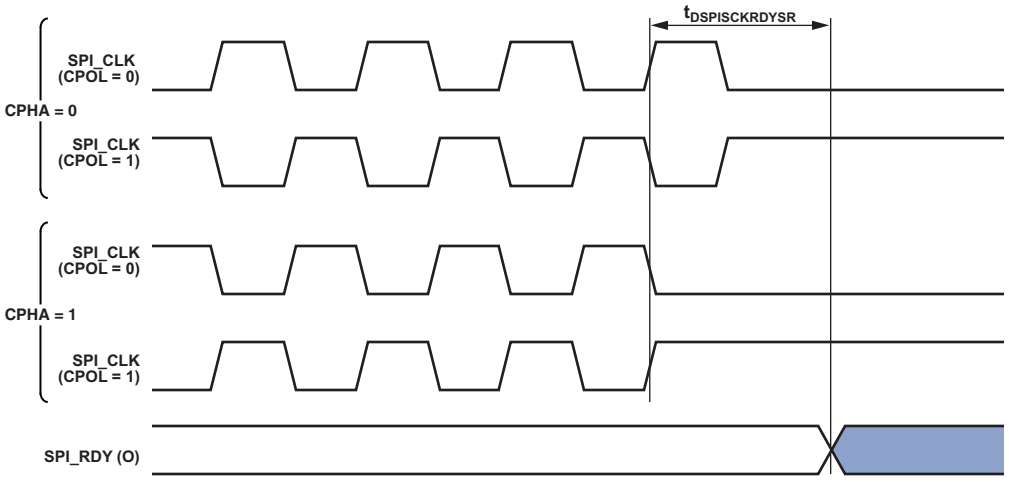


Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

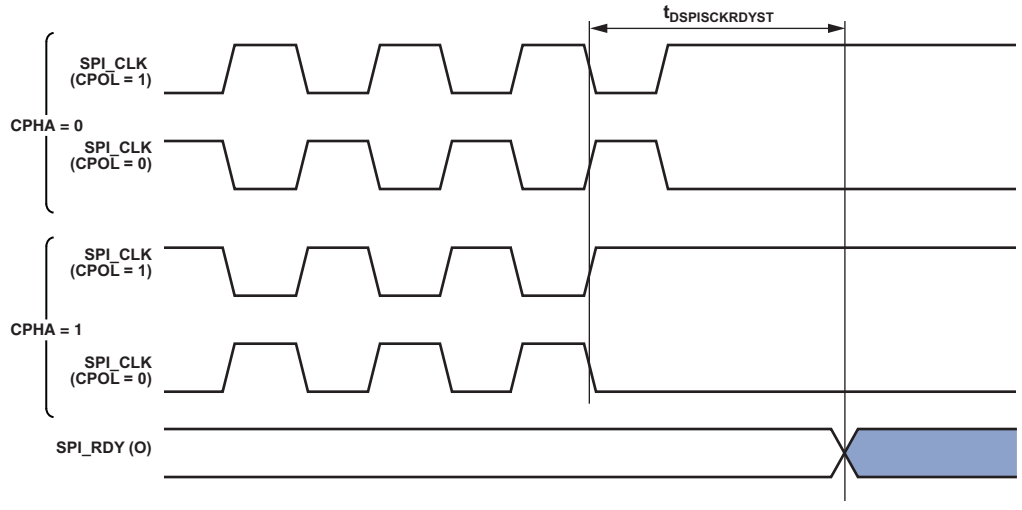


Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

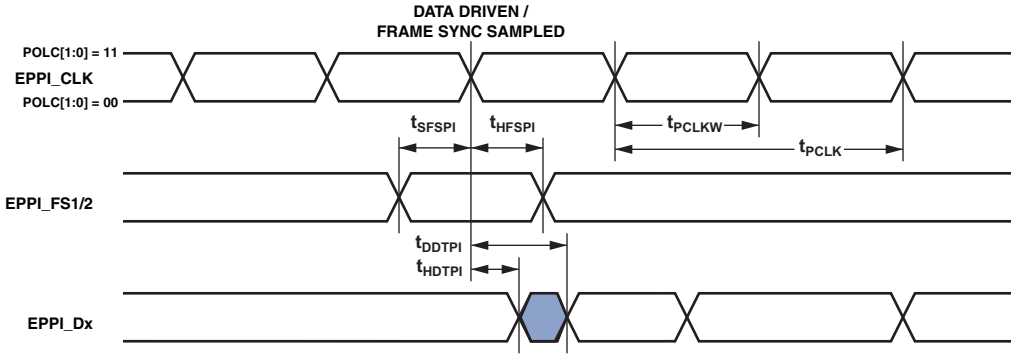


Figure 43. PPI Internal Clock GP Transmit Mode with External Frame Sync Timing

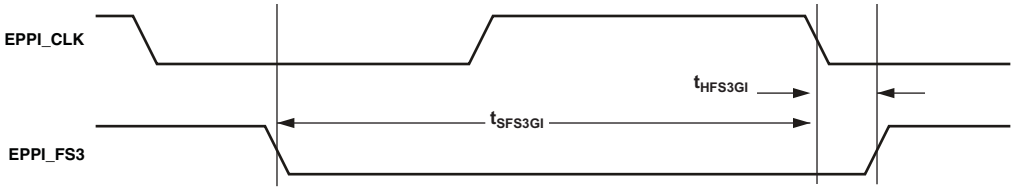


Figure 44. Clock Gating Mode with Internal Clock and External Frame Sync Timing

ORDERING GUIDE

Model[1]	Max. Core Clock	L2 SRAM	Temperature Grade[2]	Package Description	Package Option
ADSP-BF700KCPZ-1	100 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700KCPZ-2	200 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700BCPZ-2	200 MHz	128K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF701KBCZ-1	100 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701KBCZ-2	200 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701BBCZ-2	200 MHz	128K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF702KCPZ-3	300 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-3	300 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702KCPZ-4	400 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-4	400 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF703KBCZ-3	300 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-3	300 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703KBCZ-4	400 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-4	400 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF704KCPZ-3	300 MHz	512K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-3	300 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704KCPZ-4	400 MHz	512K bytes	0C to +70C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-4	400 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF705KBCZ-3	300 MHz	512K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-3	300 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705KBCZ-4	400 MHz	512K bytes	0C to +70C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-4	400 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF706KCPZ-3	300 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-3	300 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706KCPZ-4	400 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-4	400 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF707KBCZ-3	300 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-3	300 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707KBCZ-4	400 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-4	400 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 50 for the junction temperature (T_J) specification which is the only temperature specification.

D12396-0-9/15(A)