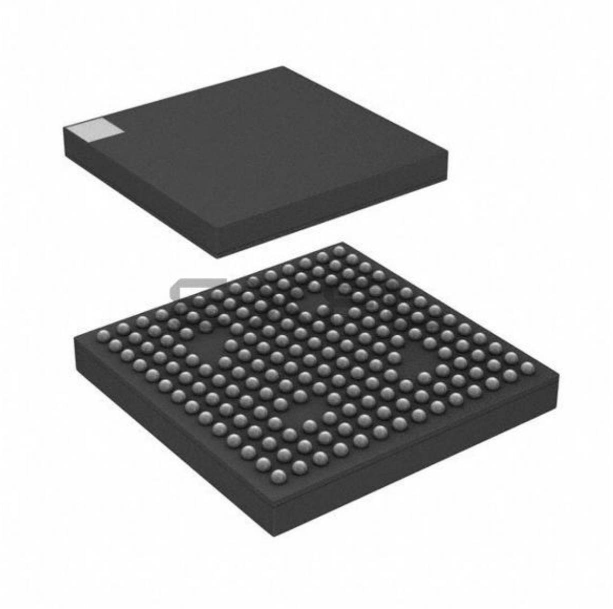
Analog Devices Inc. - ADSP-BF705BBCZ-4 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	512kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf705bbcz-4

GENERAL DESCRIPTION

The ADSP-BF70x processor is a member of the Blackfin® family of products. The Blackfin processor combines a dual-MAC 16-bit state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture. New enhancements to the Blackfin+ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements—all while maintaining instruction set compatibility to previous Blackfin products.

The processor offers performance up to 400 MHz, as well as low static power consumption. Produced with a low-power and low-voltage design methodology, they provide world-class power management and performance.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the Blackfin processor is the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package. These applications span a wide array of markets, from automotive systems to embedded industrial, instrumentation, video/image analysis, biometric and power/motor control applications.

Table 1. Processor Comparison

Processor Feature		ADSP-BF700	ADSP-BF701	ADSP-BF702	ADSP-BF703	ADSP-BF704	ADSP-BF705	ADSP-BF706	ADSP-BF707
Maximum Speed Grade (MHz)[1]		200		400					
Maximum SYSCLK (MHz)		100		200					
Package Options		88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA
GPIOs		43	47	43	47	43	47	43	47
Memory (bytes)	L1 Instruction SRAM	48K							
	L1 Instruction SRAM/Cache	16K							
	L1 Data SRAM	32K							
	L1 Data SRAM/Cache	32K							
	L1 Scratchpad (L1 Data C)	8K							
	L2 SRAM	128K		256K		512K		1024K	
	L2 ROM	512K							
	DDR2/LPDDR (16-bit)	No	Yes	No	Yes	No	Yes	No	Yes
I²C		1							
Up/Down/Rotary Counter		1							
GP Timer		8							
Watchdog Timer		1							
GP Counter		1							
SPORTs		2							
Quad SPI		2							
Dual SPI		1							
SPI Host Port		1							
USB 2.0 HS OTG		1							
Parallel Peripheral Interface		1							
CAN		2							
UART		2							
Real-Time Clock		1							
Static Memory Controller (SMC)		Yes							
Security Crypto Engine		Yes							
SD/SDIO (MSI)		4-bit	8-bit	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit
4-Channel 12-Bit ADC		No	Yes	No	Yes	No	Yes	No	Yes

[1] Other speed grades available.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with dynamic branch prediction), and subroutine calls. Hardware supports zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

The Blackfin processor supports a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

INSTRUCTION SET DESCRIPTION

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. The Blackfin processor supports a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Control of all asynchronous and synchronous events to the processor is handled by two subsystems: the core event controller (CEC) and the system event controller (SEC).
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADSP-BF70x processor.

DMA Controllers

The processor uses direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processor can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory-to-memory DMA stream uses two channels, where one channel is the source channel, and the second is the destination channel.

All DMAs can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers, descriptor-based or register-based. Register-based DMA allows the processor to directly program DMA control registers to initiate a DMA transfer. On completion, the control registers may be automatically updated with their original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together and a DMA channel can be programmed to automatically set up and start another DMA transfer after the current sequence completes.

The DMA controller supports the following DMA operations.

- A single linear buffer that stops on completion.
- A linear buffer with negative, positive, or zero stride length.
- A circular, auto-refreshing buffer that interrupts when each buffer becomes full.

- A similar buffer that interrupts on fractional buffers (for example, 1/2, 1/4).
- 1D DMA—uses a set of identical ping-pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address.
- 1D DMA—uses a linked list of 4 word descriptor sets containing a link pointer, an address, a length, and a configuration.
- 2D DMA—uses an array of one-word descriptor sets, specifying only the base DMA address.
- 2D DMA—uses a linked list of multi-word descriptor sets, specifying everything.

Event Handling

The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The processor provides support for five different types of events:

- Emulation—An emulation event causes the processor to enter emulation mode, allowing command and control of the processor through the JTAG interface.
- Reset—This event resets the processor.
- Nonmaskable interrupt (NMI)—The NMI event can be generated either by the software watchdog timer, by the $\overline{\text{NMI}}$ input signal to the processor, or by software. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions—Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts —Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

The SEC manages the enabling, prioritization, and routing of events from each system interrupt or fault source. Additionally, it provides notification and identification of the highest priority active system interrupt request to the core and routes system fault sources to its integrated fault management unit. The SEC triggers core general-purpose interrupt IVG11. It is recommended that IVG11 be set to allow self-nesting. The four lower priority interrupts (IVG15-12) may be used for software interrupts.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register—Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers—A write one to modify mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers—Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers—Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Interrupts

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Three system-level interrupt channels (PINT0–3) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of 4 peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature—that is, when the system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even L3 memories (DDR2, LPDDR). The processor features two CRC engines which are embedded in the memory-to-memory DMA controllers. CRC checksums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Memory Protection

The Blackfin+ core features a memory protection concept, which grants data and/or instruction accesses to enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

The system protection unit (SPU) guards against accidental or unwanted access to the MMR space of a peripheral by providing a write-protection mechanism. The user is able to choose and configure the peripherals that are protected as well as configure which ones of the four system MMR masters (core, memory DMA, the SPI host port, and Coresight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write-protection functionality, the SPU is employed to define which resources in the system are secure or non-secure and to block access to secure resources from non-secure masters.

Synonymously, the system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are two SMPU units in the ADSP-BF70x processors. One is for the L2 memory and the other is for the external DDR memory.

The SMPU is also part of the security infrastructure. It allows the user to not only protect against arbitrary read and/or write transactions, but it also allows regions of memory to be defined as secure and prevent non-secure masters from accessing those memory regions.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or the core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the fault management unit of the SEC.

Watchdog

The on-chip software watchdog timer can supervise the Blackfin+ core.

Bandwidth Monitor

Memory-to-memory DMA channels are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the GP counter can flag this to the processor or to the fault management unit of the SEC.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a fault. Additionally, the system events can be defined as an interrupt to the core. If defined as such, the SEC forwards the event to the fault management unit, which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken through a keyed sequence, to provide a final chance for the Blackfin+ core to resolve the issue and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

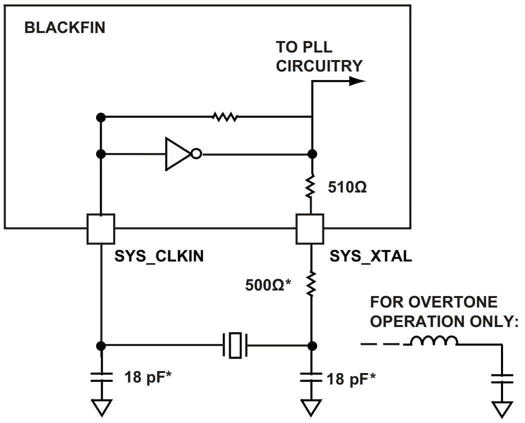
The processor contains a rich set of peripherals connected to the core through several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processor contains high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not previously described.

Timers

The processor includes several timers which are described in the following sections.

level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over the required temperature range.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM.

Figure 4. External Crystal Connection

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) *Using Third Overtone Crystals with the ADSP-218x DSP* (www.analog.com/ee-168).

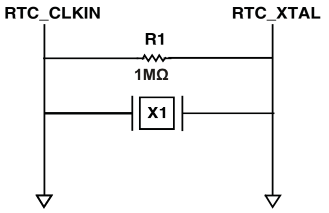
The same recommendations may be used for the USB crystal oscillator.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. Connect RTC pins RTC_CLKIN and RTC_XTAL with external components as shown in Figure 5.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms. The first alarm is for a time of day. The second alarm is for a specific day and time of that day.



NOTE: CRYSTAL LOAD CAPACITORS ARE NOT NECESSARY IN MOST CASES.

Figure 5. External Components for RTC

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0, and SCLK1), the LPDDR or DDR2 clock (DCLK), and the output clock (OCLK).

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ can be applied after all voltage supplies are within specifications, and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example, PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be output on the SYS_CLKOUT pin.

ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
USB_DM	I/O	**Data –.** Bidirectional differential data line.
USB_DP	I/O	**Data +.** Bidirectional differential data line.
USB_ID	Input	**OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. May be configured as open-drain. Polarity is configurable as well.
USB_VBUS	I/O	**Bus Voltage.** Connects to bus voltage in host and device modes.
USB_XTAL	Output	**Crystal.** Drives an external crystal. Must be left unconnected if an external clock is driving USB_CLKIN.

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	C	PC_03
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	C	PC_02
$\overline{\text{UART0\_RX}}$	UART0 Receive	B	PB_09
$\overline{\text{UART0\_TX}}$	UART0 Transmit	B	PB_08
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	B	PB_14
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	B	PB_13
$\overline{\text{UART1\_RX}}$	UART1 Receive	C	PC_01
$\overline{\text{UART1\_TX}}$	UART1 Transmit	C	PC_00
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB0_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB0_XTAL
VDD_EXT	External VDD	Not Muxed	VDD_EXT
VDD_INT	Internal VDD	Not Muxed	VDD_INT
VDD_OTP	VDD for OTP	Not Muxed	VDD_OTP
VDD_RTC	VDD for RTC	Not Muxed	VDD_RTC
VDD_USB	VDD for USB	Not Muxed	VDD_USB

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input Notes: If USB is not used, connect to ground. Active during reset
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data – Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_ID	I/O	na	none	none	none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: If USB is not used connect to ground. When USB is being used, the internal pull-up that is present during hibernate is programmable. See the USB chapter in the HRM. Active during reset.
USB0_VBC	I/O	E	none	none	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: If USB is not, used pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: If USB is not used, connect to ground.
USB0_XTAL	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Crystal Notes: No notes.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD Notes: Must be powered.
VDD_HADC	s	na	none	none	none	none	none	na	Desc: VDD for HADC Notes: If HADC is not used, connect to ground.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD Notes: Must be powered.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Internal Supply Voltage	CCLK ≤ 400 MHz	1.045	1.100	1.155	V
V_{DD_EXT}[1]	External Supply Voltage		1.7	1.8	1.9	V
V_{DD_EXT}[1]	External Supply Voltage		3.13	3.30	3.47	V
V_{DD_DMC}	DDR2/LPDDR Supply Voltage		1.7	1.8	1.9	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.30	3.47	V
V_{DD_RTC}	Real-Time Clock Supply Voltage		2.00	3.30	3.47	V
V_{DD_HADC}	Housekeeping ADC Supply Voltage		3.13	3.30	3.47	V
V_{DD_OTP}[1]	OTP Supply Voltage					
	For Reads		2.25	3.30	3.47	V
	For Writes		3.13	3.30	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage		$0.49 \times V_{DD\_DMC}$	$0.50 \times V_{DD\_DMC}$	$0.51 \times V_{DD\_DMC}$	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{IH}[4]	High Level Input Voltage	$V_{DD\_EXT} = 3.47$ V	2.0			V
V_{IH}[4]	High Level Input Voltage	$V_{DD\_EXT} = 1.9$ V	$0.7 \times V_{DD\_EXT}$			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = maximum	$0.7 \times V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IH_DDR2}[7]		$V_{DD\_DMC} = 1.9$ V	$V_{DDR\_REF} + 0.25$			V
V_{IH_LPDDR}[8]		$V_{DD\_DMC} = 1.9$ V	$0.8 \times V_{DD\_DMC}$			V
V_{ID_DDR2}[9]	Differential Input Voltage	$V_{IX} = 1.075$ V	0.50			V
V_{ID_DDR2}[9]	Differential Input Voltage	$V_{IX} = 0.725$ V	0.55			V
V_{IL}[4]	Low Level Input Voltage	$V_{DD\_EXT} = 3.13$ V			0.8	V
V_{IL}[4]	Low Level Input Voltage	$V_{DD\_EXT} = 1.7$ V			$0.3 \times V_{DD\_EXT}$	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = minimum			$0.3 \times V_{VBUSTWI}$	V
V_{IL_DDR2}[7]		$V_{DD\_DMC} = 1.7$ V			$V_{DDR\_REF} – 0.25$	V
V_{IL_LPDDR}[8]		$V_{DD\_DMC} = 1.7$ V			$0.2 \times V_{DD\_DMC}$	V
T_J	Junction Temperature	$T_{AMBIENT}$ = 0°C to +70°C	0		105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).

[2] If not used, connect to 1.8 V or 3.3 V.

[3] V_{HADC_VREF} should always be less than V_{DD_HADC}.

[4] Parameter value applies to all input and bidirectional signals except RTC signals, TWI signals, DMC0 signals, and USB0 signals.

[5] Parameter applies to TWI signals.

[6] TWI signals are pulled up to V_{BUSTWI}. See Table 16.

[7] Parameter applies to DMC0 signals in DDR2 mode.

[8] Parameter applies to DMC0 signals in LPDDR mode.

[9] Parameter applies to signals DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$ when used in DDR2 differential input mode.

Table 21. Static Current—$I_{DD\_DEEPSLEEP}$ (mA)

	Voltage (V_{DD_INT})												
T_J (°C)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
–40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
–20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

Table 22. Activity Scaling Factors (ASF)

I_{DDINT} Power Vector	ASF
$I_{DD-IDLE1}$	0.05
$I_{DD-IDLE2}$	0.05
$I_{DD-NOP1}$	0.56
$I_{DD-NOP2}$	0.59
$I_{DD-APP3}$	0.78
$I_{DD-APP1}$	0.79
$I_{DD-APP2}$	0.83
$I_{DD-TYP1}$	1.00
$I_{DD-TYP3}$	1.01
$I_{DD-TYP2}$	1.03
$I_{DD-HIGH1}$	1.39
$I_{DD-HIGH3}$	1.39
$I_{DD-HIGH2}$	1.54

Table 23. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})												
f_{CCLK} (MHz)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

DDR2 SDRAM Read Cycle Timing

Table 40 and Figure 18 show DDR2 SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 40. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

		200 MHz[1]		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.35	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.8		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.

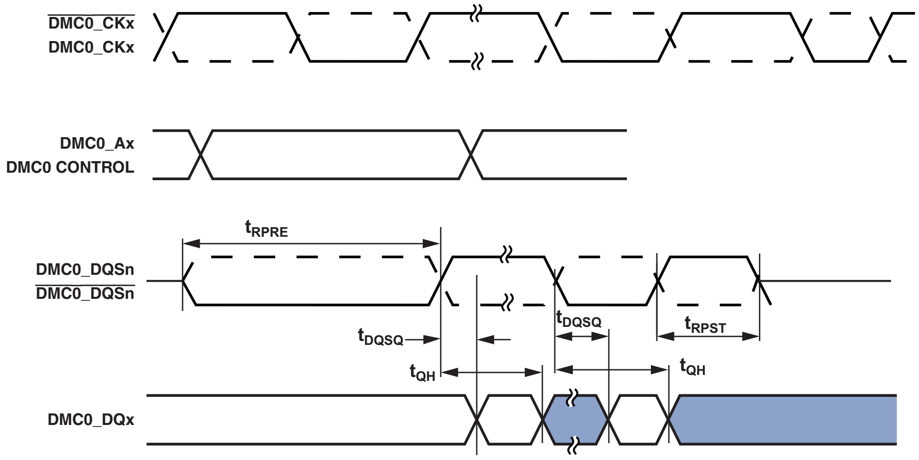


Figure 18. DDR2 SDRAM Controller Input AC Timing

Mobile DDR SDRAM Read Cycle Timing

Table 43 and Figure 21 show mobile DDR SDRAM read cycle timing, related to the dynamic memory controller (DMC).

Table 43. Mobile DDR SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz		Unit
		Min	Max	
Timing Requirements				
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	1.5		ns
t_{DQSQ}	DMC0_DQS-DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.7	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}

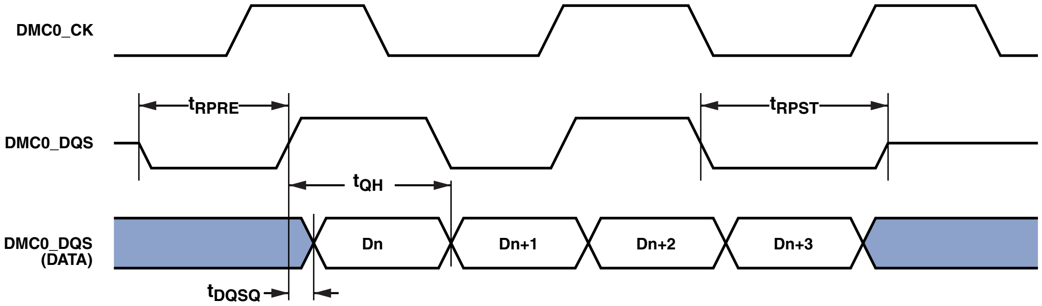


Figure 21. Mobile DDR SDRAM Controller Input AC Timing

Debug Interface (JTAG Emulation Port) Timing

Table 48 and Figure 26 provide I/O timing, related to the debug interface (JTAG emulator port).

Table 48. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	5		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	4		4		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK Cycles)[2]	4		4		t_{TCK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		16.5		14.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		18		16.5	ns
t_{DTMS}	TMS Delay After TCK High in SWD Mode	3.5	16.5	3.5	14.5	ns

[1] System inputs = DMC0_DQxx, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_xx, PB_xx, PC_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA, and SYS_EXTWAKE.

[2] 50 MHz maximum.

[3] System outputs = DMC0_Axx, DMC0_BAx, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, PA_xx, PB_xx, PC_xx, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$, and $\overline{\text{SYS\_NMI}}$.

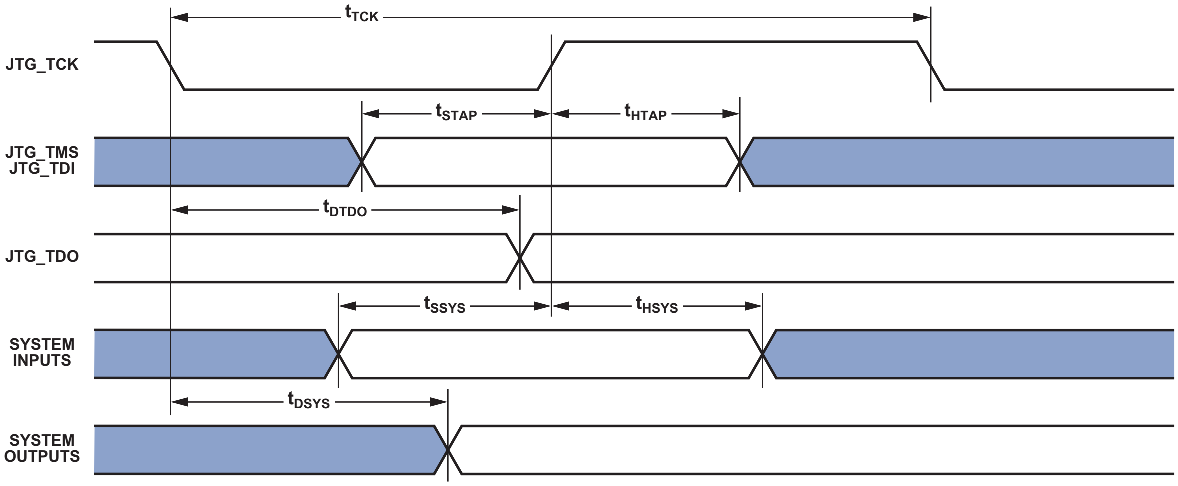


Figure 26. JTAG Port Timing

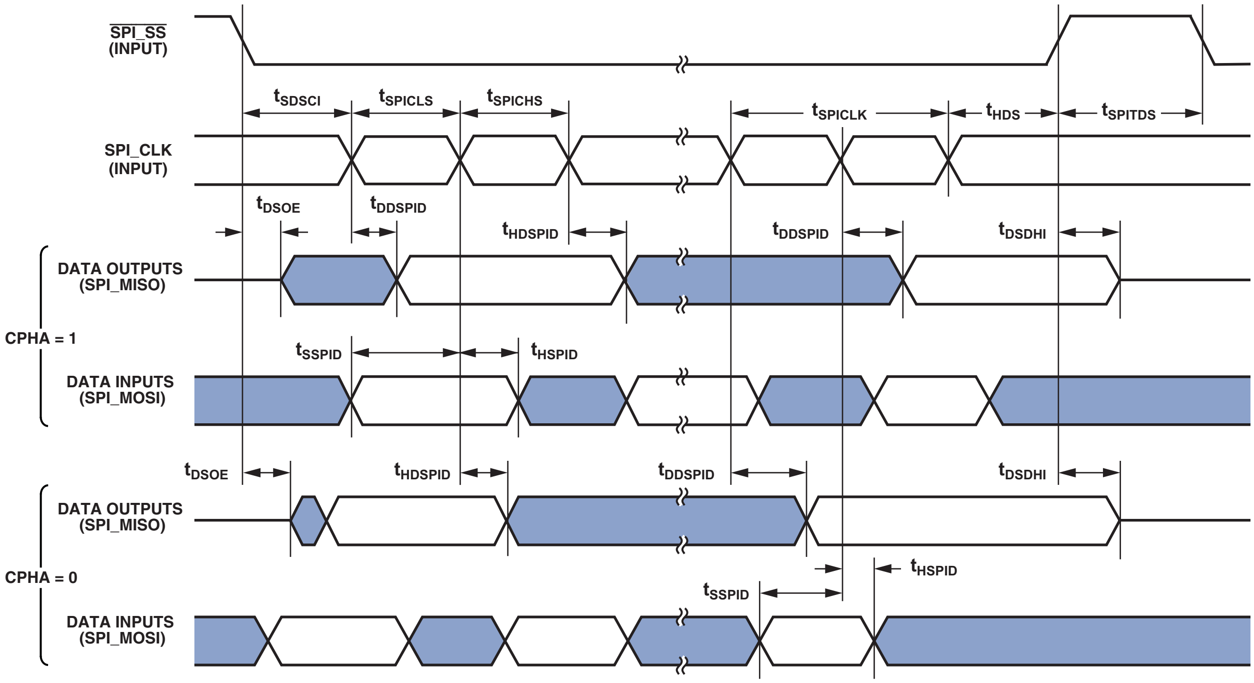


Figure 32. Serial Peripheral Interface (SPI) Port—Slave Timing

Enhanced Parallel Peripheral Interface Timing

The following tables and figures describe enhanced parallel peripheral interface timing operations. The POLC bits in the EPPI_CTL register may be used to set the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in MHz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65,535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 60. Enhanced Parallel Peripheral Interface—Internal Clock

		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	1.5		1		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.4		5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	1		1		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	16.5		14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	1.5		0		ns
Switching Characteristics						
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 2$		$0.5 \times t_{PCLKPROG} - 2$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 2$		$t_{PCLKPROG} - 2$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		2		2	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–4		–3		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		2		2	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–4		–3		ns

[1] See Table 18 on Page 52 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{PCLKPROG}$.

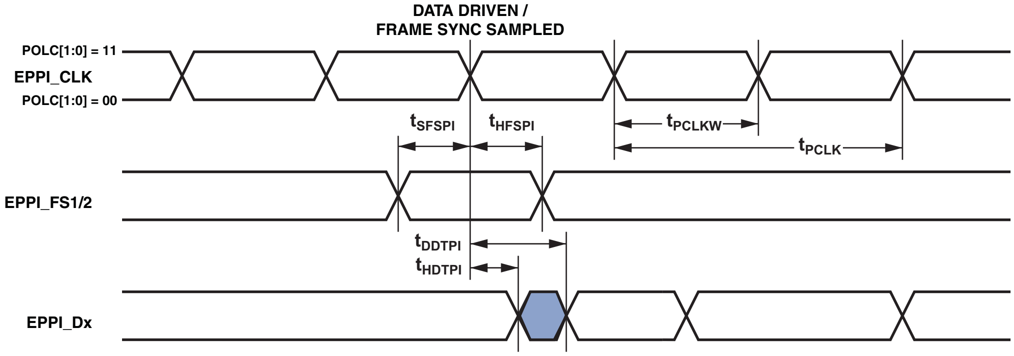


Figure 43. PPI Internal Clock GP Transmit Mode with External Frame Sync Timing

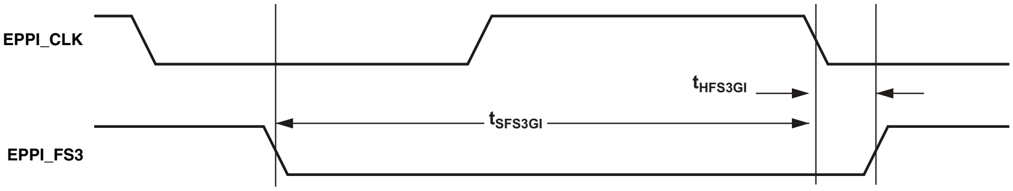


Figure 44. Clock Gating Mode with Internal Clock and External Frame Sync Timing

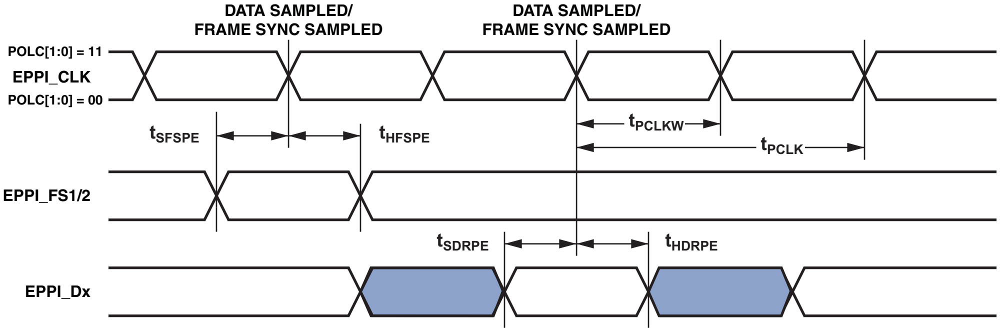


Figure 47. PPI External Clock GP Receive Mode with External Frame Sync Timing

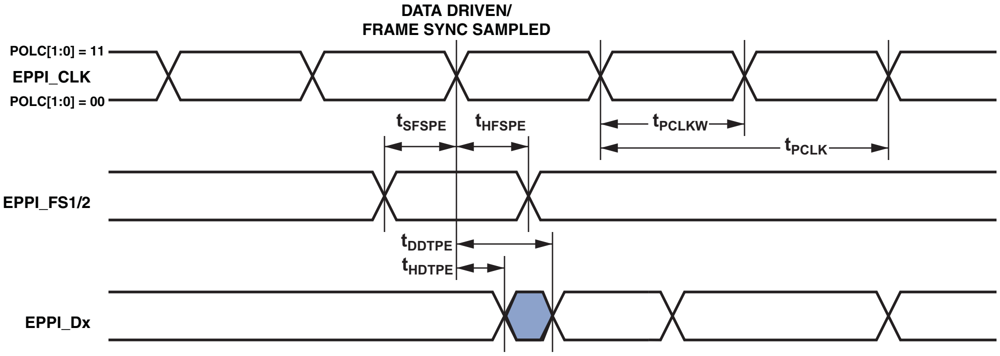


Figure 48. PPI External Clock GP Transmit Mode with External Frame Sync Timing

OUTPUT DRIVE CURRENTS

Figure 50 through Figure 61 show typical current-voltage characteristics for the output drivers of the ADSP-BF70x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

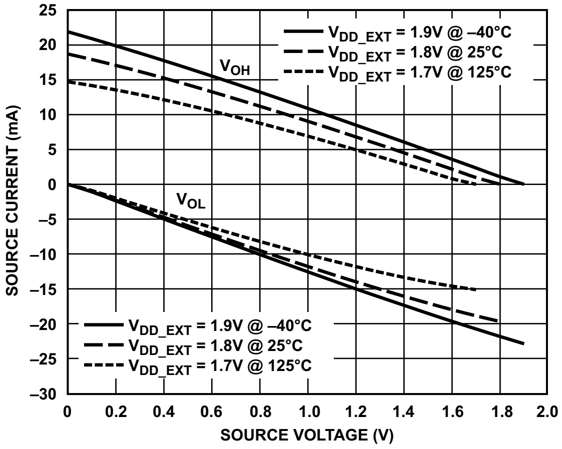


Figure 50. Driver Type A Current (1.8 V V_{DD_EXT})

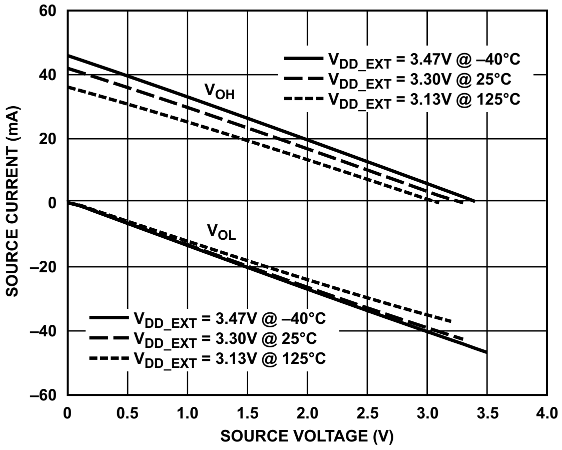


Figure 51. Driver Type A Current (3.3 V V_{DD_EXT})

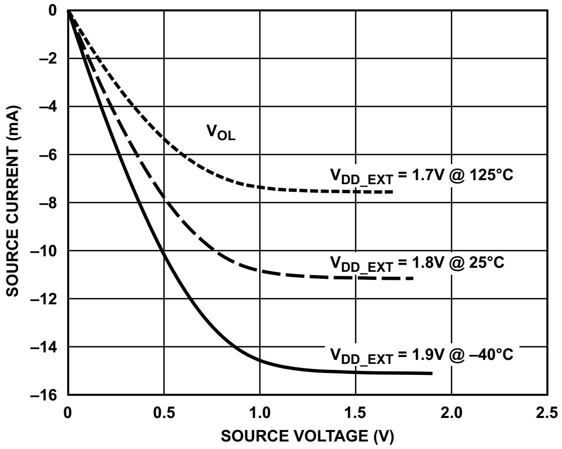


Figure 52. Driver Type D Current (1.8 V V_{DD_EXT})

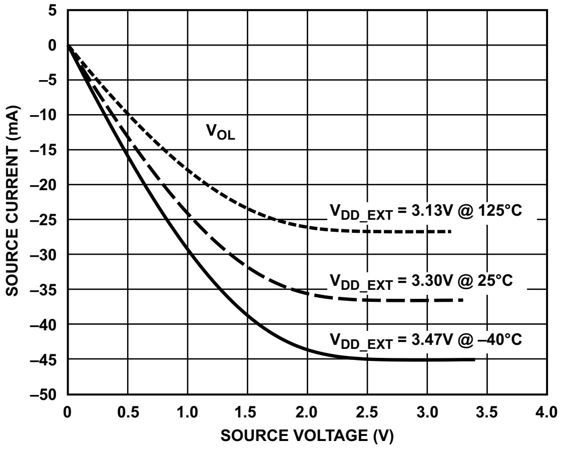


Figure 53. Driver Type D Current (3.3 V V_{DD_EXT})

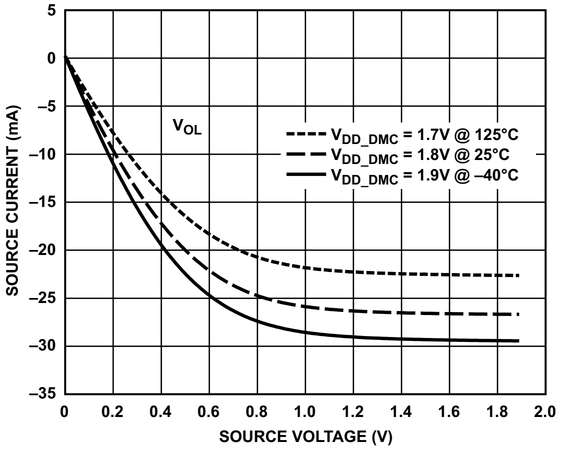


Figure 54. Driver Type B and Driver Type C (DDR Drive Strength 34 Ω)

ADSP-BF70x 184-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Figure 69 shows an overview of signal placement on the 184-ball CSP_BGA.

Table 67 lists the 184-ball CSP_BGA package by ball number for the ADSP-BF70x. Table 68 lists the 184-ball CSP_BGA package by signal.

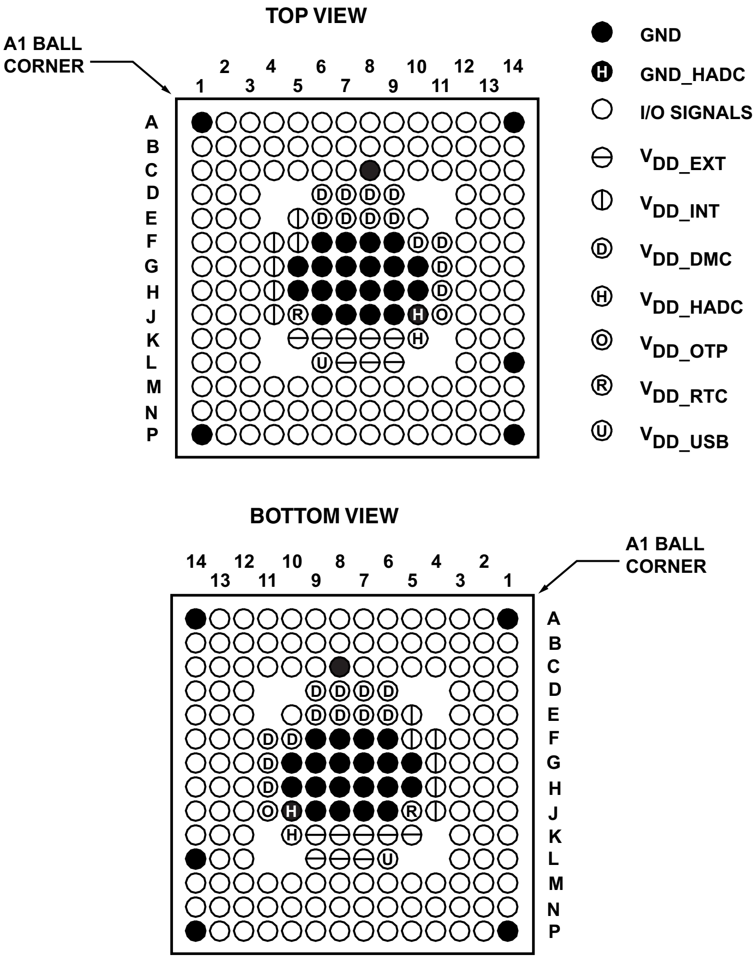


Figure 69. 184-Ball CSP_BGA Configuration