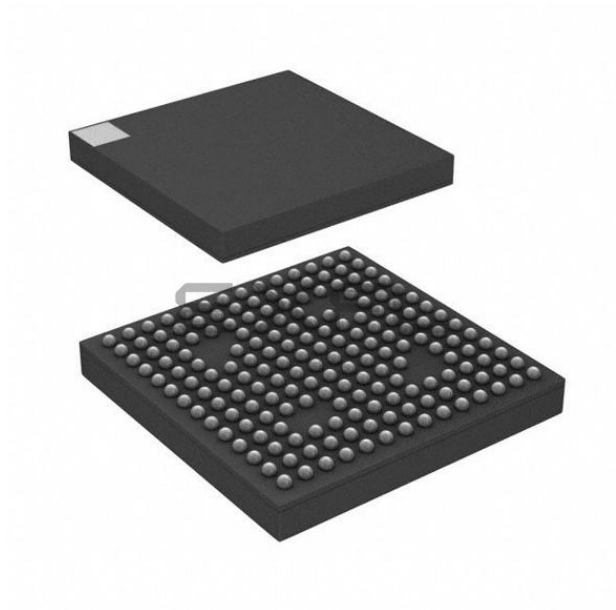

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	512kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf705kbcz-3

GENERAL DESCRIPTION

The ADSP-BF70x processor is a member of the Blackfin® family of products. The Blackfin processor combines a dual-MAC 16-bit state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture. New enhancements to the Blackfin+ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements—all while maintaining instruction set compatibility to previous Blackfin products.

The processor offers performance up to 400 MHz, as well as low static power consumption. Produced with a low-power and low-voltage design methodology, they provide world-class power management and performance.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the Blackfin processor is the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package. These applications span a wide array of markets, from automotive systems to embedded industrial, instrumentation, video/image analysis, biometric and power/motor control applications.

Table 1. Processor Comparison

Processor Feature		ADSP-BF700	ADSP-BF701	ADSP-BF702	ADSP-BF703	ADSP-BF704	ADSP-BF705	ADSP-BF706	ADSP-BF707
Maximum Speed Grade (MHz)[1]		200		400					
Maximum SYSCLK (MHz)		100		200					
Package Options		88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA	88-Lead LFCSP	184-Ball CSP_BGA
GPIOs		43	47	43	47	43	47	43	47
Memory (bytes)	L1 Instruction SRAM	48K							
	L1 Instruction SRAM/Cache	16K							
	L1 Data SRAM	32K							
	L1 Data SRAM/Cache	32K							
	L1 Scratchpad (L1 Data C)	8K							
	L2 SRAM	128K		256K		512K		1024K	
	L2 ROM	512K							
	DDR2/LPDDR (16-bit)	No	Yes	No	Yes	No	Yes	No	Yes
I^2C		1							
Up/Down/Rotary Counter		1							
GP Timer		8							
Watchdog Timer		1							
GP Counter		1							
SPORTs		2							
Quad SPI		2							
Dual SPI		1							
SPI Host Port		1							
USB 2.0 HS OTG		1							
Parallel Peripheral Interface		1							
CAN		2							
UART		2							
Real-Time Clock		1							
Static Memory Controller (SMC)		Yes							
Security Crypto Engine		Yes							
SD/SDIO (MSI)		4-bit	8-bit	4-bit	8-bit	4-bit	8-bit	4-bit	8-bit
4-Channel 12-Bit ADC		No	Yes	No	Yes	No	Yes	No	Yes

[1] Other speed grades available.

BLACKFIN+ PROCESSOR CORE

As shown in Figure 1, the processor integrates a Blackfin+ processor core. The core, shown in Figure 2, contains two 16-bit multipliers, one 32-bit multiplier, two 40-bit accumulators (which may be used together as a 72-bit accumulator), two 40-bit ALUs, one 72-bit ALU, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

The core can perform two 16-bit by 16-bit multiply-accumulates or one 32-bit multiply-accumulate in each cycle. Signed and unsigned formats, rounding, saturation, and complex multiplies are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If a second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

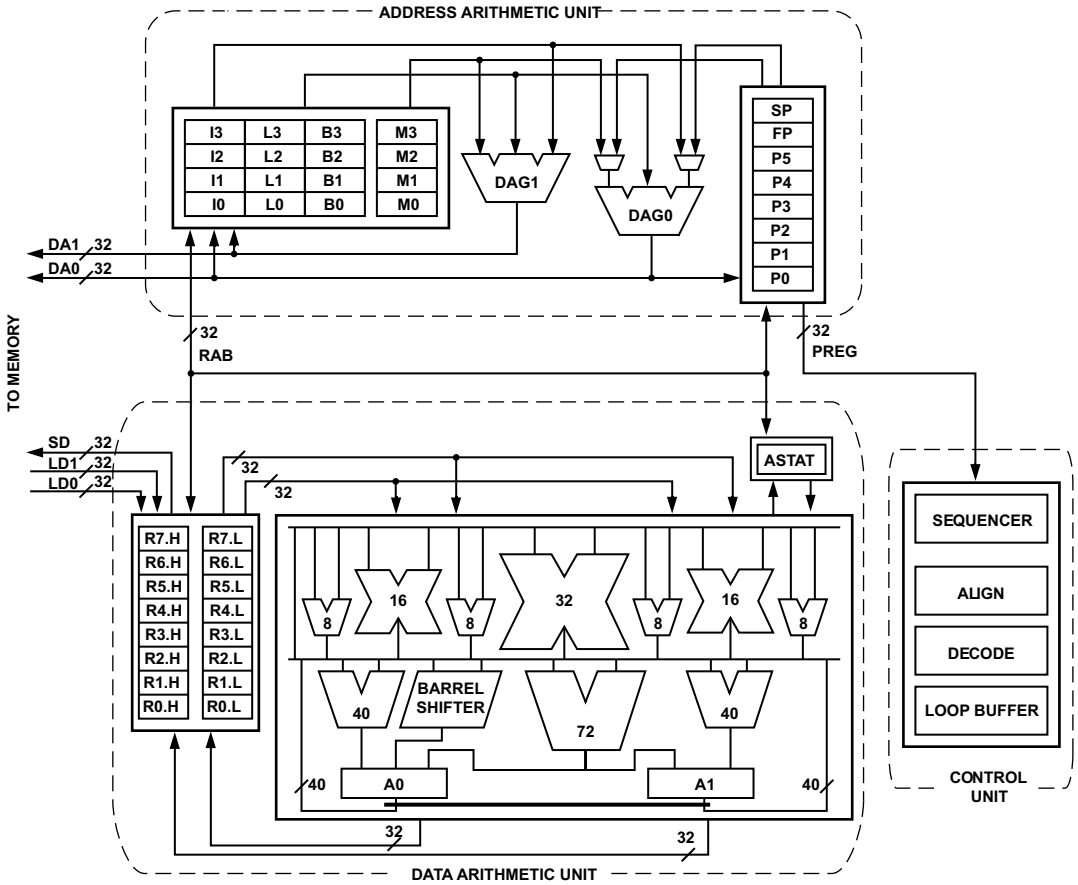


Figure 2. Blackfin+ Processor Core

Table 7. ADSP-BF70x 184-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SYS_FAULT	Active-Low Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_NMI	Nonmaskable Interrupt	Not Muxed	SYS_NMI
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_WAKE0	Power Saving Mode Wake-up 0	B	PB_07
SYS_WAKE1	Power Saving Mode Wake-up 1	B	PB_08
SYS_WAKE2	Power Saving Mode Wake-up 2	B	PB_12
SYS_WAKE3	Power Saving Mode Wake-up 3	C	PC_02
SYS_WAKE4	Power Saving Mode Wake-up 4	A	PA_12
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI0	TIMER0 Alternate Capture Input 0	C	PC_03
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_01
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_07
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_09
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_02
TM0_ACI6	TIMER0 Alternate Capture Input 6	A	PA_12
TM0_ACLK0	TIMER0 Alternate Clock 0	C	PC_04
TM0_ACLK1	TIMER0 Alternate Clock 1	C	PC_10
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_09
TM0_ACLK3	TIMER0 Alternate Clock 3	B	PB_00
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_10
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_14
TM0_ACLK6	TIMER0 Alternate Clock 6	B	PB_04
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	A	PA_05
TM0_TMR1	TIMER0 Timer 1	A	PA_06
TM0_TMR2	TIMER0 Timer 2	A	PA_07
TM0_TMR3	TIMER0 Timer 3	C	PC_05
TM0_TMR4	TIMER0 Timer 4	A	PA_09
TM0_TMR5	TIMER0 Timer 5	A	PA_10
TM0_TMR6	TIMER0 Timer 6	A	PA_11
TM0_TMR7	TIMER0 Timer 7	A	PA_04
TRACE0_CLK	TPIU0 Trace Clock	B	PB_10
TRACE0_D00	TPIU0 Trace Data 0	B	PB_15
TRACE0_D01	TPIU0 Trace Data 1	B	PB_14
TRACE0_D02	TPIU0 Trace Data 2	B	PB_13
TRACE0_D03	TPIU0 Trace Data 3	B	PB_12
TRACE0_D04	TPIU0 Trace Data 4	B	PB_11
TRACE0_D05	TPIU0 Trace Data 5	A	PA_02
TRACE0_D06	TPIU0 Trace Data 6	A	PA_01
TRACE0_D07	TPIU0 Trace Data 7	A	PA_00
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
UART0_CTS	UART0 Clear to Send	C	PC_03
UART0_RTS	UART0 Request to Send	C	PC_02

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D11	SMC0 Data 11	B	PB_11
SMC0_D12	SMC0 Data 12	B	PB_12
SMC0_D13	SMC0 Data 13	B	PB_13
SMC0_D14	SMC0 Data 14	B	PB_14
SMC0_D15	SMC0 Data 15	B	PB_15
SPI0_CLK	SPI0 Clock	B	PB_00
SPI0_CLK	SPI0 Clock	C	PC_04
SPI0_D2	SPI0 Data 2	B	PB_03
SPI0_D2	SPI0 Data 2	C	PC_08
SPI0_D3	SPI0 Data 3	B	PB_07
SPI0_D3	SPI0 Data 3	C	PC_09
SPI0_MISO	SPI0 Master In, Slave Out	B	PB_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_06
SPI0_MOSI	SPI0 Master Out, Slave In	B	PB_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_07
SPI0_RDY	SPI0 Ready	A	PA_06
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	A	PA_05
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	A	PA_06
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	B	PB_04
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	B	PB_05
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	B	PB_06
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	A	PA_05
SPI1_CLK	SPI1 Clock	A	PA_00
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_01
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_02
SPI1_RDY	SPI1 Ready	A	PA_03
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	A	PA_04
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	A	PA_03
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	C	PC_10
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	A	PA_14
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	A	PA_04
SPI2_CLK	SPI2 Clock	B	PB_10
SPI2_D2	SPI2 Data 2	B	PB_13
SPI2_D3	SPI2 Data 3	B	PB_14
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_11
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_12
SPI2_RDY	SPI2 Ready	A	PA_04
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	B	PB_15
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	B	PB_08
$\overline{\text{SPI2\_SEL3}}$	SPI2 Slave Select Output 3	B	PB_09
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	B	PB_15
SPT0_ACLK	SPORT0 Channel A Clock	A	PA_13
SPT0_ACLK	SPORT0 Channel A Clock	C	PC_09
SPT0_AD0	SPORT0 Channel A Data 0	A	PA_14
SPT0_AD0	SPORT0 Channel A Data 0	C	PC_08
SPT0_AD1	SPORT0 Channel A Data 1	C	PC_00

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 3 | SPT0 Channel B Clock | SPI0 Slave Select Output 4 | SMC0 Data 3 | TM0 Alternate Clock 6 Notes: SPI slave select outputs require a pull-up when used.
PB_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 2 | SPT0 Channel B Data 0 | SPI0 Slave Select Output 5 | SMC0 Data 2 Notes: SPI slave select outputs require a pull-up when used.
PB_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 1 | SPT0 Channel B Frame Sync | SPI0 Slave Select Output 6 | SMC0 Data 1 | TM0 Clock Notes: SPI slave select outputs require a pull-up when used.
PB_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 0 | SPT0 Channel B Data 1 | SPI0 Data 3 | SMC0 Data 0 | SYS Power Saving Mode Wakeup 0 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Transmit | PPI0 Data 16 | SPI2 Slave Select Output 2 | SMC0 Data 8 | SYS Power Saving Mode Wakeup 1 Notes: SPI slave select outputs require a pull-up when used. If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Receive | PPI0 Data 17 | SPI2 Slave Select Output 3 | SMC0 Data 9 | TM0 Alternate Capture Input 3 Notes: SPI slave select outputs require a pull-up when used.
PB_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Clock | TRACE0 Trace Clock | SMC0 Data 10 | TM0 Alternate Clock 4 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PB_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master In, Slave Out | TRACE0 Trace Data 4 | SMC0 Data 11 Notes: Pull-up required for SPI_MISO if SPI master boot is used.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
VDD_OTP	s	na	none	none	none	none	none	na	Desc: VDD for OTP Notes: Must be powered.
VDD_RTC	s	na	none	none	none	none	none	na	Desc: VDD for RTC Notes: If RTC is not used, connect to ground.
VDD_USB	s	na	none	none	none	none	none	na	Desc: VDD for USB Notes: If USB is not used, connect to VDD_EXT.

Total Internal Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current (deep sleep)
2. Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DDINT\_TOT} = I_{DDINT\_DEEPSLEEP} + I_{DDINT\_CCLK\_DYN} + I_{DDINT\_PLLCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_USBCLK\_DYN}$$

$I_{DDINT\_DEEPSLEEP}$ is the only item present that is part of the static power dissipation component. $I_{DDINT\_DEEPSLEEP}$ is specified as a function of voltage (V_{DD_INT}) and temperature (see Table 21).

There are eight different items that contribute to the dynamic power dissipation. These components fall into three broad categories: application-dependent currents, clock currents, and data transmission currents.

Application-Dependent Current

The application-dependent currents include the dynamic current in the core clock domain.

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor cores and L1/L2 memories (Table 22). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent data in Table 23 to calculate this portion.

$I_{DDINT\_CCLK\_DYN}$ (mA) = Table 23 × *ASF*

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency and a unique scaling factor.

$I_{DDINT\_PLLCLK\_DYN}$ (mA) = 0.012 × f_{PLLCLK} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SYSCLK\_DYN}$ (mA) = 0.120 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK0\_DYN}$ (mA) = 0.110 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_SCLK1\_DYN}$ (mA) = 0.068 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DDINT\_DCLK\_DYN}$ (mA) = 0.055 × f_{DCLK} (MHz) × V_{DD_INT} (V)

The dynamic component of the USB clock is a unique case. The USB clock contributes a near constant current value when used.

Table 20. $I_{DDINT\_USBCLK\_DYN}$ Current

Is USB Enabled?	$I_{DDINT\_USBCLK\_DYN}$ (mA)
Yes – High-Speed Mode	13.94
Yes – Full-Speed Mode	10.83
Yes – Suspend Mode	5.2
No	0.34

Data Transmission Current

The data transmission current represents the power dissipated when transmitting data. This current is expressed in terms of data rate. The calculation is performed by adding the data rate (MB/s) of each DMA-driven access to peripherals, L1, L2, and external memory. This number is then multiplied by a weighted data-rate coefficient and V_{DD_INT}:

$I_{DDINT\_DMADR\_DYN}$ (mA) = *Weighted DRC* × *Total Data Rate* (MB/s) × V_{DD_INT} (V)

A weighted data-rate coefficient is used because different coefficients exist depending on the source and destination of the transfer. For details on using this equation and calculating the weighted DRC, see the related Engineer Zone material. For a quick maximum calculation, the weighted DRC can be assumed to be 0.0497, which is the coefficient for L1 to L1 transfers.

Table 21. Static Current—$I_{DD\_DEEPSLEEP}$ (mA)

	Voltage (V_{DD_INT})												
T_J (°C)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
–40	0.6	0.6	0.7	0.7	0.7	0.8	0.8	0.8	0.9	0.9	0.9	1.0	1.0
–20	1.1	1.1	1.2	1.2	1.2	1.3	1.4	1.4	1.5	1.5	1.6	1.7	1.7
0	2.0	2.0	2.1	2.2	2.3	2.4	2.5	2.5	2.6	2.7	2.8	3.0	3.0
25	4.3	4.3	4.5	4.7	4.8	5.0	5.2	5.3	5.5	5.7	5.9	6.1	6.2
40	6.7	6.8	7.0	7.3	7.5	7.8	8.0	8.3	8.6	8.8	9.1	9.4	9.6
55	10.3	10.5	10.8	11.2	11.5	11.9	12.3	12.6	13.0	13.4	13.9	14.3	14.5
70	15.7	15.9	16.4	16.8	17.4	17.9	18.4	18.9	19.5	20.1	20.7	21.3	21.6
85	23.3	23.6	24.3	25.0	25.7	26.4	27.2	27.9	28.7	29.5	30.4	31.2	31.7
100	34.2	34.6	35.5	36.5	37.5	38.5	39.5	40.6	41.7	42.8	43.9	45.1	45.7
105	38.7	39.2	40.2	41.3	42.4	43.5	44.6	45.8	47.0	48.2	49.5	50.8	51.5
115	48.9	49.5	50.7	52.0	53.4	54.7	56.0	57.5	59.0	60.5	62.0	63.6	64.4
125	61.5	62.1	63.6	65.1	66.7	68.3	69.9	71.7	73.4	75.2	77.0	79.0	79.9

Table 22. Activity Scaling Factors (ASF)

I_{DDINT} Power Vector	ASF
$I_{DD-IDLE1}$	0.05
$I_{DD-IDLE2}$	0.05
$I_{DD-NOP1}$	0.56
$I_{DD-NOP2}$	0.59
$I_{DD-APP3}$	0.78
$I_{DD-APP1}$	0.79
$I_{DD-APP2}$	0.83
$I_{DD-TYP1}$	1.00
$I_{DD-TYP3}$	1.01
$I_{DD-TYP2}$	1.03
$I_{DD-HIGH1}$	1.39
$I_{DD-HIGH3}$	1.39
$I_{DD-HIGH2}$	1.54

Table 23. CCLK Dynamic Current per core (mA, with ASF = 1)

	Voltage (V_{DD_INT})												
f_{CCLK} (MHz)	1.045	1.050	1.060	1.070	1.080	1.090	1.100	1.110	1.120	1.130	1.140	1.150	1.155
400	66.7	67.2	67.9	68.7	69.4	70.2	71.1	71.8	72.6	73.4	74.2	74.9	75.4
350	58.6	59.0	59.6	60.3	61.0	61.7	62.4	63.0	63.7	64.4	65.1	65.8	66.1
300	50.2	50.5	51.1	51.7	52.3	52.9	53.5	54.1	54.7	55.3	55.9	56.4	56.8
250	42.1	42.3	42.8	43.3	43.8	44.3	44.7	45.3	45.8	46.3	46.8	47.4	47.6
200	33.7	33.9	34.3	34.7	35.1	35.5	35.9	36.3	36.7	37.1	37.5	37.9	38.0
150	25.4	25.5	25.8	26.1	26.4	26.7	27.0	27.3	27.6	27.9	28.2	28.5	28.8
100	17.0	17.1	17.3	17.5	17.7	17.9	18.1	18.3	18.5	18.6	18.8	19.0	19.1

Asynchronous Page Mode Read

Table 34 and Figure 13 show asynchronous memory page mode read timing, related to the static memory controller (SMC).

Table 34. Asynchronous Page Mode Read

Parameter		V_{DD_EXT} 1.8 V /3.3 V Nominal Min	Max	Unit
Switching Characteristics				
t_{AV}	SMC0_Ax (Address) Valid for First Address Min Width[1]	(PREST + RST + PREAT + RAT) × t_{SCLK0} – 2		ns
t_{AV1}	SMC0_Ax (Address) Valid for Subsequent SMC0_Ax (Address) Min Width	PGWS × t_{SCLK0} – 2		ns
t_{WADV}	SMC0_NORDV Active Low Width[2]	RST × t_{SCLK0} – 2		ns
t_{HARE}	Output[3] Hold After $\overline{\text{SMC0\_ARE}}$ High[4]	RHT × t_{SCLK0} – 2		ns
t_{WARE}[5]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[6]	(RAT + (Nw – 1) × PGWS) × t_{SCLK0} – 2		ns

[1] PREST, RST, PREAT and RAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.RST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_AOE}}$.
[4] RHT value set using the SMC_BxTIM.RHT bits.
[5] SMC_BxCTL.ARDYEN bit = 0.
[6] RAT value set using the SMC_BxTIM.RAT bits.

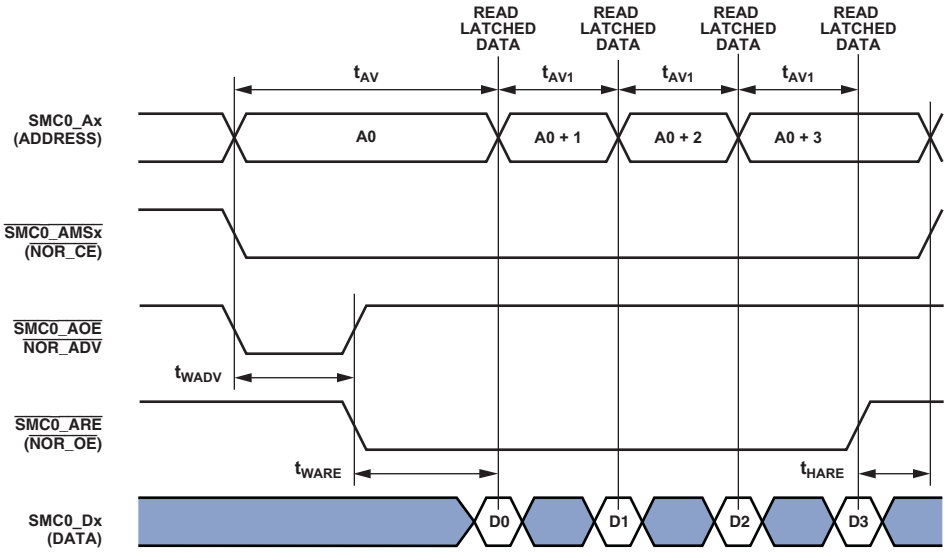


Figure 13. Asynchronous Page Mode Read

DDR2 SDRAM Write Cycle Timing

Table 41 and Figure 19 show DDR2 SDRAM write cycle timing, related to the dynamic memory controller (DMC).

Table 41. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1] Min	200 MHz[1] Max	Unit
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	–0.25	+0.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.15		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.275		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Output High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Output Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed.
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

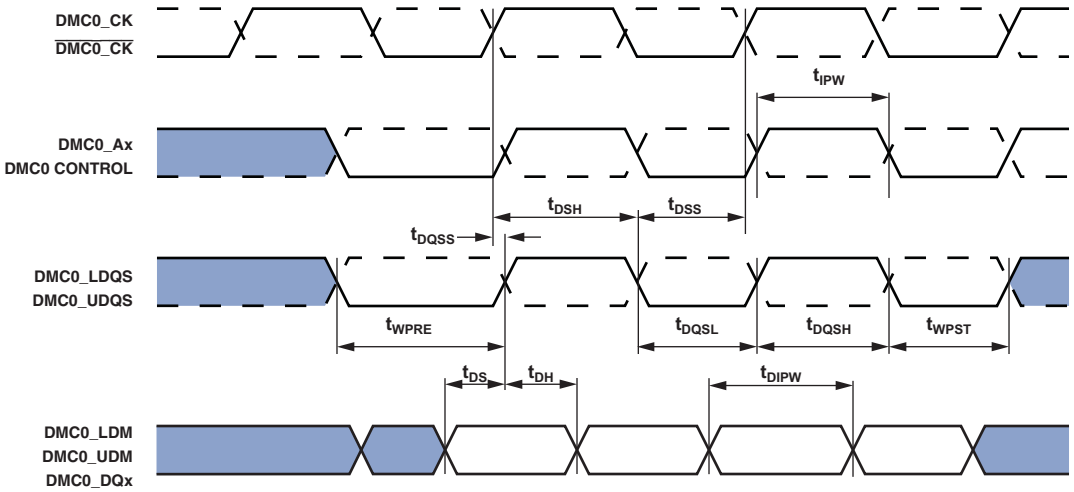


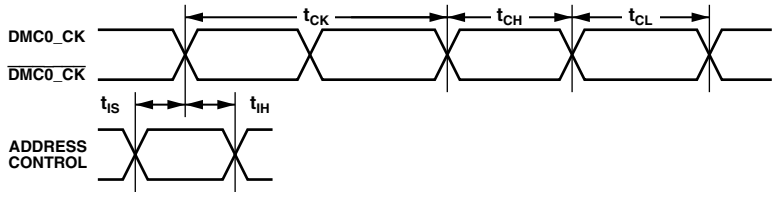
Figure 19. DDR2 SDRAM Controller Output AC Timing

Mobile DDR SDRAM Clock and Control Cycle Timing

Table 42 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the dynamic memory controller (DMC).

Table 42. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1.5		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1.5		ns



NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–2.

Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Write Cycle Timing

Table 44 and Figure 22 show mobile DDR SDRAM write cycle timing, related to the dynamic memory controller (DMC).

Table 44. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{DQSS}[1]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	1.8		ns

[1] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

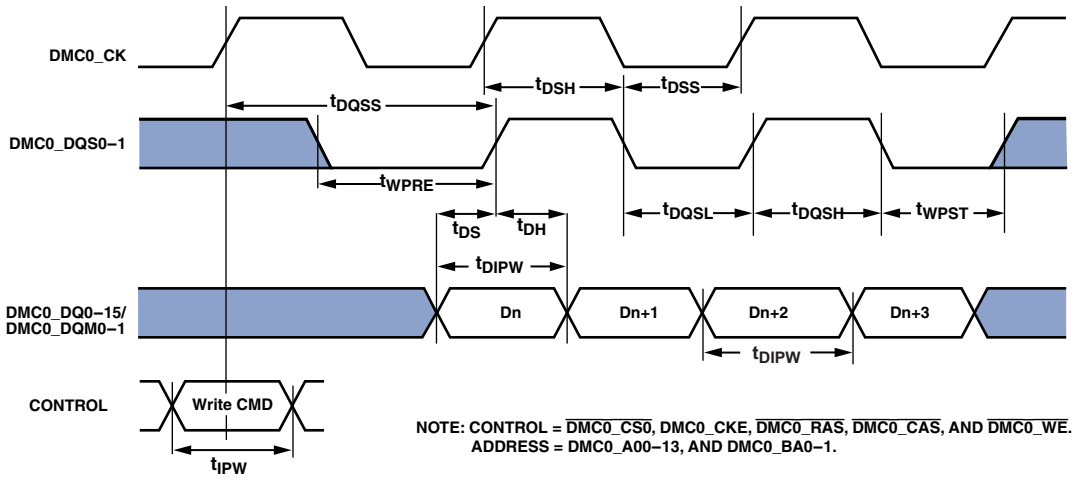


Figure 22. Mobile DDR SDRAM Controller Output AC Timing

Up/Down Counter/Rotary Encoder Timing

Table 47 and Figure 25 describe timing, related to the general-purpose counter (CNT).

Table 47. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirement						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		$2 \times t_{SCLK0}$		ns

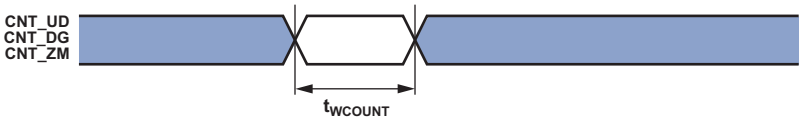


Figure 25. Up/Down Counter/Rotary Encoder Timing

Debug Interface (JTAG Emulation Port) Timing

Table 48 and Figure 26 provide I/O timing, related to the debug interface (JTAG emulator port).

Table 48. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	5		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	4		4		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK Cycles)[2]	4		4		t_{TCK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		16.5		14.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		18		16.5	ns
t_{DTMS}	TMS Delay After TCK High in SWD Mode	3.5	16.5	3.5	14.5	ns

[1] System inputs = DMC0_DQxx, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_xx, PB_xx, PC_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA, and SYS_EXTWAKE.

[2] 50 MHz maximum.

[3] System outputs = DMC0_Axx, DMC0_BAx, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, PA_xx, PB_xx, PC_xx, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$, and $\overline{\text{SYS\_NMI}}$.

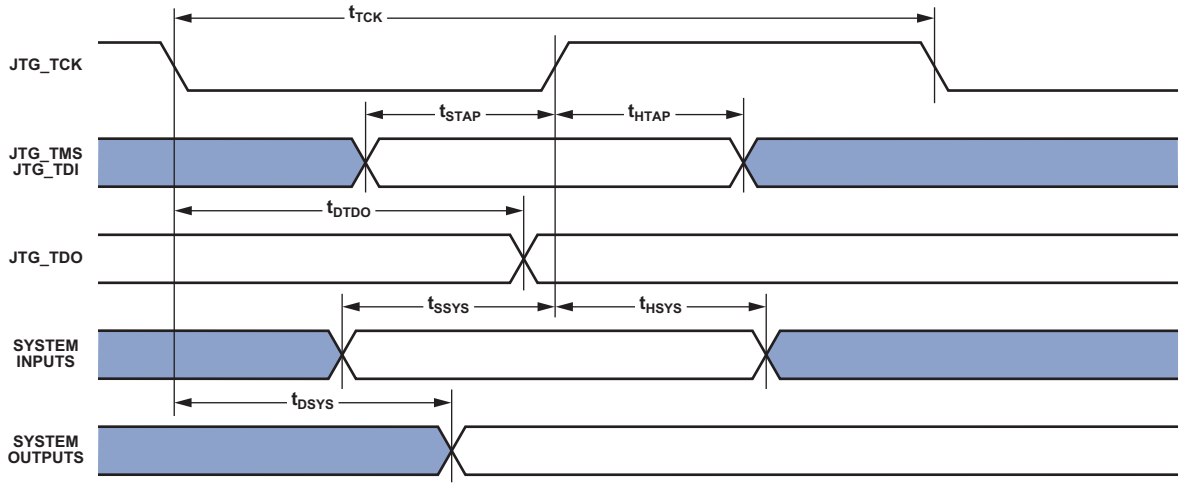


Figure 26. JTAG Port Timing

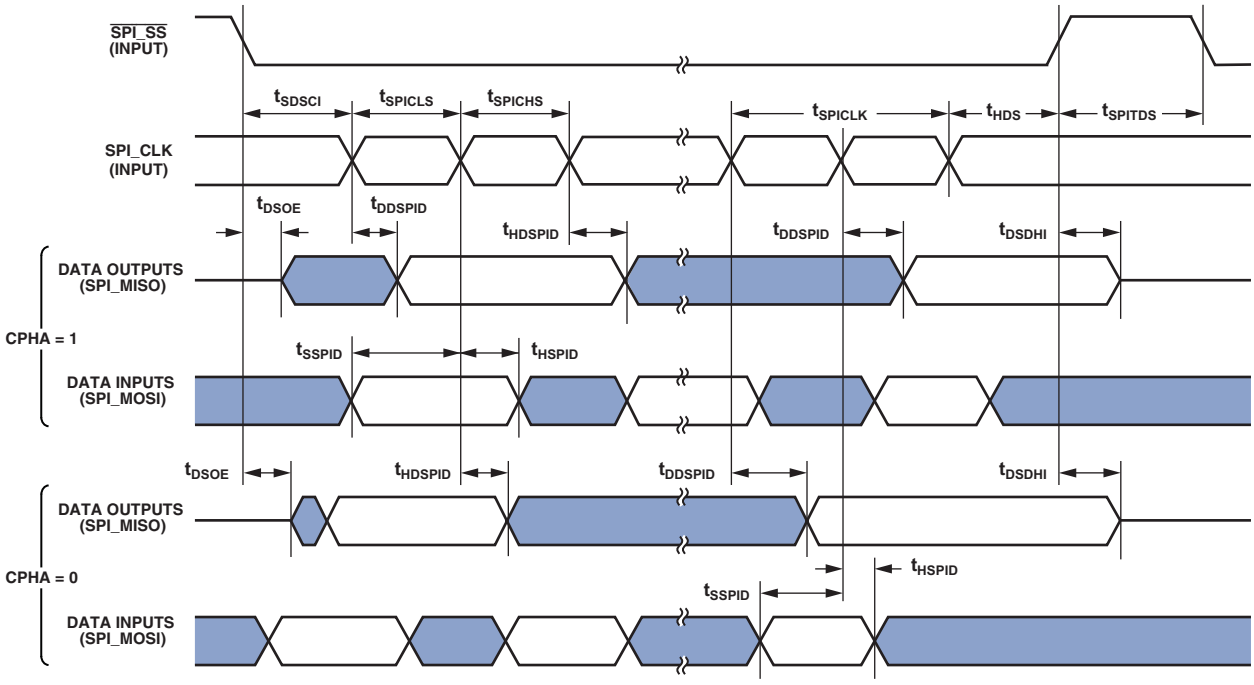


Figure 32. Serial Peripheral Interface (SPI) Port—Slave Timing

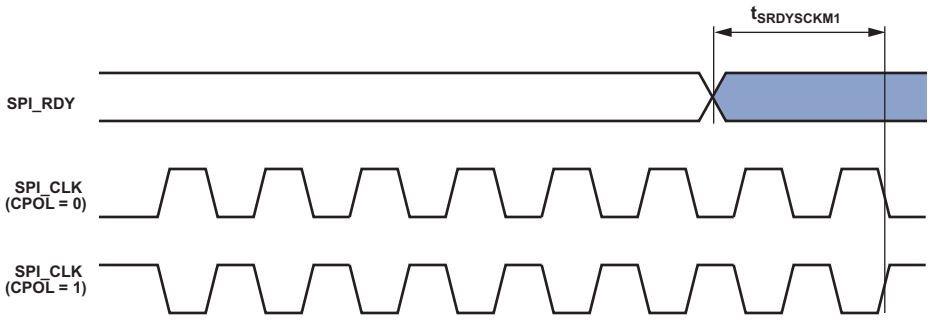


Figure 38. SPI_RDY Setup Before SPI_CLK with CPHA = 1

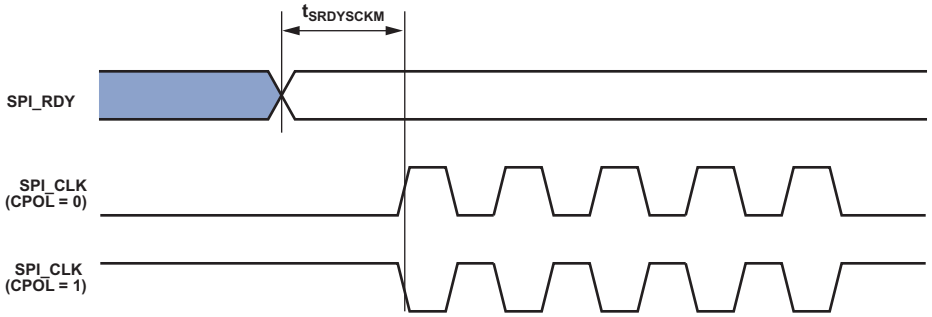


Figure 39. SPI_CLK Switching Diagram after SPI_RDY Assertion, CPHA = x

Table 61. Enhanced Parallel Peripheral Interface—External Clock

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Timing Requirements						
t_{PCLKW}	EPPI_CLK Width[1]	$(0.5 \times t_{PCLKEXT}) - 1$		$(0.5 \times t_{PCLKEXT}) - 1$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKEXT} - 1$		$t_{PCLKEXT} - 1$		ns
t_{SFSPE}	External FS Setup Before EPPI_CLK	1.5		1		ns
t_{HFSPE}	External FS Hold After EPPI_CLK	3.3		3		ns
t_{SDRPE}	Receive Data Setup Before EPPI_CLK	1		1		ns
t_{HDRPE}	Receive Data Hold After EPPI_CLK	3		3		ns
Switching Characteristics						
t_{DFSPE}	Internal FS Delay After EPPI_CLK		17.5		14.5	ns
t_{HOFSPE}	Internal FS Hold After EPPI_CLK	2.5		2.5		ns
t_{DDTPE}	Transmit Data Delay After EPPI_CLK		17.5		14.5	ns
t_{HDTPE}	Transmit Data Hold After EPPI_CLK	2.5		2.5		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external EPPI_CLK. For the external EPPI_CLK ideal maximum frequency, see the $f_{PCLKEXT}$ specification in Table 18 on Page 52 in Clock Related Operating Conditions.

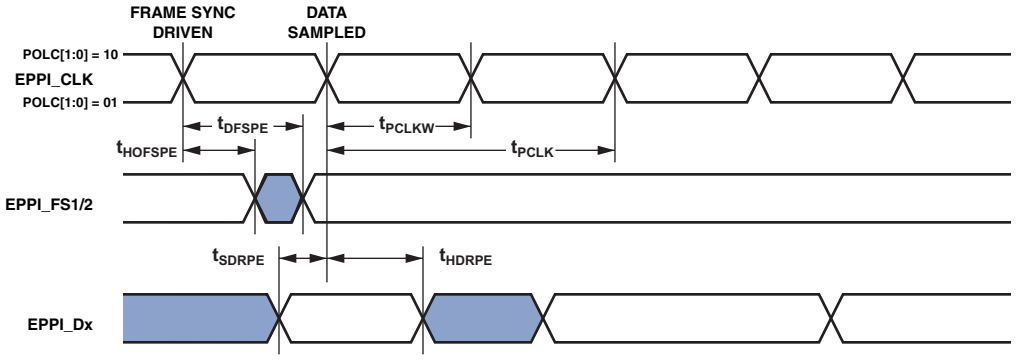


Figure 45. PPI External Clock GP Receive Mode with Internal Frame Sync Timing

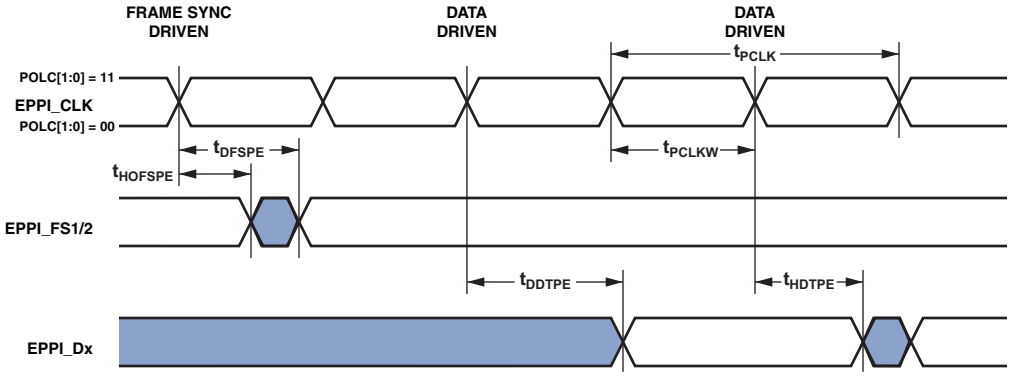


Figure 46. PPI External Clock GP Transmit Mode with Internal Frame Sync Timing

OUTPUT DRIVE CURRENTS

Figure 50 through Figure 61 show typical current-voltage characteristics for the output drivers of the ADSP-BF70x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

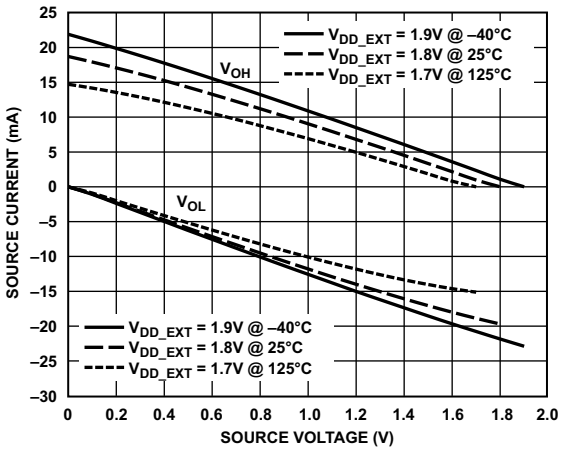


Figure 50. Driver Type A Current (1.8 V V_{DD_EXT})

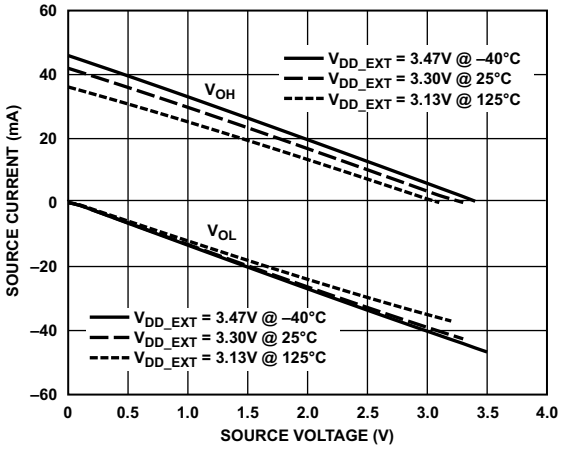


Figure 51. Driver Type A Current (3.3 V V_{DD_EXT})

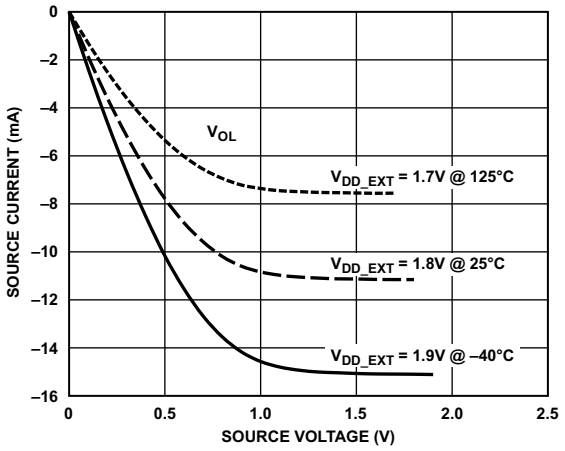


Figure 52. Driver Type D Current (1.8 V V_{DD_EXT})

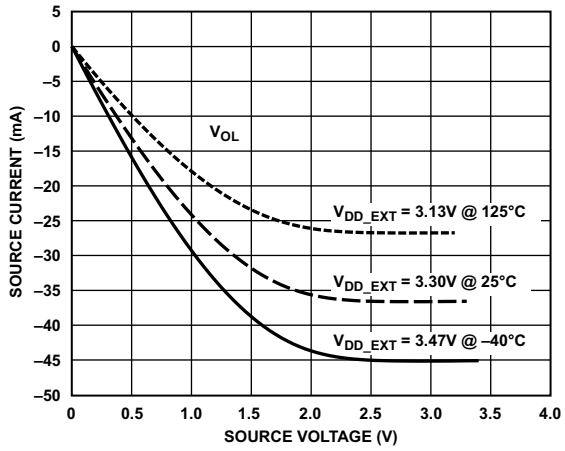


Figure 53. Driver Type D Current (3.3 V V_{DD_EXT})

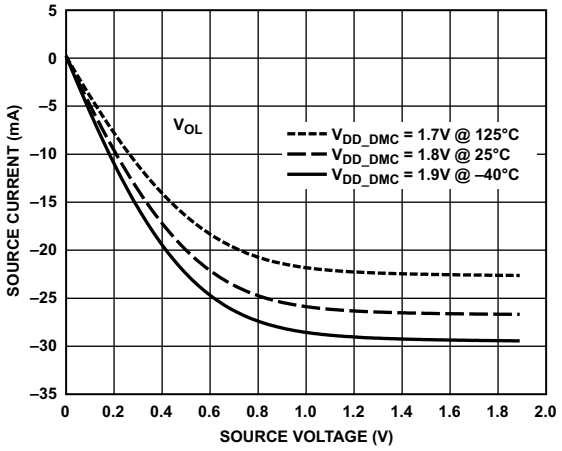


Figure 54. Driver Type B and Driver Type C (DDR Drive Strength 34 Ω)

ADSP-BF70x 184-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Figure 69 shows an overview of signal placement on the 184-ball CSP_BGA.

Table 67 lists the 184-ball CSP_BGA package by ball number for the ADSP-BF70x. Table 68 lists the 184-ball CSP_BGA package by signal.

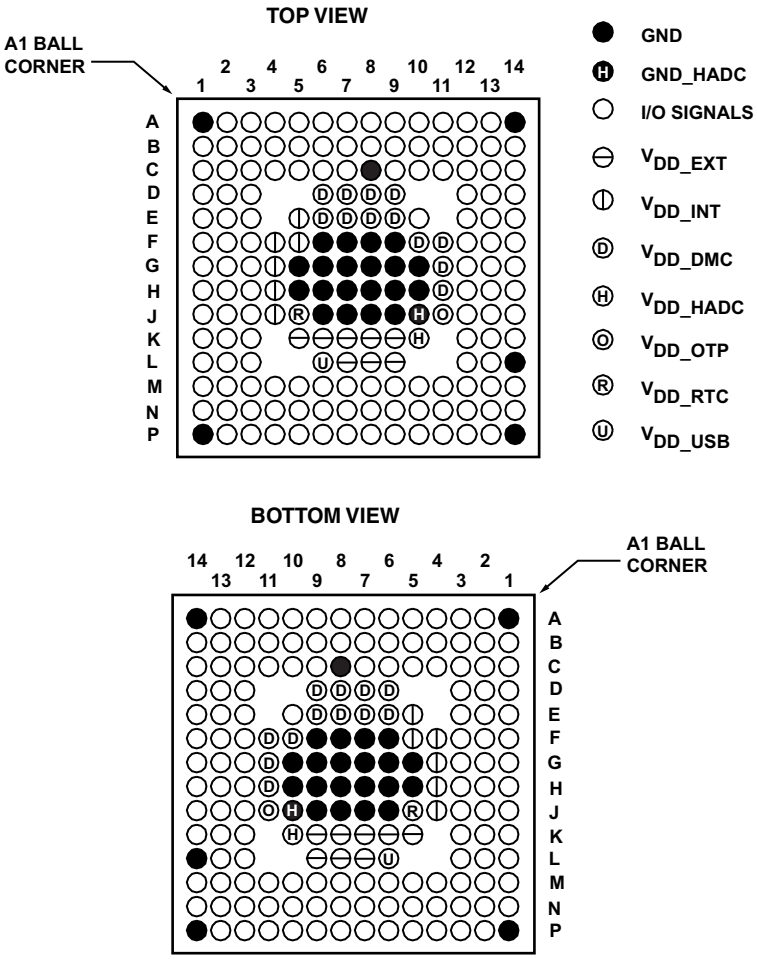


Figure 69. 184-Ball CSP_BGA Configuration

ADSP-BF70x 12 mm × 12 mm 88-LEAD LFCSP (QFN) LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

Figure 70 shows an overview of signal placement on the 12 mm × 12 mm 88-lead LFCSP (QFN).

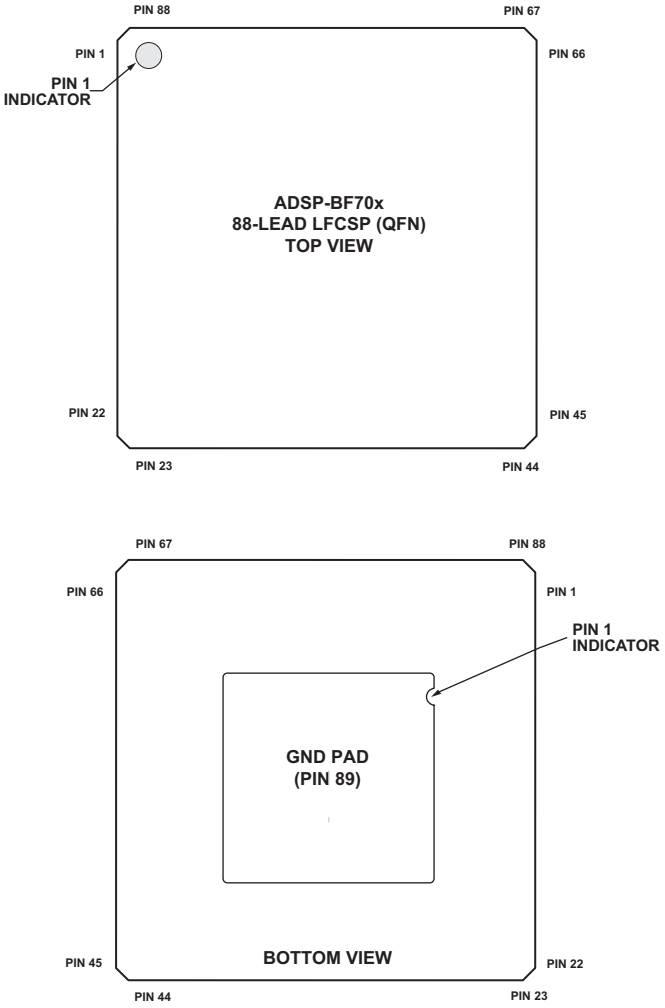


Figure 70. 12 mm × 12 mm 88-Lead LFCSP (QFN) Configuration