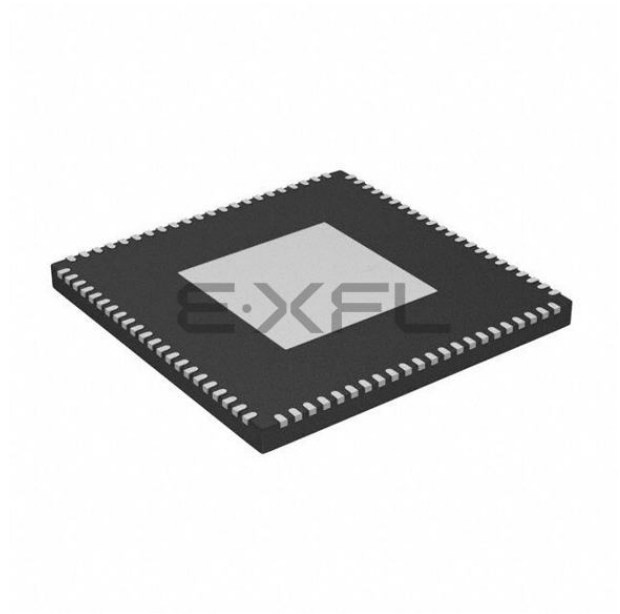

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	400MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	1MB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf706kcpz-4

BLACKFIN+ PROCESSOR CORE

As shown in Figure 1, the processor integrates a Blackfin+ processor core. The core, shown in Figure 2, contains two 16-bit multipliers, one 32-bit multiplier, two 40-bit accumulators (which may be used together as a 72-bit accumulator), two 40-bit ALUs, one 72-bit ALU, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

The core can perform two 16-bit by 16-bit multiply-accumulates or one 32-bit multiply-accumulate in each cycle. Signed and unsigned formats, rounding, saturation, and complex multiplies are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If a second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

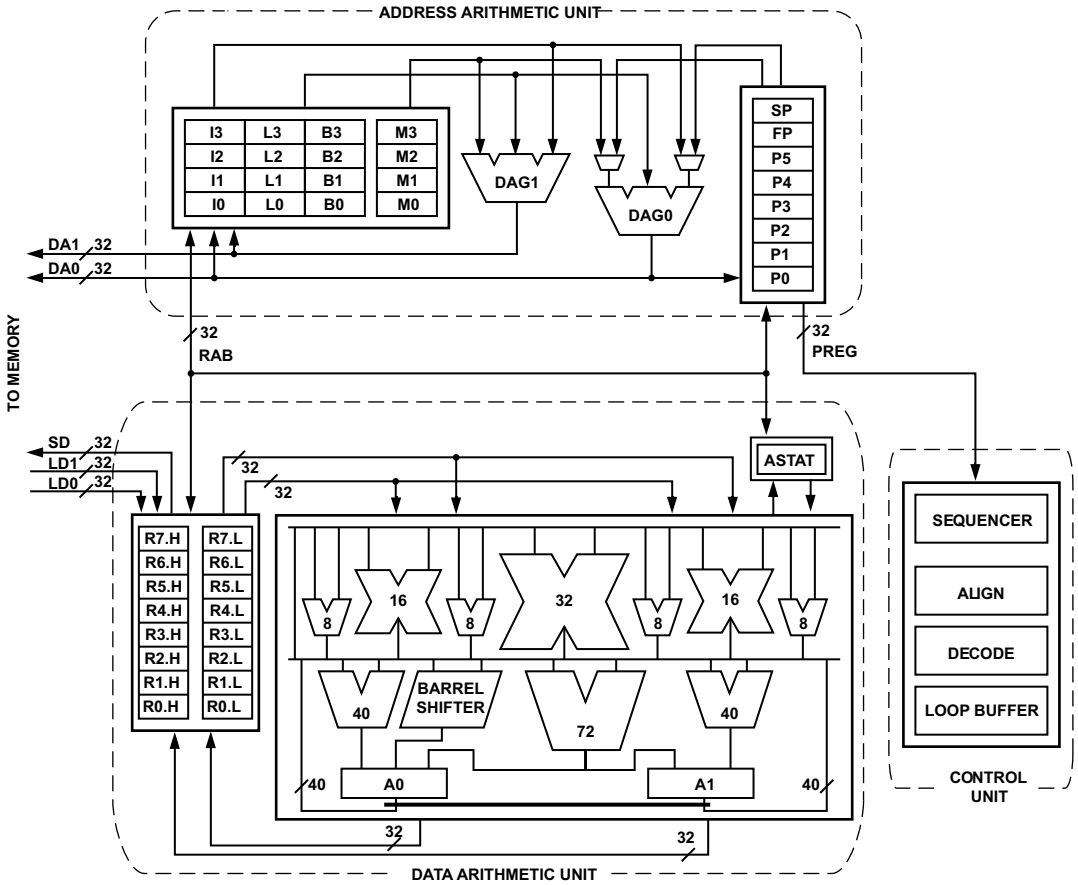


Figure 2. Blackfin+ Processor Core

system event or fault if enabled. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

CRC-Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can be used to protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even L3 memories (DDR2, LPDDR). The processor features two CRC engines which are embedded in the memory-to-memory DMA controllers. CRC checksums can be calculated or compared on the fly during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Memory Protection

The Blackfin+ core features a memory protection concept, which grants data and/or instruction accesses to enabled memory regions only. A supervisor mode vs. user mode programming model supports dynamically varying access rights. Increased flexibility in memory page size options supports a simple method of static memory partitioning.

System Protection

The system protection unit (SPU) guards against accidental or unwanted access to the MMR space of a peripheral by providing a write-protection mechanism. The user is able to choose and configure the peripherals that are protected as well as configure which ones of the four system MMR masters (core, memory DMA, the SPI host port, and Coresight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write-protection functionality, the SPU is employed to define which resources in the system are secure or non-secure and to block access to secure resources from non-secure masters.

Synonymously, the system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are two SMPU units in the ADSP-BF70x processors. One is for the L2 memory and the other is for the external DDR memory.

The SMPU is also part of the security infrastructure. It allows the user to not only protect against arbitrary read and/or write transactions, but it also allows regions of memory to be defined as secure and prevent non-secure masters from accessing those memory regions.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or the core executes from user-defined addresses. Watchpoint events can be configured such that they signal the events to the fault management unit of the SEC.

Watchdog

The on-chip software watchdog timer can supervise the Blackfin+ core.

Bandwidth Monitor

Memory-to-memory DMA channels are equipped with a bandwidth monitor mechanism. They can signal a system event or fault when transactions tend to starve because system buses are fully loaded with higher-priority traffic.

Signal Watchdogs

The eight general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help to detect undesired toggling (or lack thereof) of system-level signals.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the GP counter can flag this to the processor or to the fault management unit of the SEC.

Fault Management

The fault management unit is part of the system event controller (SEC). Any system event, whether a dual-bit uncorrectable ECC error, or any peripheral status interrupt, can be defined as being a fault. Additionally, the system events can be defined as an interrupt to the core. If defined as such, the SEC forwards the event to the fault management unit, which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken through a keyed sequence, to provide a final chance for the Blackfin+ core to resolve the issue and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core through several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). The processor contains high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not previously described.

Timers

The processor includes several timers which are described in the following sections.

Table 3. Clock Dividers

Clock Source	Divider (if Available on SYS_CLKOUT)
CCLK (Core Clock)	By 16
SYSCLK (System Clock)	By 8
SCLK0 (System Clock, All Peripherals not Covered by SCLK1)	Not available on SYS_CLKOUT
SCLK1 (System Clock for Crypto Engines and MDMA)	By 8
DCLK (LPDDR/DDR2 Clock)	By 8
OCLK (Output Clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports multiple power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
OTP Memory	V_{DD_OTP}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
All Other I/O (Includes SYS, JTAG, and Ports Pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

See Table 5 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core and to all of the peripherals. This setting signals the external voltage regulator supplying the VDD_INT pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation.

Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a nonvolatile storage device (or self-refreshed DRAM) prior to removing power if the processor state is to be preserved.

Because the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or the core and is the result of a hardware- or software-triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with the core being ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when the core is reset (programs must ensure that there is no pending system activity involving the core when it is being reset).

From a system perspective, reset is defined by both the reset target and the reset source described as follows in the following list.

ADSP-BF70x DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-BF70x Detailed Signal Descriptions

Port Name	Direction	Description
CAN_RX	Input	**Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver's TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal Count Down - This input causes the GP counter to decrement Gate - Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal Count Up - This input causes the GP counter to increment Direction - Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DMC_Ann	Output	**Address n.** Address bus.
DMC_BAn	Output	**Bank Address Input n.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to on the dynamic memory. Also defines which mode registers (MR, EMR, EMR2, and/or EMR3) are loaded during the LOAD MODE REGISTER command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock enable.** Active high clock enables. Connects to the dynamic memory's CKE input.
$\overline{\text{DMC\_CSn}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQnn	I/O	**Data n.** Bidirectional Data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	I/O	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	I/O	**Data Strobe for Lower Byte (complement).** Complement of LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On-die termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled/disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	I/O	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with Write Data. Input with Read Data. May be single-ended or differential depending on register settings.
$\overline{\text{DMC\_UDQS}}$	I/O	**Data Strobe for Upper Byte (complement).** Complement of UDQSb. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connect to half of the VDD_DMC voltage.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
PPI_CLK	I/O	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_Dnn	I/O	**Data n.** Bidirectional data bus.
PPI_FS1	I/O	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS2	I/O	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
PPI_FS3	I/O	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI HRM chapter for more details.
HADC_VINn	Input	**Analog Input at channel n.** Analog voltage inputs for digital conversion.

Table 6. ADSP-BF70x Detailed Signal Descriptions (Continued)

Port Name	Direction	Description
SPT_BCLK	I/O	**Channel B Clock.** Data and Frame Sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BD1	I/O	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BFS	I/O	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SYS_BMODEn	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN	Input	**Clock/Crystal Input.** Connect to an external clock source or crystal.
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the HRM for more details.
SYS_EXTWAKE	Output	**External Wake Control.** Drives low during hibernate and high all other times. Typically connected to the enable input of the voltage regulator controlling the VDD_INT supply.
$\overline{\text{SYS\_FAULT}}$	I/O	**Active-Low Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_NMI}}$	Input	**Non-maskable Interrupt.** See the processor hardware and programming references for more details.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates that the device is in the reset or hibernate state.
SYS_WAKEn	Input	**Power Saving Mode Wakeup n.** Wake-up source input for deep sleep and/or hibernate mode.
SYS_XTAL	Output	**Crystal Output.** Drives an external crystal. Must be left unconnected if an external clock is driving CLKIN.
JTG_SWCLK	I/O	**Serial Wire Clock.** Clocks data into and out of the target during debug.
JTG_SWDIO	I/O	**Serial Wire DIO.** Sends and receives serial data to and from the target during debug.
JTG_SWO	Output	**Serial Wire Out.** Provides trace data to the emulator.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
TM_ACIn	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLKn	Input	**Alternate Clock n.** Provides an additional time base for use by an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for use by all the GP timers.
TM_TMRn	I/O	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_Dnn	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	I/O	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	I/O	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receive input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmit output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input.** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.

12 mm × 12 mm 88-LEAD LFCSP (QFN) SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 11. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions

Signal Name	Description	Port	Pin Name
CAN0_RX	CAN0 Receive	C	PC_02
CAN0_TX	CAN0 Transmit	C	PC_03
CAN1_RX	CAN1 Receive	A	PA_12
CAN1_TX	CAN1 Transmit	A	PA_13
CNT0_DG	CNT0 Count Down and Gate	A	PA_07
CNT0_UD	CNT0 Count Up and Direction	A	PA_15
CNT0_ZM	CNT0 Count Zero Marker	A	PA_13
GND	Ground	Not Muxed	GND
JTG_SWCLK	TAPC0 Serial Wire Clock	Not Muxed	JTG_TCK_SWCLK
JTG_SWDIO	TAPC0 Serial Wire DIO	Not Muxed	JTG_TMS_SWDIO
JTG_SWO	TAPC0 Serial Wire Out	Not Muxed	JTG_TDO_SWO
JTG_TCK	TAPC0 JTAG Clock	Not Muxed	JTG_TCK_SWCLK
JTG_TDI	TAPC0 JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	TAPC0 JTAG Serial Data Out	Not Muxed	JTG_TDO_SWO
JTG_TMS	TAPC0 JTAG Mode Select	Not Muxed	JTG_TMS_SWDIO
$\overline{\text{JTG\_TRST}}$	TAPC0 JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
$\overline{\text{MSI0\_CD}}$	MSI0 Card Detect	A	PA_08
MSI0_CLK	MSI0 Clock	C	PC_09
MSI0_CMD	MSI0 Command	C	PC_05
MSI0_D0	MSI0 Data 0	C	PC_08
MSI0_D1	MSI0 Data 1	C	PC_04
MSI0_D2	MSI0 Data 2	C	PC_07
MSI0_D3	MSI0 Data 3	C	PC_06
MSI0_D4	MSI0 Data 4	C	PC_10
PA_00-PA_15	Position 00 through Position 15	A	PA_00-PA_15
PB_00-PB_15	Position 00 through Position 15	B	PB_00-PB_15
PC_00-PC_10	Position 00 through Position 10	C	PC_00-PC_10
PPI0_CLK	EPPI0 Clock	A	PA_14
PPI0_D00	EPPI0 Data 0	B	PB_07
PPI0_D01	EPPI0 Data 1	B	PB_06
PPI0_D02	EPPI0 Data 2	B	PB_05
PPI0_D03	EPPI0 Data 3	B	PB_04
PPI0_D04	EPPI0 Data 4	B	PB_03
PPI0_D05	EPPI0 Data 5	B	PB_02
PPI0_D06	EPPI0 Data 6	B	PB_01
PPI0_D07	EPPI0 Data 7	B	PB_00

Table 11. ADSP-BF70x 12 mm × 12 mm 88-Lead LFCSP (QFN) Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D08	EPPI0 Data 8	A	PA_11
PPI0_D09	EPPI0 Data 9	A	PA_10
PPI0_D10	EPPI0 Data 10	A	PA_09
PPI0_D11	EPPI0 Data 11	A	PA_08
PPI0_D12	EPPI0 Data 12	C	PC_03
PPI0_D13	EPPI0 Data 13	C	PC_02
PPI0_D14	EPPI0 Data 14	C	PC_01
PPI0_D15	EPPI0 Data 15	C	PC_00
PPI0_D16	EPPI0 Data 16	B	PB_08
PPI0_D17	EPPI0 Data 17	B	PB_09
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	A	PA_12
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	A	PA_13
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	A	PA_15
RTC0_CLKIN	RTC0 Crystal input/external oscillator connection	Not Muxed	RTC0_CLKIN
RTC0_XTAL	RTC0 Crystal output	Not Muxed	RTC0_XTAL
SMC0_A01	SMC0 Address 1	A	PA_08
SMC0_A02	SMC0 Address 2	A	PA_09
SMC0_A03	SMC0 Address 3	A	PA_10
SMC0_A04	SMC0 Address 4	A	PA_11
SMC0_A05	SMC0 Address 5	A	PA_07
SMC0_A06	SMC0 Address 6	A	PA_06
SMC0_A07	SMC0 Address 7	A	PA_05
SMC0_A08	SMC0 Address 8	A	PA_04
SMC0_A09	SMC0 Address 9	C	PC_01
SMC0_A10	SMC0 Address 10	C	PC_02
SMC0_A11	SMC0 Address 11	C	PC_03
SMC0_A12	SMC0 Address 12	C	PC_04
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	A	PA_00
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	A	PA_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	A	PA_15
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	A	PA_02
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	A	PA_12
SMC0_ARDY	SMC0 Asynchronous Ready	A	PA_03
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	A	PA_13
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	A	PA_14
SMC0_D00	SMC0 Data 0	B	PB_07
SMC0_D01	SMC0 Data 1	B	PB_06
SMC0_D02	SMC0 Data 2	B	PB_05
SMC0_D03	SMC0 Data 3	B	PB_04
SMC0_D04	SMC0 Data 4	B	PB_03
SMC0_D05	SMC0 Data 5	B	PB_02
SMC0_D06	SMC0 Data 6	B	PB_01
SMC0_D07	SMC0 Data 7	B	PB_00
SMC0_D08	SMC0 Data 8	B	PB_08
SMC0_D09	SMC0 Data 9	B	PB_09
SMC0_D10	SMC0 Data 10	B	PB_10

Table 14. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	$\overline{\text{UART1\_TX}}$	SPT0_AD1	PPI0_D15		
PC_01	$\overline{\text{UART1\_RX}}$	SPT0_BD1	PPI0_D14	SMC0_A09	TM0_ACI4
PC_02	$\overline{\text{UART0\_RTS}}$	CAN0_RX	PPI0_D13	SMC0_A10	TM0_ACI5/SYS_ WAKE3
PC_03	$\overline{\text{UART0\_CTS}}$	CAN0_TX	PPI0_D12	SMC0_A11	TM0_ACI0
PC_04	SPT0_BCLK	SPI0_CLK	MSI0_D1	SMC0_A12	TM0_ACLK0
PC_05	SPT0_AFS	TM0_TMR3	MSI0_CMD		
PC_06	SPT0_BD0	SPI0_MISO	MSI0_D3		
PC_07	SPT0_BFS	SPI0_MOSI	MSI0_D2		TM0_ACI2
PC_08	SPT0_AD0	SPI0_D2	MSI0_D0		
PC_09	SPT0_ACLK	SPI0_D3	MSI0_CLK		TM0_ACLK2
PC_10	SPT1_BCLK	MSI0_D4	$\overline{\text{SPI1\_SEL3}}$		TM0_ACLK1

Table 18. Peripheral Clock Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{OCLK}	Output Clock Frequency				50	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[1, 2]			±2		%
$f_{PCLKPROG}$	Programmed PPI Clock When Transmitting Data and Frame Sync				50	MHz
$f_{PCLKPROG}$	Programmed PPI Clock When Receiving Data or Frame Sync				50	MHz
$f_{PCLKEXT}$	External PPI Clock When Receiving Data and Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{PCLKEXT}$	External PPI Clock Transmitting Data or Frame Sync[3, 4]	$f_{PCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync[3, 4]	$f_{SPTCLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[3, 4]	$f_{SPICLKEXT} \le f_{SCLK0}$			50	MHz
$f_{MSICLKPROG}$	Programmed MSI Clock				50	MHz

[1] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this typical specification for each end application.
[2] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[3] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications section for that peripheral. Pay particular attention to setup and hold times for VDD_EXT = 1.8 V which may preclude the maximum frequency listed here.
[4] The peripheral external clock frequency must also be less than or equal to the f_{SCLK} that clocks the peripheral.

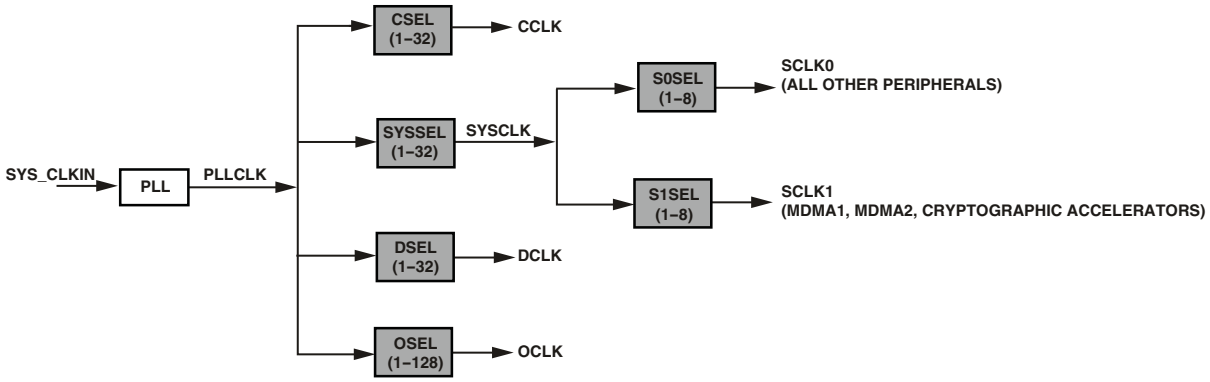


Figure 6. Clock Relationships and Divider Values

Table 19. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	230.2	800	MHz
CGU_CTL.MSEL[1]	PLL Multiplier	8	41	

[1] The CGU_CTL.MSEL setting must also be chosen to ensure that the f_{PLLCLK} specification is not violated.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0		33		µA
$I_{DD\_HIBERNATE}$[17, 19]	Hibernate State Current Without USB	V_{DD_INT} = 0 V, V_{DD_DMC} = 1.8 V, V_{DD_EXT} = V_{DD_HADC} = V_{DD_OTP} = V_{DD_RTC} = V_{DD_USB} = 3.3 V, T_J = 25°C, f_{CLKIN} = 0, USB protection disabled (USB_PHY_CTLDIS = 1)		15		µA
I_{DD_INT}[18]	V_{DD_INT} Current	V_{DD_INT} within operating conditions table specifications			See I_{DDINT_TOT} equation on on Page 56	mA
I_{DD_RTC}	I_{DD_RTC} Current	V_{DD_RTC} = 3.3 V, T_J = 125°C			10	µA

[1] Applies to all output and bidirectional signals except DMC0 signals, TWI signals, and USB0 signals.

[2] Applies to DMC0_Axx, DMC0_CAS, DMC0_CKE, DMC0_CK, DMC0_CK, DMC0_CS, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, DMC0_LDQS, DMC0_ODT, DMC0_RAS, DMC0_UDM, DMC0_UDQS, DMC0_UDQS, and DMC0_WE signals.

[3] Applies to all output and bidirectional signals except DMC0 signals and USB0 signals.

[4] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TDI, and JTG_TMS_SWDIO signals.

[5] Applies to DMC0_VREF signal.

[6] Applies to JTG_TCK_SWCLK and JTG_TRST signals.

[7] Applies to SMC0_ARDY, SYS_BMODEx, SYS_CLKIN, SYS_HWRST, JTG_TCK, and JTG_TRST signals.

[8] Applies to JTG_TDI, JTG_TMS_SWDIO, PA_xx, PB_xx, and PC_xx signals when internal GPIO pull-ups are enabled. For information on when internal pull-ups are enabled for GPIOs. See ADSP-BF70x Designer Quick Reference on Page 38.

[9] Applies to USB0_CLKIN signal.

[10] Applies to PA_xx, PB_xx, PC_xx, SMC0_AMS0, SMC0_ARE, SMC0_AWE, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, and USB0_VBC signals.

[11] Applies to DMC0_Axx, DMC0_BAxx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, and DMC0_WE signals.

[12] Applies to PA_xx, PB_xx, PC_xx, SMC0_A0E, SMC0_Axx, SMC0_Dxx, SYS_FAULT, JTG_TDO_SWO, USB0_DM, USB0_DP, USB0_ID, USB0_VBC, USB0_VBUS, DMC0_Axx, DMC0_BAx, DMC0_CAS, DMC0_CS0, DMC0_DQxx, DMC0_LDQS, DMC0_LDQS, DMC0_UDQS, DMC0_UDQS, DMC0_LDM, DMC0_UDM, DMC0_ODT, DMC0_RAS, DMC0_WE, and TWI signals.

[13] Applies to USB0_VBUS signals.

[14] Applies to all TWI signals.

[15] Applies to all signals, except DMC0 and TWI signals.

[16] Applies to all DMC0 signals.

[17] See the *ADSP-BF70x Blackfin+ Processor Hardware Reference* for definition of deep sleep and hibernate operating modes.

[18] Additional information can be found at Total Internal Power Dissipation.

[19] Applies to VDD_EXT, VDD_DMC, and VDD_USB supply signals only. Clock inputs are tied high or low.

Power-Up Reset Timing

A power-up reset is required to place the processor in a known state after power-up. A power-up reset is initiated by asserting $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$. During power-up reset, all pins are high impedance except for those noted in the ADSP-BF70x Designer Quick Reference on Page 38.

Both $\overline{\text{JTG\_TRST}}$ and $\overline{\text{SYS\_HWRST}}$ need to be asserted upon power-up, but only $\overline{\text{SYS\_HWRST}}$ needs to be released for the device to boot properly. $\overline{\text{JTG\_TRST}}$ may be asserted indefinitely for normal operation. $\overline{\text{JTG\_TRST}}$ only needs to be released when using an emulator to connect to the DAP for debug or boundary scan. There is an internal pull-down on $\overline{\text{JTG\_TRST}}$ to ensure internal emulation logic will always be properly initialized during power-up reset.

Table 30 and Figure 9 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU). In Figure 9, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, and V_{DD_HADC}.

There is no power supply sequencing requirement for the ADSP-BF70x processor. However, if saving power during power-on is important, bringing up V_{DD_INT} last is recommended. This avoids a small current drain in the V_{DD_INT} domain during the transition period of I/O voltages from 0 V to within the voltage specification.

Table 30. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ Deasserted After V_{DD_INT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_RTC}, V_{DD_OTP}, V_{DD_HADC}, and SYS_CLKIN are Stable and Within Specification	$11 \times t_{CKIN}$		ns
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (No External Pull-Down on $\overline{\text{JTG\_TRST}}$)	10		µs
t_{VDDEXT_RST}	$\overline{\text{SYS\_HWRST}}$ Deasserted After V_{DD_EXT} is Stable and Within Specifications (10k External Pull-Down on $\overline{\text{JTG\_TRST}}$)	1		µs

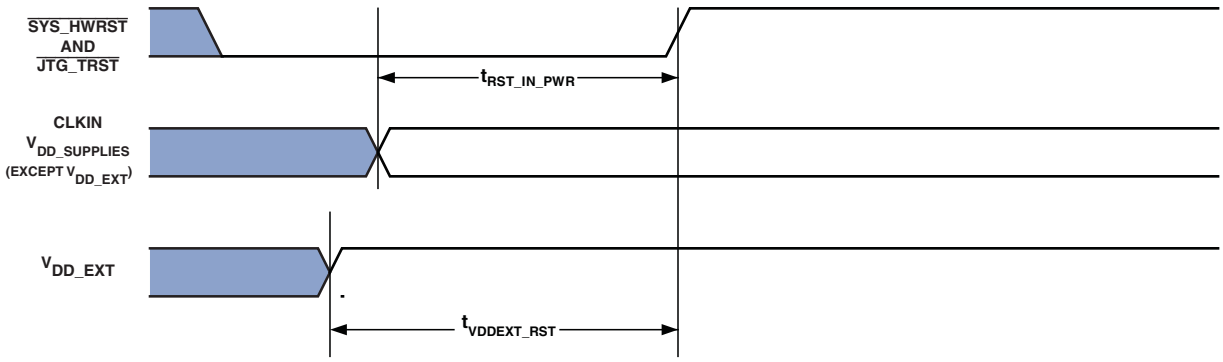


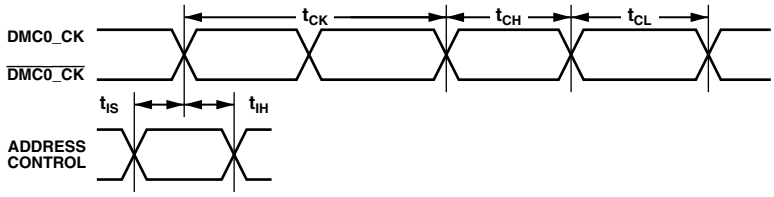
Figure 9. Power-Up Reset Timing

DDR2 SDRAM Clock and Control Cycle Timing

Table 39 and Figure 17 show DDR2 SDRAM clock and control cycle timing, related to the dynamic memory controller (DMC).

Table 39. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	High Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Low Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	350		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	475		ps



NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–2.

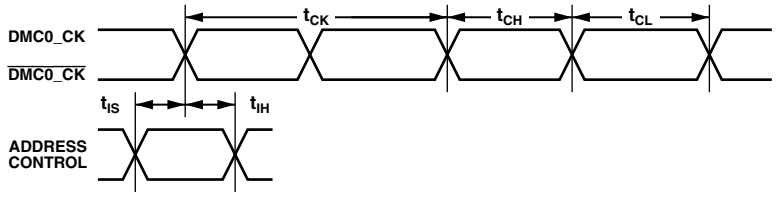
Figure 17. DDR2 SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Clock and Control Cycle Timing

Table 42 and Figure 20 show mobile DDR SDRAM clock and control cycle timing, related to the dynamic memory controller (DMC).

Table 42. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz Min	200 MHz Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1.5		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1.5		ns



NOTE: CONTROL = $\overline{\text{DMC0\_CS0}}$, DMC0_CKE, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_CAS}}$, AND $\overline{\text{DMC0\_WE}}$.
ADDRESS = DMC0_A00–13, AND DMC0_BA0–2.

Figure 20. Mobile DDR SDRAM Clock and Control Cycle Timing

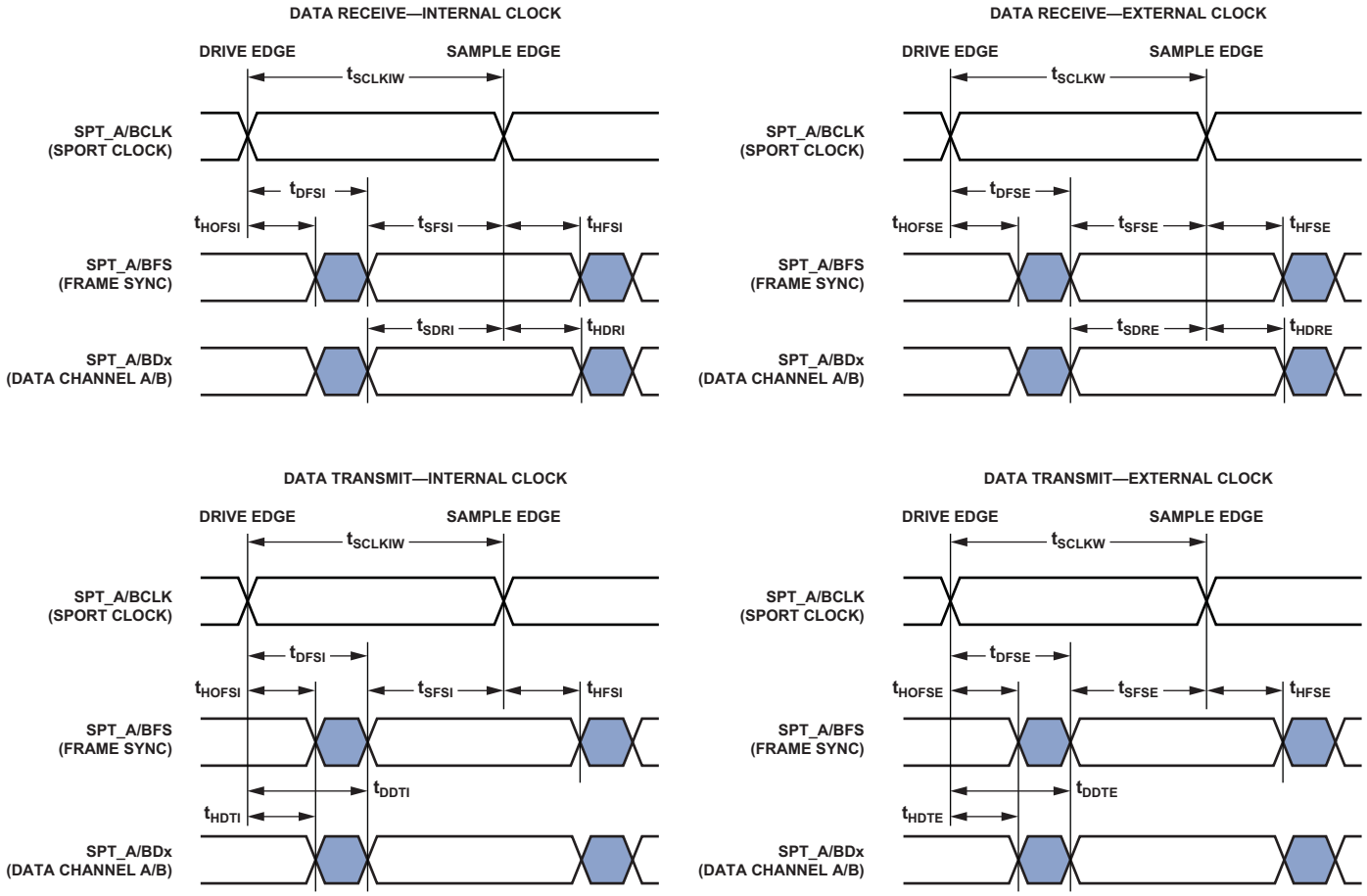


Figure 27. Serial Ports

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

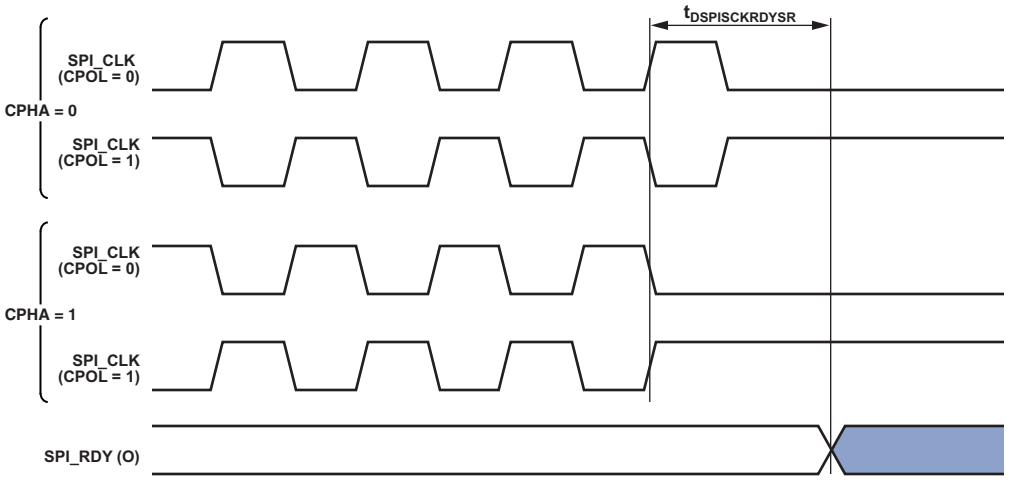


Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

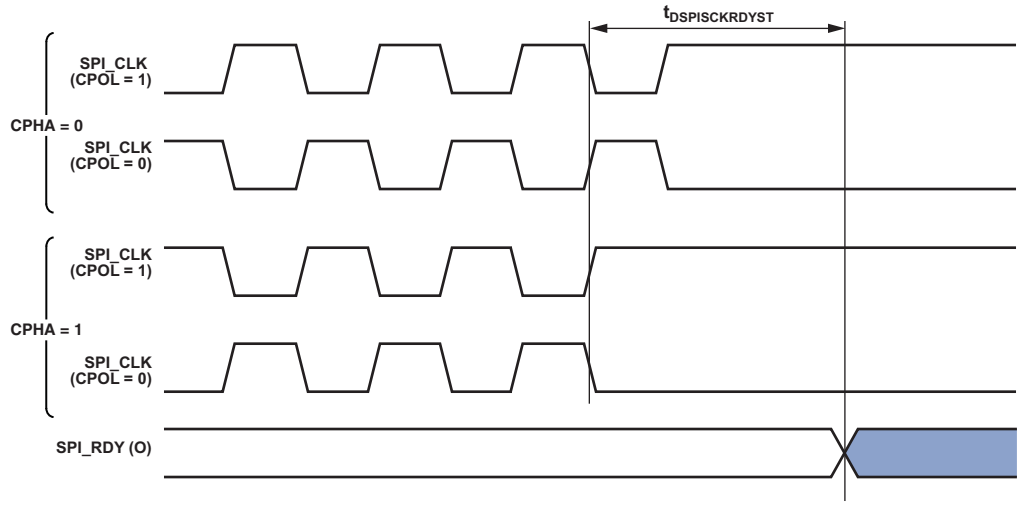


Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

Table 58. SPI Port—ODM Slave Mode

Parameter		V_{DD_EXT} 1.8 V Nominal Min	V_{DD_EXT} 1.8 V Nominal Max	V_{DD_EXT} 3.3 V Nominal Min	V_{DD_EXT} 3.3 V Nominal Max	Unit
Switching Characteristics						
$t_{HDSPIODMS}$	SPI_CLK Edge to High Impedance from Data Out Valid	2.5		2.5		ns
$t_{DDSPIODMS}$	SPI_CLK Edge to Data Out Valid from High Impedance		17.5		14.5	ns

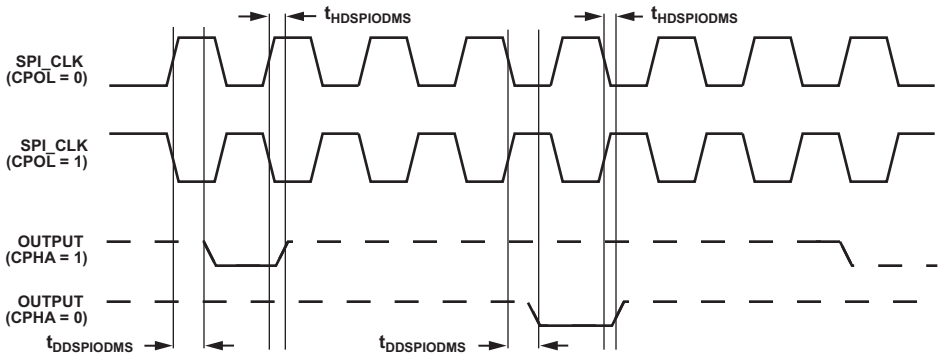


Figure 36. ODM Slave

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The universal asynchronous receiver-transmitter (UART) ports receive and transmit operations are described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Controller Area Network (CAN) Interface

The controller area network (CAN) interface timing is described in the *ADSP-BF70x Blackfin+ Processor Hardware Reference*.

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 62 describes the universal serial bus (USB) on-the-go receive and transmit operations.

Table 62. USB On-The-Go—Receive and Transmit Timing

		V_{DD_USB} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{USBS}	USB_XI Frequency	24	24	MHz
fs_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

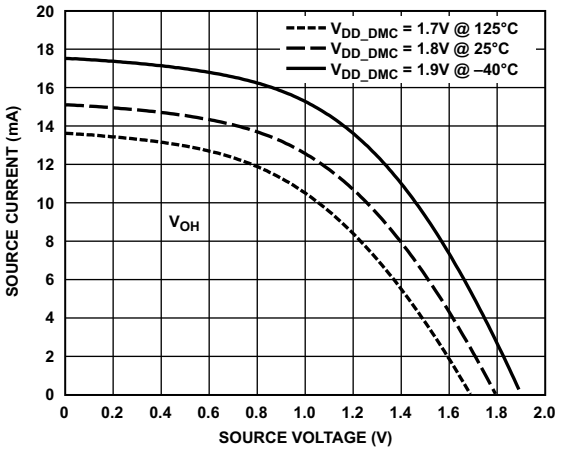


Figure 61. Driver Type B and Device Driver C (DDR Drive Strength 60 Ω)

TEST CONDITIONS

All timing requirements appearing in this data sheet were measured under the conditions described in this section. Figure 62 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 1.8 V/3.3 V.

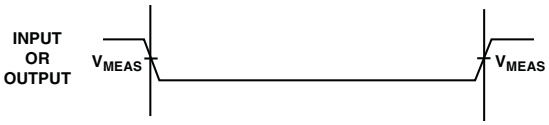


Figure 62. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output balls are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 63.

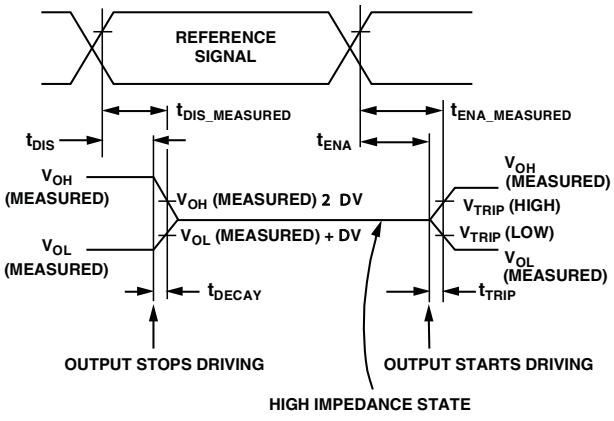


Figure 63. Output Enable/Disable

The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches V_{TRIP} (high) or V_{TRIP} (low). For V_{DD_EXT} (nominal) = 1.8 V, V_{TRIP} (high) is 1.05 V, and V_{TRIP} (low) is 0.75 V. For V_{DD_EXT} (nominal) = 3.3 V, V_{TRIP} (high) is 1.9 V, and V_{TRIP} (low) is 1.4 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple balls (such as the data bus) are enabled, the measurement value is that of the first ball to start driving.

Output Disable Time Measurement

Output balls are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 63.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DD_EXT} (nominal) = 3.3 V and 0.15 V for V_{DD_EXT} (nominal) = 1.8V.

The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 60.

Table 69 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by lead number for the ADSP-BF70x. Table 70 lists the 12 mm × 12 mm 88-Lead LFCSP (QFN) package by signal.

Table 69. 12 mm × 12 mm 88-Lead LFCSP (QFN) Lead Assignment (Numerical by Lead Number)

Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name	Lead No.	Signal Name
1	PC_10	24	PB_14	47	PB_02	70	PA_07
2	PC_09	25	PB_13	48	PB_01	71	PA_06
3	PC_08	26	VDD_EXT	49	VDD_OTP	72	VDD_EXT
4	VDD_EXT	27	PB_12	50	VDD_EXT	73	PA_05
5	PC_07	28	PB_11	51	VDD_INT	74	PA_04
6	PC_06	29	PB_10	52	PB_00	75	PA_03
7	PC_05	30	VDD_INT	53	PA_15	76	GND
8	PC_04	31	USB0_XTAL	54	PA_14	77	$\overline{\text{SYS\_NMI}}$
9	PC_03	32	USB0_CLKIN	55	VDD_EXT	78	PA_02
10	PC_02	33	USB0_ID	56	SYS_XTAL	79	SYS_EXTWAKE
11	VDD_EXT	34	USB0_VBUS	57	SYS_CLKIN	80	PA_01
12	SYS_CLKOUT	35	USB0_DP	58	PA_13	81	VDD_INT
13	PC_01	36	VDD_USB	59	PA_12	82	VDD_EXT
14	VDD_INT	37	USB0_DM	60	PA_11	83	JTG_TDO_SWO
15	$\overline{\text{SYS\_RESOUT}}$	38	USB0_VBC	61	VDD_INT	84	JTG_TMS_SWDIO
16	PC_00	39	PB_09	62	VDD_EXT	85	JTG_TCK_SWCLK
17	VDD_EXT	40	PB_08	63	PA_10	86	JTG_TDI
18	TWI0_SDA	41	VDD_EXT	64	PA_09	87	$\overline{\text{JTG\_TRST}}$
19	TWI0_SCL	42	PB_07	65	$\overline{\text{SYS\_FAULT}}$	88	PA_00
20	RTC0_XTAL	43	PB_06	66	SYS_BMODE0	89*	GND
21	RTC0_CLKIN	44	PB_05	67	SYS_BMODE1		
22	VDD_RTC	45	PB_04	68	$\overline{\text{SYS\_HWRST}}$		
23	PB_15	46	PB_03	69	PA_08		

*Pin no. 89 is the GND supply (see Figure 70) for the processor; this pad must connect to GND.

ORDERING GUIDE

Model[1]	Max. Core Clock	L2 SRAM	Temperature Grade[2]	Package Description	Package Option
ADSP-BF700KCPZ-1	100 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700KCPZ-2	200 MHz	128K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF700BCPZ-2	200 MHz	128K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF701KBCZ-1	100 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701KBCZ-2	200 MHz	128K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF701BBCZ-2	200 MHz	128K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF702KCPZ-3	300 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-3	300 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702KCPZ-4	400 MHz	256K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF702BCPZ-4	400 MHz	256K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF703KBCZ-3	300 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-3	300 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703KBCZ-4	400 MHz	256K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF703BBCZ-4	400 MHz	256K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF704KCPZ-3	300 MHz	512K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-3	300 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704KCPZ-4	400 MHz	512K bytes	0C to +70C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF704BCPZ-4	400 MHz	512K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF705KBCZ-3	300 MHz	512K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-3	300 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705KBCZ-4	400 MHz	512K bytes	0C to +70C	184-Ball CSP_BGA	BC-184-1
ADSP-BF705BBCZ-4	400 MHz	512K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF706KCPZ-3	300 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-3	300 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706KCPZ-4	400 MHz	1024K bytes	0°C to +70°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF706BCPZ-4	400 MHz	1024K bytes	–40°C to +85°C	88-Lead LFCSP_VQ	CP-88-8
ADSP-BF707KBCZ-3	300 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-3	300 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707KBCZ-4	400 MHz	1024K bytes	0°C to +70°C	184-Ball CSP_BGA	BC-184-1
ADSP-BF707BBCZ-4	400 MHz	1024K bytes	–40°C to +85°C	184-Ball CSP_BGA	BC-184-1

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 50 for the junction temperature (T_J) specification which is the only temperature specification.

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