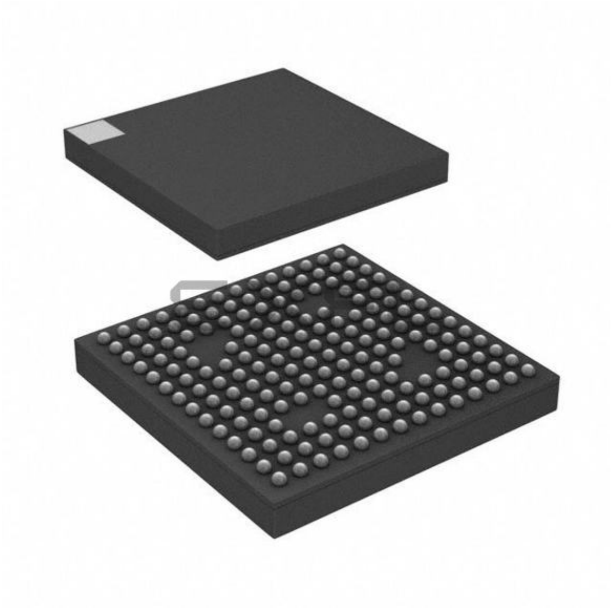

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Blackfin+
Interface	CAN, DSPI, EBI/EMI, I²C, PPI, QSPI, SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	1MB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf707bbcz-3

Static Memory Controller (SMC)

The SMC can be programmed to control up to two blocks of external memories or memory-mapped devices, with very flexible timing parameters. Each block occupies a 8K byte segment regardless of the size of the device used.

Dynamic Memory Controller (DMC)

The DMC includes a controller that supports JESD79-2E compatible double-data-rate (DDR2) SDRAM and JESD209A low-power DDR (LPDDR) SDRAM devices. The DMC PHY features on-die termination on all data and data strobe pins that can be used during reads.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses in a region of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processor has several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE input pins dedicated for this purpose. There are two categories of boot modes. In master boot mode, the processor actively loads data from serial memories. In slave boot modes, the processor receives data from external host devices.

The boot modes are shown in Table 2. These modes are implemented by the SYS_BMODE bits of the reset configuration register and are sampled during power-on resets and software-initiated resets.

Table 2. Boot Modes

SYS_BMODE Setting	Boot Mode
00	No Boot/Idle
01	SPI2 Master
10	SPI2 Slave
11	UART0 Slave

SECURITY FEATURES

The ADSP-BF70x processor supports standards-based hardware-accelerated encryption, decryption, authentication, and true random number generation.

The following hardware-accelerated cryptographic ciphers are supported:

- AES in ECB, CBC, ICM, and CTR modes with 128-, 192-, and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key

The following hardware-accelerated hash functions are supported:

- SHA-1
- SHA-2 with 224-bit and 256-bit digest
- HMAC transforms for SHA-1 and SHA-2

Public key accelerator is available to offload computation-intensive public key cryptography operations.

Both a hardware-based nondeterministic random number generator and pseudo-random number generator are available. The TRNG also provides HW post-processing to meet NIST requirements of FIPS 140-2, while the PRNG is ANSI X9.31 compliant.

Secure boot is also available with 224-bit elliptic curve digital signatures ensuring integrity and authenticity of the boot stream. Optionally, confidentiality is also ensured through AES-128 encryption.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

Secure debug is also employed to allow only trusted users to access the system with debug tools.

PROCESSOR SAFETY FEATURES

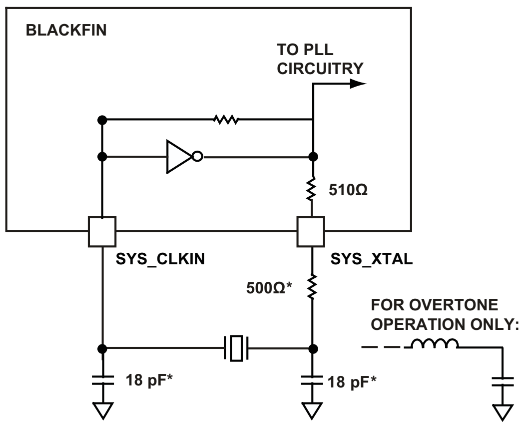
The ADSP-BF70x processor has been designed for functional safety applications. While the level of safety is mainly dominated by the system concept, the following primitives are provided by the devices to build a robust safety concept.

Multi-Parity-Bit-Protected L1 Memories

In the processor's L1 memory space, whether SRAM or cache, each word is protected by multiple parity bits to detect the single event upsets that occur in all RAMs. This applies both to L1 instruction and data memory spaces.

ECC-Protected L2 Memories

Error correcting codes (ECC) are used to correct single event upsets. The L2 memory is protected with a single error correct-double error detect (SEC-DED) code. By default ECC is enabled, but it can be disabled on a per-bank basis. Single-bit errors are transparently corrected. Dual-bit errors can issue a level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over the required temperature range.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18pF SHOULD BE TREATED AS A MAXIMUM.

Figure 4. External Crystal Connection

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) *Using Third Overtone Crystals with the ADSP-218x DSP* (www.analog.com/ee-168).

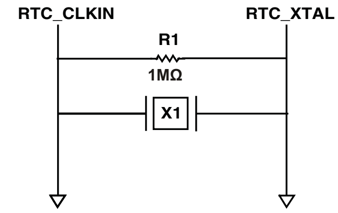
The same recommendations may be used for the USB crystal oscillator.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. Connect RTC pins RTC_CLKIN and RTC_XTAL with external components as shown in Figure 5.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms. The first alarm is for a time of day. The second alarm is for a specific day and time of that day.



NOTE: CRYSTAL LOAD CAPACITORS ARE NOT NECESSARY IN MOST CASES.

Figure 5. External Components for RTC

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

Clock Generation

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SYSCLK, SCLK0, and SCLK1), the LPDDR or DDR2 clock (DCLK), and the output clock (OCLK).

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ can be applied after all voltage supplies are within specifications, and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example, PLL unlock) may trigger a reset by hardware. The clocks shown in Table 3 can be output on the SYS_CLKOUT pin.

Table 3. Clock Dividers

Clock Source	Divider (if Available on SYS_CLKOUT)
CCLK (Core Clock)	By 16
SYSCLK (System Clock)	By 8
SCLK0 (System Clock, All Peripherals not Covered by SCLK1)	Not available on SYS_CLKOUT
SCLK1 (System Clock for Crypto Engines and MDMA)	By 8
DCLK (LPDDR/DDR2 Clock)	By 8
OCLK (Output Clock)	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 4, the processor supports multiple power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 4. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
OTP Memory	V_{DD_OTP}
HADC	V_{DD_HADC}
RTC	V_{DD_RTC}
All Other I/O (Includes SYS, JTAG, and Ports Pins)	V_{DD_EXT}

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

See Table 5 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core and to all synchronous peripherals. Asynchronous peripherals may still be running but cannot access internal resources or external memory.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	f_{CCLK}	f_{SYSCLK}, f_{DCLK}, f_{SCLK0}, f_{SCLK1}	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core and to all of the peripherals. This setting signals the external voltage regulator supplying the VDD_INT pins to shut off using the SYS_EXTWAKE signal, which provides the lowest static power dissipation.

Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a nonvolatile storage device (or self-refreshed DRAM) prior to removing power if the processor state is to be preserved.

Because the V_{DD_EXT} pins can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

Reset Control Unit

Reset is the initial state of the whole processor or the core and is the result of a hardware- or software-triggered event. In this state, all control registers are set to their default values and functional units are idle. Exiting a full system reset starts with the core being ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions puts the system into an undefined state or causes resources to stall. This is particularly important when the core is reset (programs must ensure that there is no pending system activity involving the core when it is being reset).

From a system perspective, reset is defined by both the reset target and the reset source described as follows in the following list.

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

GPIO MULTIPLEXING FOR 184-BALL CSP_BGA

Table 8 through Table 10 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 184-ball CSP_BGA package.

Table 8. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	SPI1_CLK		TRACE0_D07	SMC0_ABE0	
PA_01	SPI1_MISO		TRACE0_D06	SMC0_ABE1	
PA_02	SPI1_MOSI		TRACE0_D05	SMC0_AMS1	
PA_03	SPI1_SEL2	SPI1_RDY		SMC0_ARDY	
PA_04	SPI1_SEL1	TM0_TMR7	SPI2_RDY	SMC0_A08	SPI1_SS
PA_05	TM0_TMR0	SPI0_SEL1		SMC0_A07	SPI0_SS
PA_06	TM0_TMR1	SPI0_SEL2	SPI0_RDY	SMC0_A06	
PA_07	TM0_TMR2	SPT1_BTDV	SPT1_ATDV	SMC0_A05	CNT0_DG
PA_08	PPI0_D11	MSI0_CD	SPT1_ACLK	SMC0_A01	
PA_09	PPI0_D10	TM0_TMR4	SPT1_AFS	SMC0_A02	
PA_10	PPI0_D09	TM0_TMR5	SPT1_AD0	SMC0_A03	
PA_11	PPI0_D08	TM0_TMR6	SPT1_AD1	SMC0_A04	
PA_12	PPI0_FS1	CAN1_RX	SPT0_AFS	SMC0_AOE	TM0_ACI6/SYS_WAKE4
PA_13	PPI0_FS2	CAN1_TX	SPT0_ACLK	SMC0_ARE	CNT0_ZM
PA_14	PPI0_CLK	SPI1_SEL4	SPT0_AD0	SMC0_AWE	TM0_ACLK5
PA_15	PPI0_FS3	SPT0_ATDV	SPT0_BTDV	SMC0_AMS0	CNT0_UD

Table 9. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PPI0_D07	SPT1_BCLK	SPI0_CLK	SMC0_D07	TM0_ACLK3
PB_01	PPI0_D06	SPT1_BFS	SPI0_MISO	SMC0_D06	TM0_ACI1
PB_02	PPI0_D05	SPT1_BD0	SPI0_MOSI	SMC0_D05	
PB_03	PPI0_D04	SPT1_BD1	SPI0_D2	SMC0_D04	
PB_04	PPI0_D03	SPT0_BCLK	SPI0_SEL4	SMC0_D03	TM0_ACLK6
PB_05	PPI0_D02	SPT0_BD0	SPI0_SEL5	SMC0_D02	
PB_06	PPI0_D01	SPT0_BFS	SPI0_SEL6	SMC0_D01	TM0_CLK
PB_07	PPI0_D00	SPT0_BD1	SPI0_D3	SMC0_D00	SYS_WAKE0
PB_08	UART0_TX	PPI0_D16	SPI2_SEL2	SMC0_D08	SYS_WAKE1
PB_09	UART0_RX	PPI0_D17	SPI2_SEL3	SMC0_D09	TM0_ACI3
PB_10	SPI2_CLK		TRACE0_CLK	SMC0_D10	TM0_ACLK4
PB_11	SPI2_MISO		TRACE0_D04	SMC0_D11	
PB_12	SPI2_MOSI		TRACE0_D03	SMC0_D12	SYS_WAKE2
PB_13	SPI2_D2	UART1_RTS	TRACE0_D02	SMC0_D13	
PB_14	SPI2_D3	UART1_CTS	TRACE0_D01	SMC0_D14	
PB_15	SPI2_SEL1		TRACE0_D00	SMC0_D15	SPI2_SS

ADSP-BF70x DESIGNER QUICK REFERENCE

Table 15 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Pin Type: The Type column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (none), I/O (input/output), a (analog), s (supply), and g (ground).
- Driver Type: The Driver Type column in the table identifies the driver type used by the pin. The driver types are defined in the output drive currents section of this data sheet.
- Internal Termination: The Int Term column in the table specifies the termination present when the processor is not in the reset or hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Termination: The Reset Term column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Drive: The Reset Drive column in the table specifies the active drive on the signal when the processor is in the reset state.
- Hibernate Termination: The Hiber Term column in the table specifies the termination present when the processor is in the hibernate state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Hibernate Drive: The Hiber Drive column in the table specifies the active drive on the signal when the processor is in the hibernate state.
- Power Domain: The Power Domain column in the table specifies the power supply domain in which the signal resides.
- Description and Notes: The Description and Notes column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

If an external pull-up or pull-down resistor is required for any signal, 100 kΩ is the maximum value that can be used unless otherwise noted.

Note that for Port A, Port B, and Port C (PA_00 to PC_14), when $\overline{\text{SYS\_HWRST}}$ is low, these pads are three-state. After $\overline{\text{SYS\_HWRST}}$ is released, but before code execution begins, these pins are internally pulled up. Subsequently, the state depends on the input enable and output enable which are controlled by software.

Software control of internal pull-ups works according to the following settings in the PADS_PCFG0 register. When PADS_PCFG0 = 0: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled when both the input enable and output enable of a particular pin are deasserted. When PADS_PCFG0 = 1: For PA_15:PA_00, PB_15:PB_00, and PC_14:PC_00, the internal pull-up is enabled as long as the output enable of a particular pin is deasserted.

There are some exceptions to this scheme:

- Internal pull-ups are always disabled if MSI mode is selected for that signal.
- The following signals enabled the internal pull-down when the output enable is de-asserted: $\overline{\text{SMC0\_AMS[1:0]}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, $\overline{\text{SMC0\_AOE}}$, SMC0_ARDY, $\overline{\text{SPI0\_SEL[6:1]}}$, $\overline{\text{SPI1\_SEL[4:1]}}$, and $\overline{\text{SPI2\_SEL[3:1]}}$.

Table 15. ADSP-BF70x Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 0 Notes: No notes.
DMC0_A01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 1 Notes: No notes.
DMC0_A02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 2 Notes: No notes.
DMC0_A03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 3 Notes: No notes.
DMC0_A04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 4 Notes: No notes.
DMC0_A05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 5 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
DMC0_A06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 6 Notes: No notes.
DMC0_A07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 7 Notes: No notes.
DMC0_A08	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 8 Notes: No notes.
DMC0_A09	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 9 Notes: No notes.
DMC0_A10	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 10 Notes: No notes.
DMC0_A11	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 11 Notes: No notes.
DMC0_A12	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 12 Notes: No notes.
DMC0_A13	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Address 13 Notes: No notes.
DMC0_BA0	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 0 Notes: No notes.
DMC0_BA1	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 1 Notes: No notes.
DMC0_BA2	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Bank Address Input 2 Notes: For LPDDR, leave unconnected.
DMC0_CAS	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes.
DMC0_CK	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes.
DMC0_CK	I/O	C	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock (complement) Notes: No notes.
DMC0_CKE	I/O	B	none	none	L	none	L	VDD_DMC	Desc: DMC0 Clock enable Notes: No notes.
DMC0_CS0	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Chip Select 0 Notes: No notes.
DMC0_DQ00	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 0 Notes: No notes.
DMC0_DQ01	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 1 Notes: No notes.
DMC0_DQ02	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 2 Notes: No notes.
DMC0_DQ03	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 3 Notes: No notes.
DMC0_DQ04	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 4 Notes: No notes.
DMC0_DQ05	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 5 Notes: No notes.
DMC0_DQ06	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 6 Notes: No notes.
DMC0_DQ07	I/O	B	none	none	none	none	none	VDD_DMC	Desc: DMC0 Data 7 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PA_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 1 (HSYNC) | CAN1 Receive | SPORT0 Channel A Frame Sync |SMC0 Output Enable |SYS Power Saving Mode Wakeup 4 | TM0 Alternate Capture Input 6 Notes: If hibernate mode is used one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PA_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 2 (VSYNC) | CAN1 Transmit | SPORT0 Channel A Clock | SMC0 Read Enable | CNT0 Count Zero Marker Notes: No notes.
PA_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Clock | SPI1 Slave Select Output 4 | SPORT0 Channel A Data 0 | SMC0 Write Enable | TM0 Alternate Clock 5 Notes: SPI slave select outputs require a pull-up when used.
PA_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Frame Sync 3 (FIELD) | SPT0 Channel A Transmit Data Valid | SPT0 Channel B Transmit Data Valid | SMC0 Memory Select 0 | CNT0 Count Up and Direction Notes: May require a pull-up if used as an SMC memory select. Check the data sheet requirements of the IC it connects to.
PB_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 7 | SPT1 Channel B Clock | SPI0 Clock | SMC0 Data 7 | TM0 Alternate Clock 3 Notes: SPI clock requires a pull-down when controlling most SPI flash devices.
PB_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 6 | SPT1 Channel B Frame Sync | SPI0 Master In, Slave Out | SMC0 Data 6 | TM0 Alternate Capture Input 1 Notes: Pull-up required for SPI_MISO if SPI master boot is used.
PB_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 5 | SPT1 Channel B Data 0 | SPI0 Master Out, Slave In | SMC0 Data 5 Notes: No notes.
PB_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: PPI0 Data 4 | SPT1 Channel B Data 1 | SPI0 Data 2 | SMC0 Data 4 Notes: No notes.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PB_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Master Out, Slave In | TRACE0 Trace Data 3 | SMC0 Data 12 | SYS Power Saving Mode Wakeup 2 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PB_13	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 2 | UART1 Request to Send | TRACE0 Trace Data 2 | SMC0 Data 13 Notes: No notes.
PB_14	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Data 3 | UART1 Clear to Send | TRACE0 Trace Data 1 | SMC0 Data 14 Notes: No notes.
PB_15	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPI2 Slave Select Output 1 | TRACE0 Trace Data 0 | SMC0 Data 15 | SPI2 Slave Select Input Notes: SPI slave select outputs require a pull-up when used.
PC_00	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Transmit | SPT0 Channel A Data 1 | PPI0 Data 15 Notes: No notes.
PC_01	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART1 Receive | SPT0 Channel B Data 1 | PPI0 Data 14 | SMC0 Address 9 | TM0 Alternate Capture Input 4 Notes: No notes.
PC_02	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Request to Send | CAN0 Receive | PPI0 Data 13 | SMC0 Address 10 | SYS Power Saving Mode Wakeup 3 | TM0 Alternate Capture Input 5 Notes: If hibernate mode is used, one of the following must be true during hibernate. Either this pin must be actively driven by another IC, or it must have a pull-up or pull-down.
PC_03	I/O	A	none	none	none	none	none	VDD_EXT	Desc: UART0 Clear to Send | CAN0 Transmit | PPI0 Data 12 | SMC0 Address 11 | TM0 Alternate Capture Input 0 Notes: No notes.
PC_04	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Clock | SPI0 Clock | MSI0 Data 1 | SMC0 Address 12 | TM0 Alternate Clock 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
PC_05	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Frame Sync | TM0 Timer 3 | MSI0 Command Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_06	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Data 0 | SPI0 Master In, Slave Out | MSI0 Data 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_07	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel B Frame Sync | SPI0 Master Out, Slave In | MSI0 Data 2 | TM0 Alternate Capture Input 2 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_08	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Data 0 | SPI0 Data 2 | MSI0 Data 0 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.
PC_09	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT0 Channel A Clock | SPI0 Data 3 | MSI0 Clock | TM0 Alternate Clock 2 Notes: No notes.
PC_10	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Clock | MSI0 Data 4 | SPI1 Slave Select Output 3 | TM0 Alternate Clock 1 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_11	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Frame Sync | MSI0 Data 5 | SPI0 Slave Select Output 3 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details. SPI slave select outputs require a pull-up when used.
PC_12	I/O	A	none	none	none	none	none	VDD_EXT	Desc: SPT1 Channel B Data 0 | MSI0 Data 6 Notes: An external pull-up may be required for MSI modes, see the MSI chapter in the hardware reference for details.

Table 15. ADSP-BF70x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Hiber Term	Hiber Drive	Power Domain	Description and Notes
TWI0_SCL	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	D	none	none	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Open drain, requires external pull up. Consult version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
USB0_CLKIN	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Clock/Crystal Input Notes: If USB is not used, connect to ground. Active during reset
USB0_DM	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data – Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_DP	I/O	F	none	none	none	none	none	VDD_USB	Desc: USB0 Data + Notes: Pull low if not using USB. For complete documentation of hibernate behavior when USB is used, see the USB chapter in the HRM.
USB0_ID	I/O	na	none	none	none	none	none	VDD_USB	Desc: USB0 OTG ID Notes: If USB is not used connect to ground. When USB is being used, the internal pull-up that is present during hibernate is programmable. See the USB chapter in the HRM. Active during reset.
USB0_VBC	I/O	E	none	none	none	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: If USB is not, used pull low.
USB0_VBUS	I/O	G	none	none	none	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: If USB is not used, connect to ground.
USB0_XTAL	a	na	none	none	none	none	none	VDD_USB	Desc: USB0 Crystal Notes: No notes.
VDD_DMC	s	na	none	none	none	none	none	na	Desc: VDD for DMC Notes: If the DMC is not used, connect to VDD_INT.
VDD_EXT	s	na	none	none	none	none	none	na	Desc: External VDD Notes: Must be powered.
VDD_HADC	s	na	none	none	none	none	none	na	Desc: VDD for HADC Notes: If HADC is not used, connect to ground.
VDD_INT	s	na	none	none	none	none	none	na	Desc: Internal VDD Notes: Must be powered.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OH} = –1.0 mA	0.8 × V_{DD_EXT}			V
V_{OH}[1]	High Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OH} = –2.0 mA	0.9 × V_{DD_EXT}			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 34 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –7.1 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 40 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –5.8 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 50 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –4.1 mA	V_{DD_DMC} – 0.320			V
V_{OH_DDR2}[2]	High Level Output Voltage, DDR2, Programmed Impedance = 60 Ω	V_{DD_DMC} = 1.70 V, I_{OH} = –3.4 mA	V_{DD_DMC} – 0.320			V
V_{OH_LPDDR}[2]	High Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OH} = –2.0 mA	V_{DD_DMC} – 0.320			V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 1.7 V, I_{OL} = 1.0 mA			0.400	V
V_{OL}[3]	Low Level Output Voltage	V_{DD_EXT} = 3.13 V, I_{OL} = 2.0 mA			0.400	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 34 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 7.1 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 40 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 5.8 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 50 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 4.1 mA			0.320	V
V_{OL_DDR2}[2]	Low Level Output Voltage, DDR2, Programmed Impedance = 60 Ω	V_{DD_DMC} = 1.70 V, I_{OL} = 3.4 mA			0.320	V
V_{OL_LPDDR}[2]	Low Level Output Voltage, LPDDR	V_{DD_DMC} = 1.70 V, I_{OL} = 2.0 mA			0.320	V
I_{IH}[4]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
$I_{IH\_DMC0\_VREF}$[5]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			1	µA
I_{IH_PD}[6]	High Level Input Current with Pull-down Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			100	µA
R_{PD}[6]	Internal Pull-down Resistance	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V	57		130	kΩ
I_{IL}[7]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
$I_{IL\_DMC0\_VREF}$[5]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			1	µA
I_{IL_PU}[8]	Low Level Input Current with Pull-up Resistor	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			100	µA
R_{PU}[8]	Internal Pull-up Resistance	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V	53		129	kΩ
I_{IH_USB0}[9]	High Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{IL_USB0}[9]	Low Level Input Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{OZH}[10]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			10	µA
I_{OZH}[11]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 1.9 V			10	µA
I_{OZL}[12]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 0 V			10	µA
I_{OZH_PD}[13]	Three-State Leakage Current	V_{DD_EXT} = 3.47 V, V_{DD_DMC} = 1.9 V, V_{DD_USB} = 3.47 V, V_{IN} = 3.47 V			100	µA

SMC Write Cycle Timing With Reference to SYS_CLKOUT

The following SMC specifications with respect to SYS_CLKOUT are given to accommodate the connection of the SMC to programmable logic devices. These specifications assume that SYS_CLKOUT is outputting a buffered version of SCLK0 by setting CGU_CLKOUTSEL.CLKOUTSEL = 0x3. However, SCLK0 must not run faster than the maximum f_{OCLK} specification. For this example WST = 0x2, WAT = 0x2, and WHT = 0x1.

Table 36. SMC Write Cycle Timing With Reference to SYS_CLKOUT (BxMODE = b#00)

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
t_{SARDY}	SMC0_ARDY Setup Before SYS_CLKOUT	14.4		ns
t_{HARDY}	SMC0_ARDY Hold After SYS_CLKOUT	0.7		ns
Switching Characteristics				
t_{DDAT}	SMC0_Dx Disable After SYS_CLKOUT		7	ns
t_{ENDAT}	SMC0_Dx Enable After SYS_CLKOUT	–2.5		ns
t_{DO}	Output Delay After SYS_CLKOUT[1]		7	ns
t_{HO}	Output Hold After SYS_CLKOUT [1]	–2.5		ns

[1] Output pins/balls include $\overline{\text{SMC0\_AMSx}}$, $\overline{\text{SMC0\_ABEx}}$, SMC0_Ax, SMC0_Dx, $\overline{\text{SMC0\_AOE}}$, and $\overline{\text{SMC0\_AWE}}$.

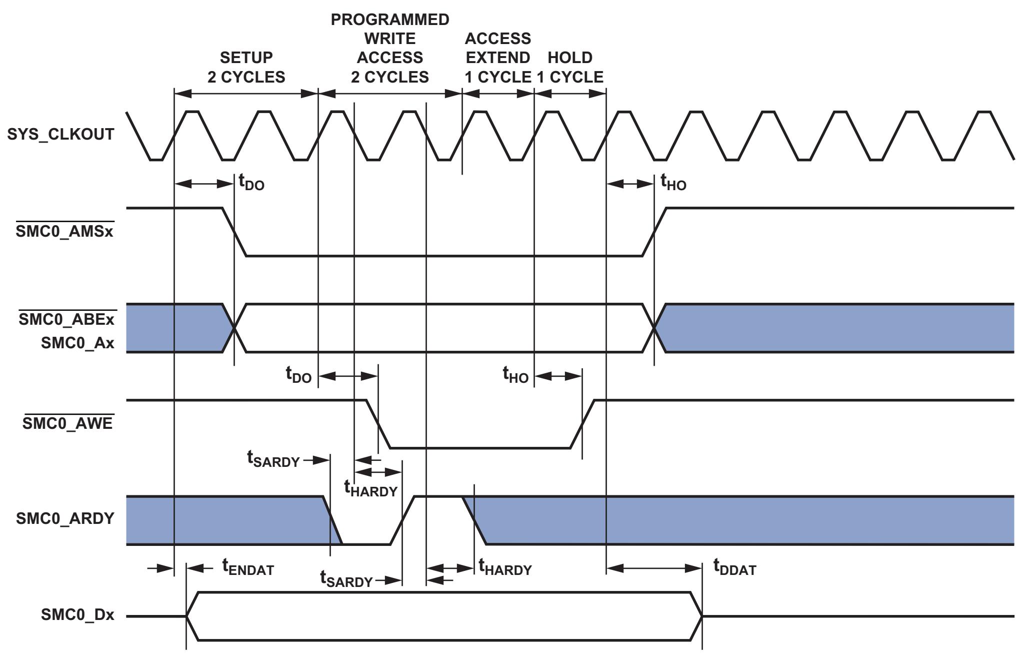


Figure 15. SMC Write Cycle Timing With Reference to SYS_CLKOUT Timing

Debug Interface (JTAG Emulation Port) Timing

Table 48 and Figure 26 provide I/O timing, related to the debug interface (JTAG emulator port).

Table 48. JTAG Port Timing

Parameter		V_{DD_EXT} 1.8 V Nominal Min	Max	V_{DD_EXT} 3.3 V Nominal Min	Max	Unit
Timing Requirements						
t_{TCK}	JTG_TCK Period	20		20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	5		4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	4		4		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK Cycles)[2]	4		4		t_{TCK}
Switching Characteristics						
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		16.5		14.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		18		16.5	ns
t_{DTMS}	TMS Delay After TCK High in SWD Mode	3.5	16.5	3.5	14.5	ns

[1] System inputs = DMC0_DQxx, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, PA_xx, PB_xx, PC_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA, and SYS_EXTWAKE.

[2] 50 MHz maximum.

[3] System outputs = DMC0_Axx, DMC0_BAx, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, $\overline{\text{DMC0\_CK}}$, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQxx, DMC0_LDM, DMC0_LDQS, $\overline{\text{DMC0\_LDQS}}$, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_UDQS}}$, $\overline{\text{DMC0\_WE}}$, PA_xx, PB_xx, PC_xx, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$, and $\overline{\text{SYS\_NMI}}$.

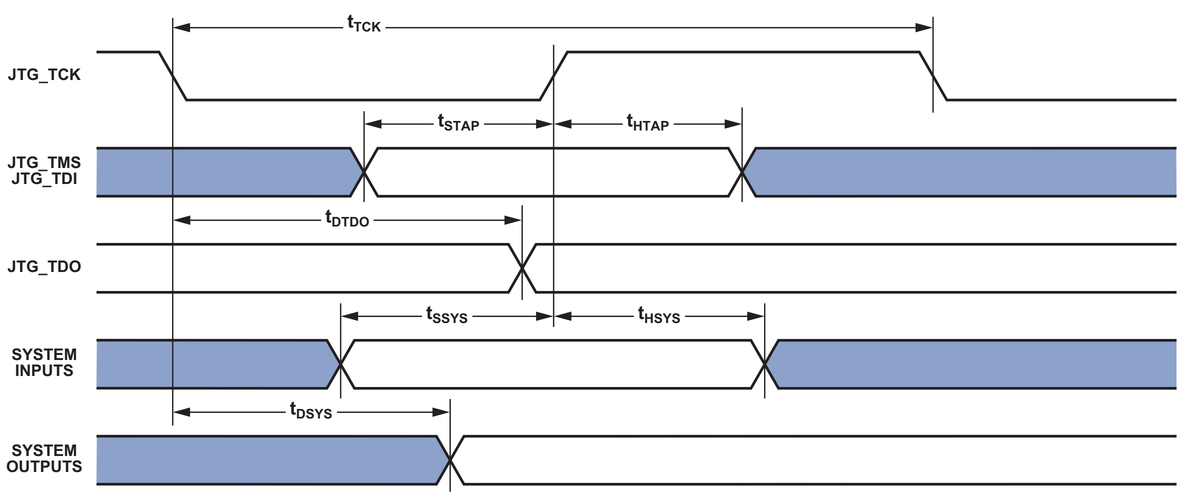


Figure 26. JTAG Port Timing

Serial Peripheral Interface (SPI) Port—Master Timing

Table 54 and Figure 31 describe serial peripheral interface (SPI) port master operations.

When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in MHz is set by the following equation where BAUD is a field in the SPI_CLK register that can be set from 0 to 65,535:

$$f_{SPICLKPROG} = \frac{f_{SCLK0}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

Note that:

- In dual mode data transmit, the SPI_MISO signal is also an output.
- In quad mode data transmit, the SPI_MISO, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive, the SPI_MOSI signal is also an input.
- In quad mode data receive, the SPI_MOSI, SPI_D2, and SPI_D3 signals are also inputs.
- To add additional frame delays, see the documentation for the SPI_DLY register in the hardware reference manual.

Table 54. Serial Peripheral Interface (SPI) Port—Master Timing

		V_{DD_EXT} 1.8 V Nominal		V_{DD_EXT} 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	6.5		5.5		ns
t_{HSPIDM}	SPI_CLK Sampling Edge to Data Input Invalid	1		1		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{\text{SPI\_SEL}}$ low to First SPI_CLK Edge	$0.5 \times t_{SCLK0} - 2.5$		$0.5 \times t_{SCLK0} - 1.5$		ns
t_{SPICHM}	SPI_CLK High Period[1]	$0.5 \times t_{SPICLKPROG} - 1.5$		$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLM}	SPI_CLK Low Period[1]	$0.5 \times t_{SPICLKPROG} - 1.5$		$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLK}	SPI_CLK Period[1]	$t_{SPICLKPROG} - 1.5$		$t_{SPICLKPROG} - 1.5$		ns
t_{HDSM}	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High	$(0.5 \times t_{SCLK0}) - 2.5$		$(0.5 \times t_{SCLK0}) - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay[2]	$(STOP \times t_{SPICLK}) - 1.5$		$(STOP \times t_{SPICLK}) - 1.5$		ns
$t_{DDSPIDM}$	SPI_CLK Edge to Data Out Valid (Data Out Delay)		2.5		2	ns
$t_{HDSPIDM}$	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	–4.5		–3.5		ns

[1] See Table 18 on Page 52 in Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.
[2] STOP value set using the SPI_DLY.STOP bits.

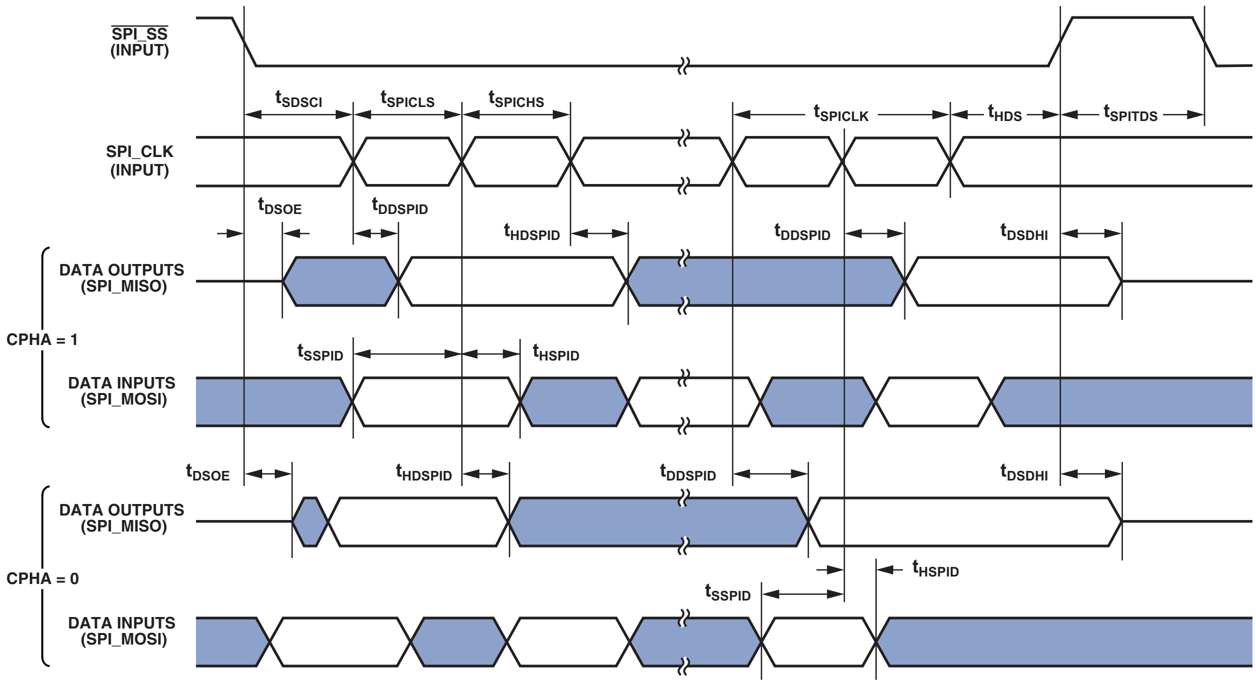


Figure 32. Serial Peripheral Interface (SPI) Port—Slave Timing

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 56. SPI Port—SPI_RDY Slave Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive	$2.5 \times t_{SCLK0} + t_{HDSPID}$	$3.5 \times t_{SCLK0} + t_{DDSPID}$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit	$3.5 \times t_{SCLK0} + t_{HDSPID}$	$4.5 \times t_{SCLK0} + t_{DDSPID}$	ns

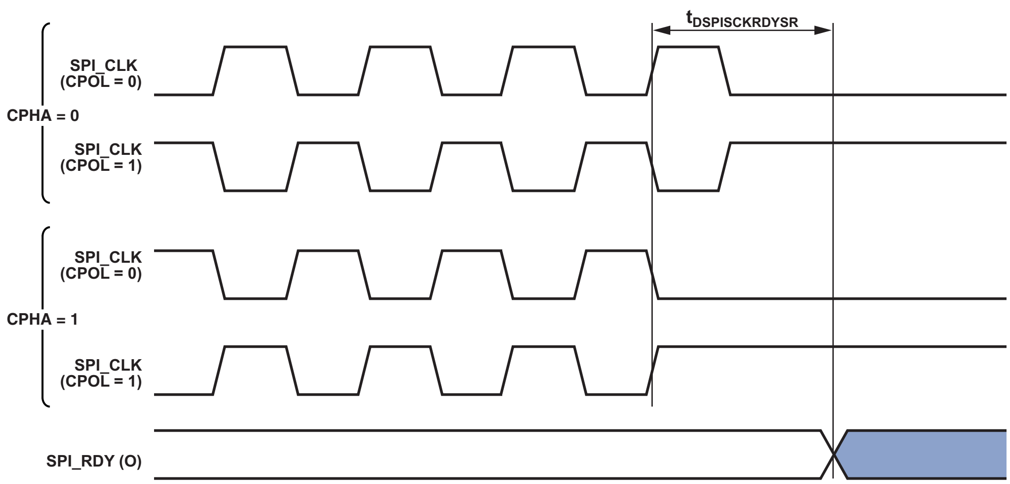


Figure 33. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

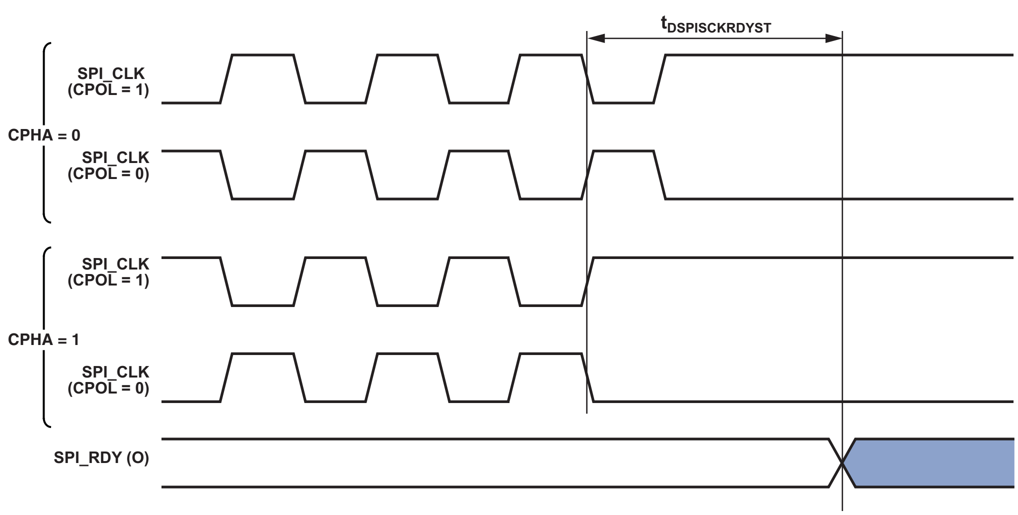


Figure 34. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

Serial Peripheral Interface (SPI) Port—SPI_RDY Timing

SPI_RDY is used to provide flow control. The CPOL and CPHA bits are set in SPI_CTL, while LEADX, LAGX, and STOP are in SPI_DLY.

Table 59. SPI Port—SPI_RDY Timing

Parameter		V_{DD_EXT} 1.8 V/3.3 V Nominal Min	Max	Unit
Timing Requirements				
$t_{SRDYSCKM0}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 0	(2.5 + 1.5 × BAUD[1]) × t_{SCLK0} + 14.5		ns
$t_{SRDYSCKM1}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	(2.5 + BAUD[1]) × t_{SCLK0} + 14.5		ns
Switching Characteristic				
$t_{SRDYSCKM}$	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 0 and BAUD = 0 (STOP, LEADX, LAGX = 0)	3 × t_{SCLK0}	4 × t_{SCLK0} + 17.5	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 0 and BAUD ≥ 1 (STOP, LEADX, LAGX = 0)	(4 + 1.5 × BAUD[1]) × t_{SCLK0}	(5 + 1.5 × BAUD[1]) × t_{SCLK0} + 17.5	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA = 1 (STOP, LEADX, LAGX = 0)	(3 + 0.5 × BAUD[1]) × t_{SCLK0}	(4 + 0.5 × BAUD[1]) × t_{SCLK0} + 17.5	ns

[1] BAUD value set using the SPI_CLK.BAUD bits.

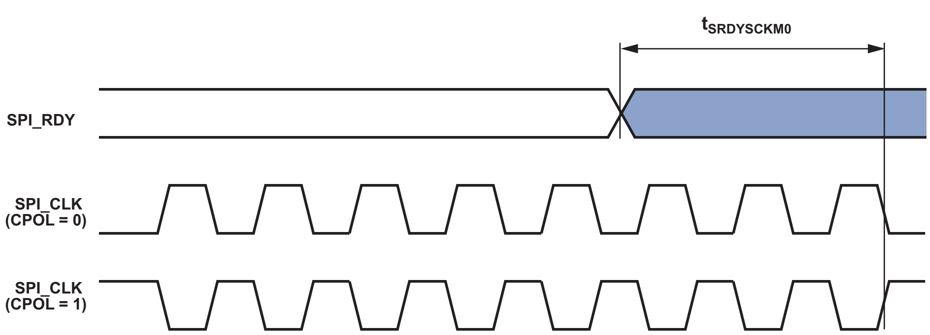


Figure 37. SPI_RDY Setup Before SPI_CLK with CPHA = 0

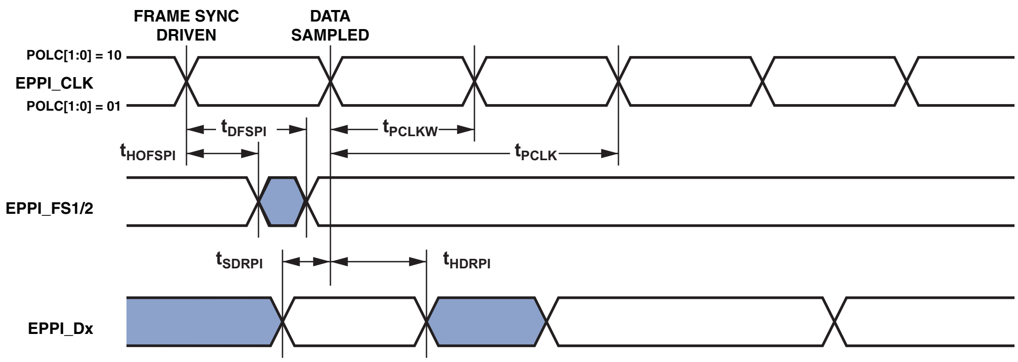


Figure 40. PPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

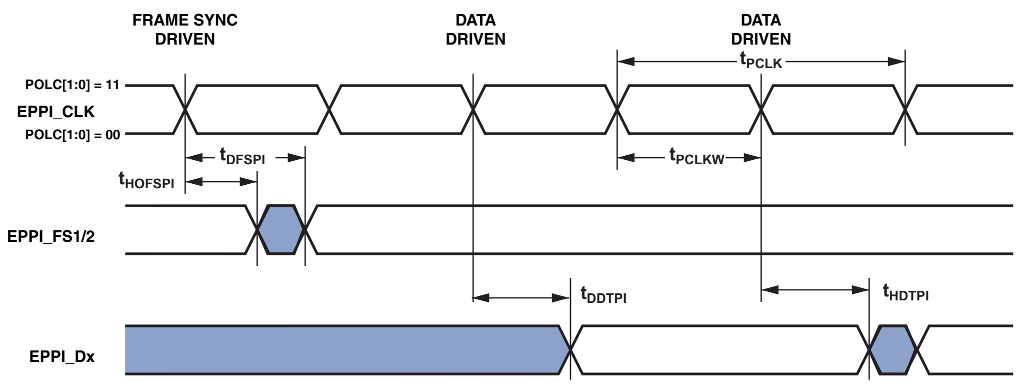


Figure 41. PPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

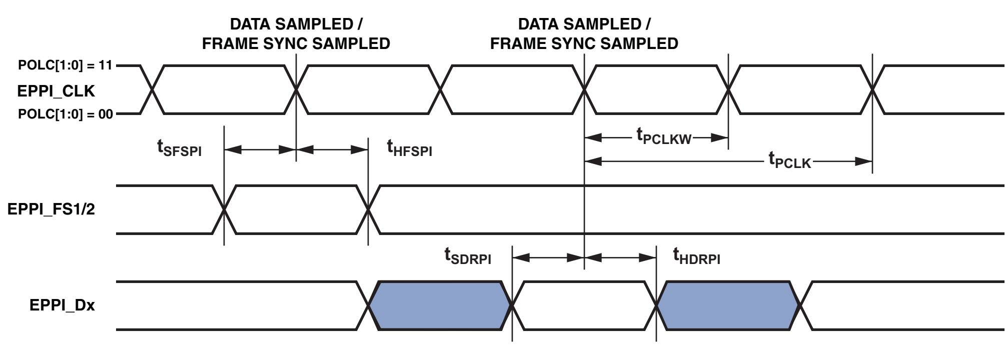


Figure 42. PPI Internal Clock GP Receive Mode with External Frame Sync Timing

Table 67. 184-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A01	GND	D08	VDD_DMC	H03	SYS_CLKOUT	L14	GND
A02	DMC0_A09	D09	VDD_DMC	H04	VDD_INT	M01	PC_00
A03	DMC0_BA0	D12	PA_08	H05	GND	M02	RTC0_CLKIN
A04	DMC0_BA1	D13	DMC0_DQ06	H06	GND	M03	PB_15
A05	DMC0_BA2	D14	DMC0_DQ05	H07	GND	M04	PB_12
A06	DMC0_CAS	E01	DMC0_A06	H08	GND	M05	PC_12
A07	DMC0_RAS	E02	DMC0_A05	H09	GND	M06	USB0_VBUS
A08	DMC0_A13	E03	JTG_TDI	H10	GND	M07	USB0_VBC
A09	PA_03	E05	VDD_INT	H11	VDD_DMC	M08	PB_09
A10	DMC0_CK	E06	VDD_DMC	H12	PA_10	M09	PB_05
A11	DMC0_CK	E07	VDD_DMC	H13	PA_11	M10	PB_04
A12	DMC0_LDQS	E08	VDD_DMC	H14	DMC0_UDQS	M11	PB_01
A13	DMC0_LDQS	E09	VDD_DMC	J01	PC_05	M12	PB_03
A14	GND	E10	DMC0_VREF	J02	PC_06	M13	DMC0_LDM
B01	DMC0_A07	E12	SYS_BMODE0	J03	SYS_RESOUT	M14	SYS_CLKIN
B02	DMC0_A08	E13	DMC0_DQ08	J04	VDD_INT	N01	RTC0_XTAL
B03	DMC0_A11	E14	DMC0_DQ07	J05	VDD_RTC	N02	PB_14
B04	DMC0_A10	F01	DMC0_A01	J06	GND	N03	PB_11
B05	DMC0_A12	F02	DMC0_A02	J07	GND	N04	PC_14
B06	DMC0_WE	F03	PC_09	J08	GND	N05	PC_11
B07	DMC0_CS0	F04	VDD_INT	J09	GND	N06	USB0_ID
B08	DMC0_ODT	F05	VDD_INT	J10	GND_HADC	N07	USB0_DP
B09	DMC0_CKE	F06	GND	J11	VDD_OTP	N08	PB_08
B10	DMC0_DQ00	F07	GND	J12	PA_13	N09	PB_06
B11	DMC0_DQ02	F08	GND	J13	DMC0_DQ13	N10	PB_00
B12	DMC0_DQ01	F09	GND	J14	DMC0_UDQS	N11	HADC0_VIN2
B13	DMC0_DQ04	F10	VDD_DMC	K01	PC_04	N12	HADC0_VIN1
B14	DMC0_DQ03	F11	VDD_DMC	K02	PC_01	N13	PA_15
C01	JTG_TDO_SWO	F12	SYS_FAULT	K03	PC_02	N14	SYS_XTAL
C02	JTG_TMS_SWDIO	F13	DMC0_DQ10	K05	VDD_EXT	P01	GND
C03	JTG_TCK_SWCLK	F14	DMC0_DQ09	K06	VDD_EXT	P02	PB_13
C04	PA_01	G01	DMC0_A03	K07	VDD_EXT	P03	PB_10
C05	SYS_EXTWAKE	G02	PA_00	K08	VDD_EXT	P04	PC_13
C06	PA_02	G03	PC_08	K09	VDD_EXT	P05	USB0_XTAL
C07	SYS_NMI	G04	VDD_INT	K10	VDD_HADC	P06	USB0_CLKIN
C08	GND	G05	GND	K12	PA_12	P07	USB0_DM
C09	PA_04	G06	GND	K13	DMC0_DQ15	P08	PB_07
C10	PA_05	G07	GND	K14	DMC0_DQ14	P09	HADC0_VREFN
C11	PA_06	G08	GND	L01	PC_03	P10	HADC0_VREFP
C12	PA_07	G09	GND	L02	TWI0_SDA	P11	HADC0_VIN3
C13	SYS_HWRST	G10	GND	L03	TWI0_SCL	P12	HADC0_VIN0
C14	SYS_BMODE1	G11	VDD_DMC	L06	VDD_USB	P13	PA_14
D01	DMC0_A00	G12	PA_09	L07	VDD_EXT	P14	GND
D02	DMC0_A04	G13	DMC0_DQ11	L08	VDD_EXT		
D03	JTG_TRST	G14	DMC0_DQ12	L09	VDD_EXT		
D06	VDD_DMC	H01	PC_07	L12	PB_02		
D07	VDD_DMC	H02	PC_10	L13	DMC0_UDM		