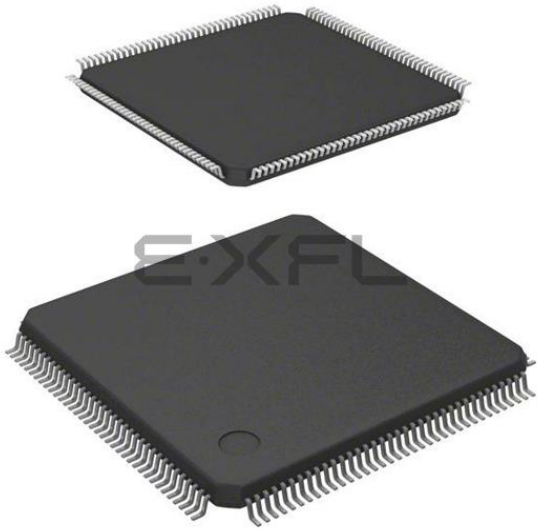


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f272-bag-t-tr

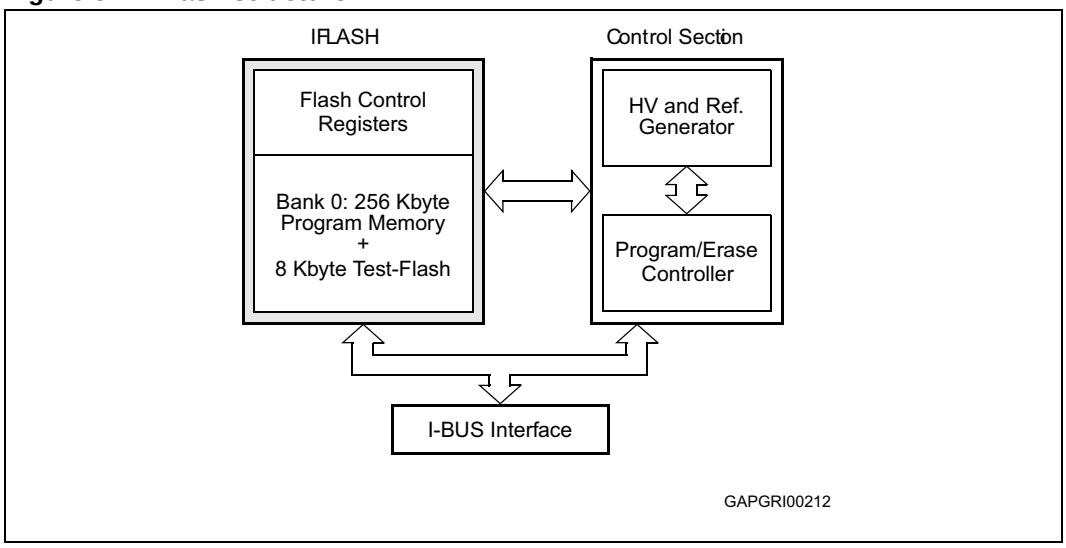
5 Internal Flash memory

5.1 Overview

The on-chip Flash is composed by one matrix module, 256 KBytes wide.

This module is on ST10 Internal bus, so it is called IFLASH

Figure 5. Flash structure



The programming operations of the flash are managed by an embedded Flash Program/Erase Controller (FPEC). The High Voltages needed for Program/Erase operations are internally generated.

The Data bus is 32-bit wide for fetch accesses to IFLASH, while it is 16 bit wide for read accesses to IFLASH. Read/write accesses to IFLASH Control Registers area are 16 bit wide.

5.2 Functional description

5.2.1 Structure

Table 3 shows the Address space reserved to the Flash module.

Table 3. Address space reserved to the Flash module

Description	Addresses	Size
IFLASH sectors	0x00 0000 to 0x04 FFFF	256 Kbyte
Reserved IBUS area	0x05 0000 to 0x07 FFFF	192 Kbyte
Registers and Flash internal reserved area	0x08 0000 to 0x08 FFFF	64 Kbyte

Table 8. Flash control register 0 high (continued)

Bit	Function
SUSP	Suspend This bit must be set to suspend the current Program (Word or Double Word) or Sector Erase operation in order to read data in one of the Sectors of the Bank under modification or to program data in another Bank. The Suspend operation resets the Flash Bank to normal read mode (automatically resetting bit BSY0). When in Program Suspend, the Flash module accepts only the following operations: Read and Program Resume. When in Erase Suspend the module accepts only the following operations: Read, Erase Resume and Program (Word or Double Word; Program operations cannot be suspended during Erase Suspend). To resume a suspended operation, the WMS bit must be set again, together with the selection bit corresponding to the operation to resume (WPG, DWPG, SER). **Note:** It is forbidden to start a new Write operation with bit SUSP already set.
WMS	Write Mode Start This bit must be set to start every write operation in the Flash module. At the end of the write operation or during a Suspend, this bit is automatically reset. To resume a suspended operation, this bit must be set again. It is forbidden to set this bit if bit ERR of FER is high (the operation is not accepted). It is also forbidden to start a new write (program or erase) operation (by setting WMS high) when bit SUSP of FCR0 is high. Resetting this bit by software has no effect.

5.4.3 Flash control register 1 low

The Flash Control Register 1 Low (FCR1L), together with Flash Control Register 1 High (FCR1H), is used to select the Sectors to Erase, or during any write operation to monitor the status of each Sector and Bank.

FCR1L (0x08 0004) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								B0F7	B0F6	B0F5	B0F4	B0F3	B0F2	B0F1	B0F0
								RS	RS	RS	RS	RS	RS	RS	RS

Table 9. Flash control register 1 low

Bit	Function
B0F(7:0)	Bank 0 IFLASH Sector 9:0 Status These bits must be set during a Sector Erase operation to select the sectors to erase in Bank 0. Besides, during any erase operation, these bits are automatically set and give the status of the 8 sectors of Bank 0 (B0F7-B0F0). The meaning of B0Fy bit for Sector y of Bank 0 is given by the next Table 4 Banks (BxS) and Sectors (BxFy) Status bits meaning. These bits are automatically reset at the end of a Write operation if no errors are detected.

5.7 Write operation summary

In general, each write operation is started through a sequence of 3 steps:

1. The first instruction is used to select the desired operation by setting its corresponding selection bit in the Flash Control Register 0.
2. The second step is the definition of the Address and Data for programming or the Sectors or Banks to erase.
3. The last instruction is used to start the write operation, by setting the start bit WMS in the FCR0.

Once selected, but not yet started, one operation can be canceled by resetting the operation selection bit.

A summary of the available Flash Module Write Operations are shown in the following *Table 25*.

Table 25. Flash write operations

Operation	Select bit	Address and data	Start bit
Word Program (32-bit)	WPG	FARL/FARH FDR0L/FDR0H	WMS
Double Word Program (64-bit)	DWPG	FARL/FARH FDR0L/FDR0H FDR1L/FDR1H	WMS
Sector Erase	SER	FCR1L/FCR1H	WMS
Set Protection	SPR	FDR0L/FDR0H	WMS
Program/Erase Suspend	SUSP	None	None

9 Interrupt system

The interrupt response time for internal program execution is from 78ns to 187.5ns at 64 MHz CPU clock.

The ST10F272 architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources (internal or external) to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited to perform the transmission or the reception of blocks of data. The ST10F272 has 8 PEC channels, each of them offers such fast interrupt-driven data transfer capabilities.

An interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit-field is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Fast external interrupts may also have interrupt sources selected from other peripherals; for example the CANx controller receive signals (CANx_RxD) and I^2C serial clock signal can be used to interrupt the system.

Table 29 shows all the available ST10F272 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 29. Interrupt sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00’0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00’0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00’0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00’004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00’0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00’0054h	15h

12 PWM modules

Two pulse width modulation modules are available on ST10F272: standard PWM0 and XBUS PWM1. They can generate up to four PWM output signals each, using edge-aligned or centre-aligned PWM. In addition, the PWM modules can generate PWM burst signals and single shot outputs. The *Table 39* and *Table 40* show the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM modules can generate interrupt requests.

Figure 11. Block diagram of PWM module

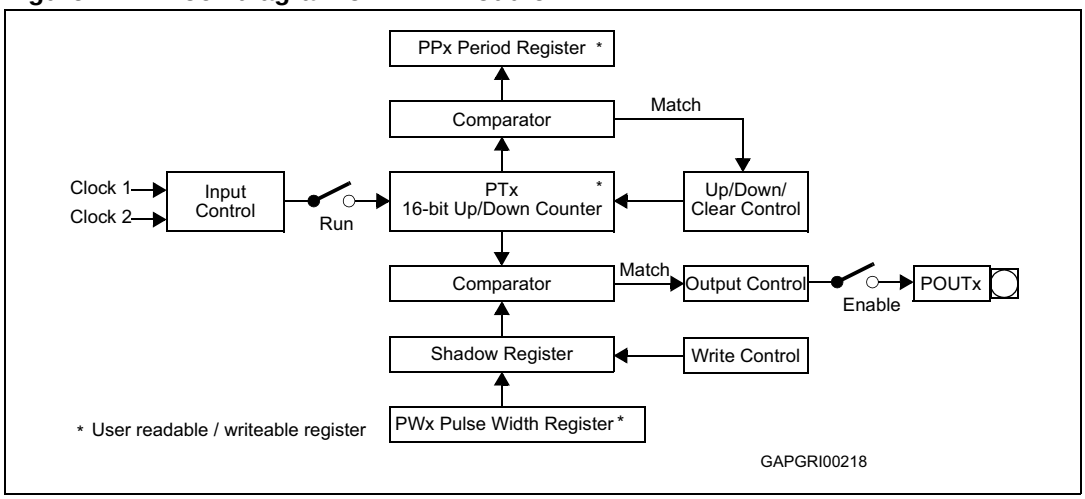


Table 39. PWM unit frequencies and resolutions at 40 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	25ns	156.25 kHz	39.1 kHz	9.77 kHz	2.44Hz	610Hz
CPU Clock/64	1.6µs	2.44 kHz	610Hz	152.6Hz	38.15Hz	9.54Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	25ns	78.12 kHz	19.53 kHz	4.88 kHz	1.22 kHz	305.2Hz
CPU Clock/64	1.6µs	1.22 kHz	305.17Hz	76.29Hz	19.07Hz	4.77Hz

This is done by setting or clearing the direction control bit DPx.y of the pin before enabling the alternate function.

There are port lines, however, where the direction of the port line is switched automatically.

For instance, in the multiplexed external bus modes of PORT0, the direction must be switched several times for an instruction fetch in order to output the addresses and to input the data.

Obviously, this cannot be done through instructions. In these cases, the direction of the port line is switched automatically by hardware if the alternate function of such a pin is enabled.

To determine the appropriate level of the port output latches check how the alternate data output is combined with the respective port latch output.

There is one basic structure for all port lines with only an alternate input function. Port lines with only an alternate output function, however, have different structures due to the way the direction of the pin is switched and depending on whether the pin is accessible by the user software or not in the alternate function mode.

All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

Table 42. ASC asynchronous baud rates by reload value and deviation errors (f_{CPU} = 64 MHz)

S0BRS = '0', f_{CPU} = 64 MHz			S0BRS = '1', f_{CPU} = 64 MHz		
Baud rate (baud)	Deviation error	Reload value (hex)	Baud rate (baud)	Deviation error	Reload value (hex)
2 000 000	0.0% / 0.0%	0000 / 0000	1 333 333	0.0% / 0.0%	0000 / 0000
112 000	+1.5% / -7.0%	0010 / 0011	112 000	+6.3% / -7.0%	000A / 000B
56 000	+1.5% / -3.0%	0022 / 0023	56 000	+6.3% / -0.8%	0016 / 0017
38 400	+1.7% / -1.4%	0033 / 0034	38 400	+3.3% / -1.4%	0021 / 0022
19 200	+0.2% / -1.4%	0067 / 0068	19 200	+0.9% / -1.4%	0044 / 0045
9 600	+0.2% / -0.6%	00CF / 00D0	9 600	+0.9% / -0.2%	0089 / 008A
4 800	+0.2% / -0.2%	019F / 01A0	4 800	+0.4% / -0.2%	0114 / 0115
2 400	+0.2% / 0.0%	0340 / 0341	2 400	+0.1% / -0.2%	022A / 015B
1 200	0.1% / 0.0%	0681 / 0682	1 200	+0.1% / -0.1%	0456 / 0457
600	0.0% / 0.0%	0D04 / 0D05	600	+0.1% / 0.0%	08AD / 08AE
300	0.0% / 0.0%	1A09 / 1A0A	300	0.0% / 0.0%	115B / 115C
245	0.0% / 0.0%	1FE2 / 1FE3	163	0.0% / 0.0%	1FF2 / 1FF3

Note: The deviation errors given in the Table 41 and Table 42 are rounded. To avoid deviation errors use a Baud rate crystal (providing a multiple of the ASC0 sampling frequency).

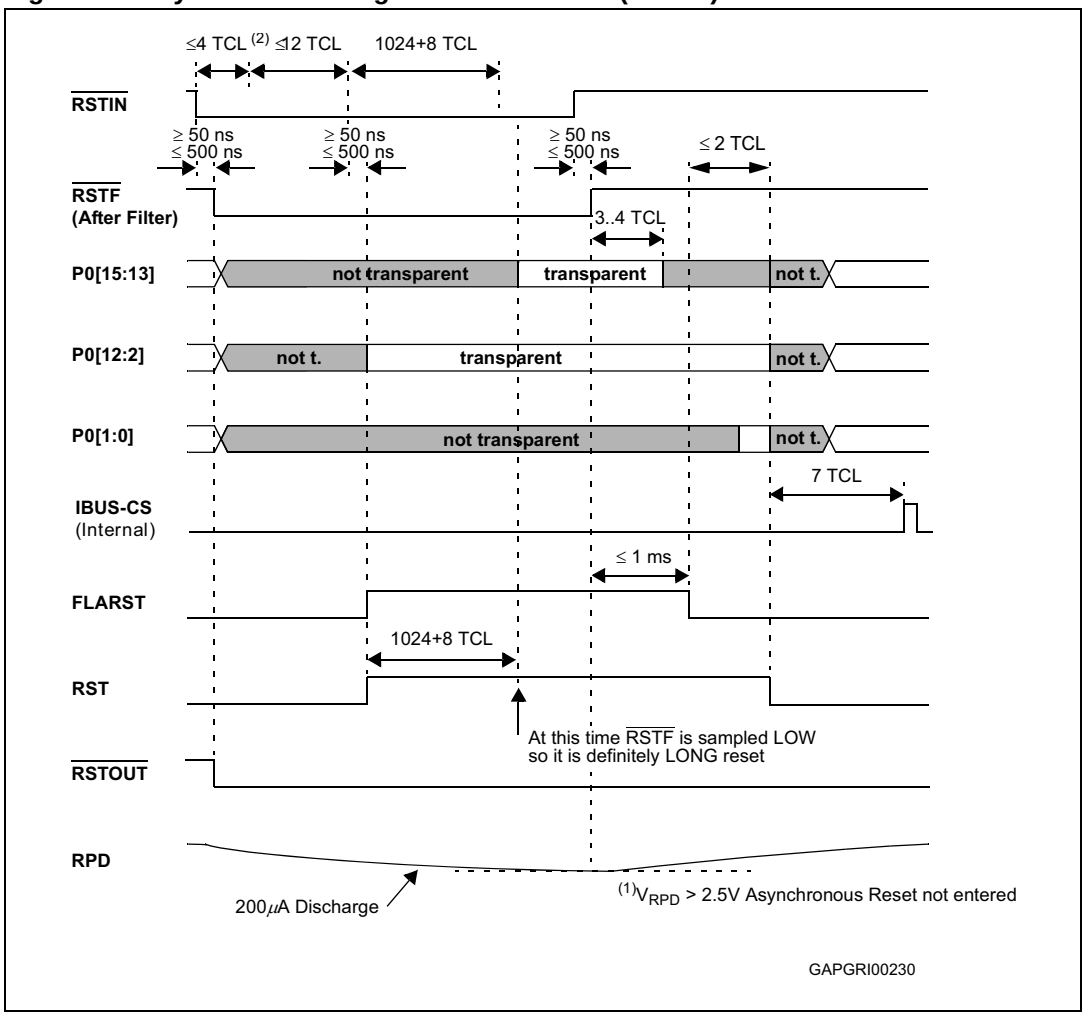
15.3 ASCx in synchronous mode

In synchronous mode, data is transmitted or received synchronously to a shift clock which is generated by the ST10F272. Half-duplex communication up to 8M Baud (at 40 MHz of f_{CPU}) is possible in this mode.

Table 43. ASC synchronous baud rates by reload value and deviation errors (f_{CPU} = 40 MHz)

S0BRS = '0', f_{CPU} = 40 MHz			S0BRS = '1', f_{CPU} = 40 MHz		
Baud rate (baud)	Deviation error	Reload value (hex)	Baud rate (baud)	Deviation error	Reload value (hex)
5 000 000	0.0% / 0.0%	0000 / 0000	3 333 333	0.0% / 0.0%	0000 / 0000
112 000	+1.5% / -0.8%	002B / 002C	112 000	+2.6% / -0.8%	001C / 001D
56 000	+0.3% / -0.8%	0058 / 0059	56 000	+0.9% / -0.8%	003A / 003B
38 400	+0.2% / -0.6%	0081 / 0082	38 400	+0.9% / -0.2%	0055 / 0056
19 200	+0.2% / -0.2%	0103 / 0104	19 200	+0.4% / -0.2%	00AC / 00AD
9 600	+0.2% / 0.0%	0207 / 0208	9 600	+0.1% / -0.2%	015A / 015B
4 800	+0.1% / 0.0%	0410 / 0411	4 800	+0.1% / -0.1%	02B5 / 02B6
2 400	0.0% / 0.0%	0822 / 0823	2 400	+0.1% / 0.0%	056B / 056C
1 200	0.0% / 0.0%	1045 / 1046	1 200	0.0% / 0.0%	0AD8 / 0AD9

Figure 22. Synchronous long hardware RESET ($\overline{EA}$ = 1)



1. If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5V for 5V operation),the asynchronous reset is then immediately entered. Even if RPD returns above the threshold, the reset is defnitively taken as asynchronous.
2. Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the nternal filter (refer to *Section 21.1*).

Figure 30. System reset circuit

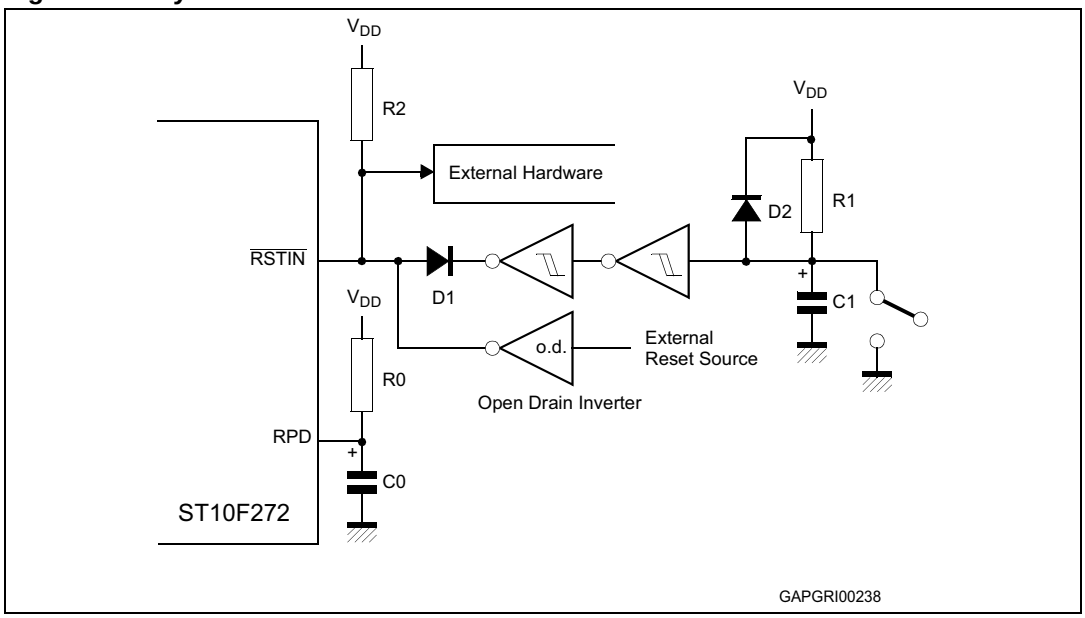
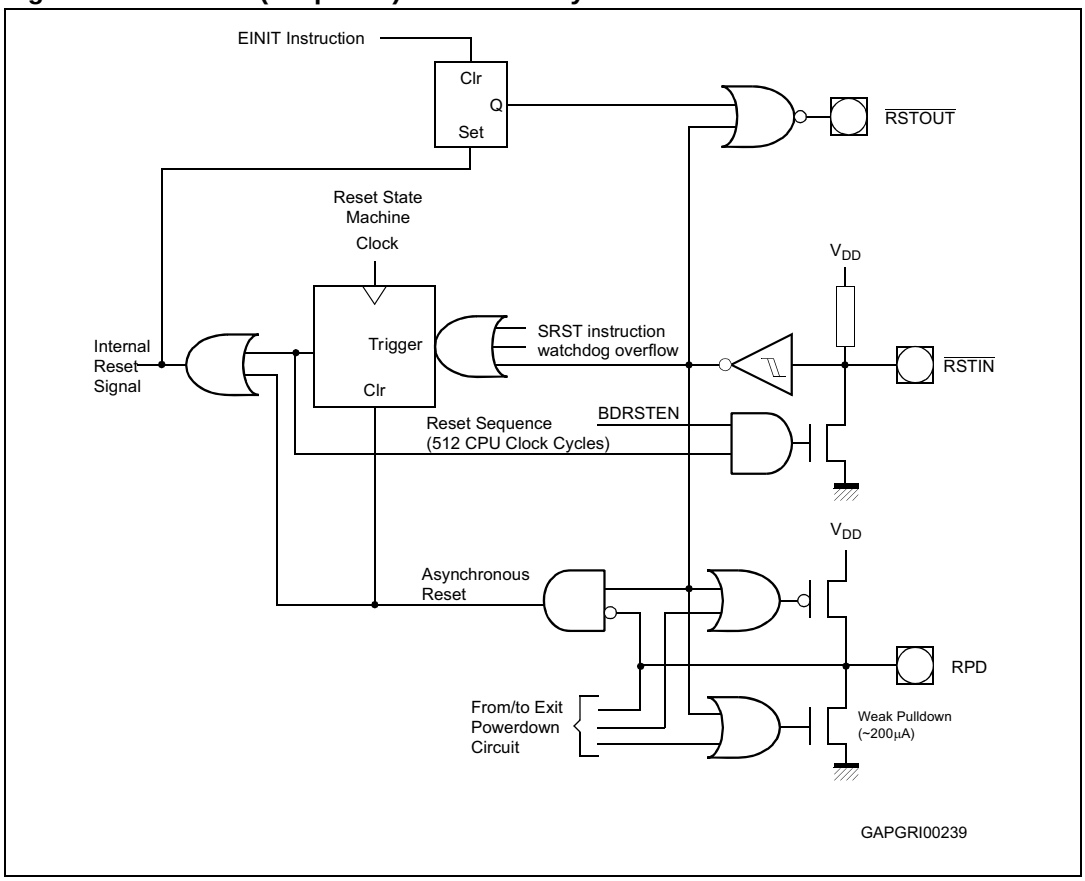


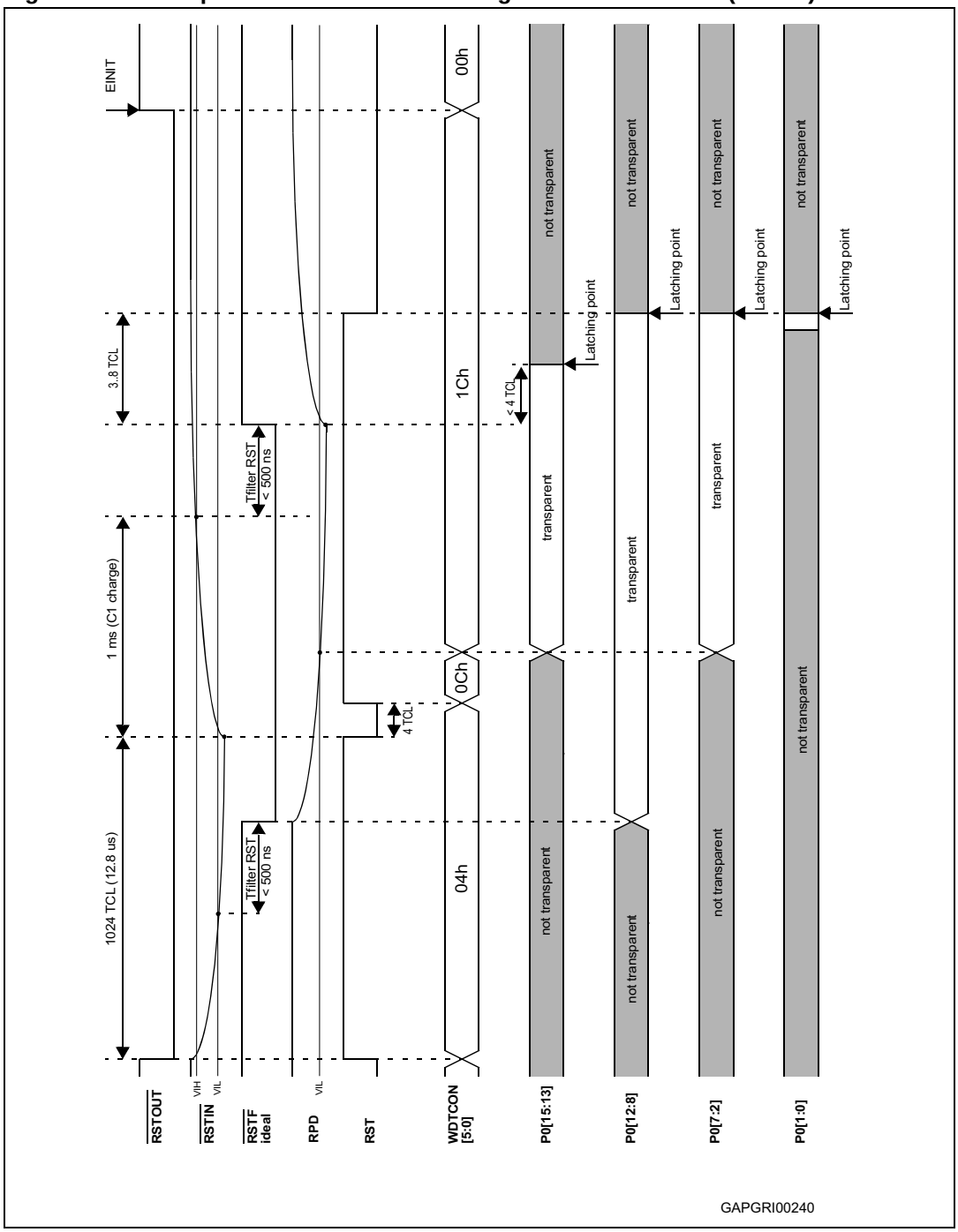
Figure 31. Internal (simplified) reset circuitry



20.8 Reset application examples

Next two timing diagrams (*Figure 32* and *Figure 33*) provides additional examples of bidirectional internal reset events (Software and Watchdog) including in particular the external capacitances charge and discharge transients (refer also to *Figure 30* for the external circuit scheme).

Figure 32. Example of software or watchdog bidirectional reset ($\overline{EA}$ = 1)



active: the portion of XRAM (16Kbytes for ST10F272E), the RTC counters and 32 kHz on-chip oscillator amplifier.

In normal running mode (that is when main V_{DD} is on) the V_{STBY} pin can be tied to V_{SS} during reset to exercise the $\overline{EA}$ functionality associated with the same pin: the voltage supply for the circuitries which are usually biased with V_{STBY} (see in particular the 32 kHz oscillator used in conjunction with Real Time Clock module), is granted by the active main V_{DD}.

It must be noted that Stand-by Mode can generate problems associated with the usage of different power supplies in CMOS systems; particular attention must be paid when the ST10F272 I/O lines are interfaced with other external CMOS integrated circuits: if V_{DD} of ST10F272 becomes (for example in Stand-by Mode) lower than the output level forced by the I/O lines of these external integrated circuits, the ST10F272 could be directly powered through the inherent diode existing on ST10F272 output driver circuitry. The same is valid for ST10F272 interfaced to active/inactive communication buses during Stand-by mode: current injection can be generated through the inherent diode.
Furthermore, the sequence of turning on/off of the different voltage could be critical for the system (not only for the ST10F272 device). The device Stand-by mode current (I_{STBY}) may vary while V_{DD} to V_{STBY} (and vice versa) transition occurs: some current flows between V_{DD} and V_{STBY} pins. System noise on both V_{DD} and V_{STBY} can contribute to increase this phenomenon.

21.3.1 Entering stand-by mode

As already said, to enter Stand-by Mode XRAM2EN bit in the XPERCON Register must be cleared: this allows to freeze immediately the RAM interface, avoiding any data corruption. As a consequence of a RESET event, the RAM Power Supply is switched to the internal low-voltage supply V_{18SB} (derived from V_{STBY} through the low-power voltage regulator). The RAM interface will remain frozen until the bit XRAM2EN is set again by software initialization routine (at next exit from main V_{DD} power-on reset sequence).

Since V_{18} is falling down (as a consequence of V_{DD} turning off), it can happen that the XRAM2EN bit is no longer able to guarantee its content (logic “0”), being the XPERCON Register powered by internal V_{18}. This does not generate any problem, because the Stand-by Mode switching dedicated circuit continues to confirm the RAM interface freezing, irrespective the XRAM2EN bit content; XRAM2EN bit status is considered again when internal V_{18} comes back over internal stand-by reference V_{18SB}.

If internal V_{18} becomes lower than internal stand-by reference (V_{18SB}) of about 0.3 to 0.45V with bit XRAM2EN set, the RAM Supply switching circuit is not active: in case of a temporary drop on internal V_{18} voltage versus internal V_{18SB} during normal code execution, no spurious Stand-by Mode switching can occur (the RAM is not frozen and can still be accessed).

The ST10F272 Core module, generating the RAM control signals, is powered by internal V_{18} supply; during turning off transient these control signals follow the V_{18}, while RAM is switched to V_{18SB} internal reference. It could happen that a high level of RAM write strobe from ST10F272 Core (active low signal) is low enough to be recognized as a logic “0” by the RAM interface (due to V_{18} lower than V_{18SB}): The bus status could contain a valid address for the RAM and an unwanted data corruption could occur. For this reason, an extra interface, powered by the switched supply, is used to prevent the RAM from this kind of potential corruption mechanism.

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
ODP7**b**	F1D2h**E**	E9h	Port 7 open drain control register	- - 00h
ODP8**b**	F1D6h**E**	EBh	Port 8 open drain control register	- - 00h
ONES**b**	FF1Eh	8Fh	Constant value 1's register (read only)	FFFFh
P0L **b**	FF00h	80h	PORT0 low register (lower half of PORT0)	- - 00h
P0H **b**	FF02h	81h	PORT0 high register (upper half of PORT0)	- - 00h
P1L **b**	FF04h	82h	PORT1 low register (lower half of PORT1)	- - 00h
P1H **b**	FF06h	83h	PORT1 high register (upper half of PORT1)	- - 00h
P2 **b**	FFC0h	E0h	Port 2 register	0000h
P3 **b**	FFC4h	E2h	Port 3 register	0000h
P4 **b**	FFC8h	E4h	Port 4 register (8-bit)	- - 00h
P5 **b**	FFA2h	D1h	Port 5 register (read only)	XXXXh
P6 **b**	FFCCh	E6h	Port 6 register (8-bit)	- - 00h
P7 **b**	FFD0h	E8h	Port 7 register (8-bit)	- - 00h
P8 **b**	FFD4h	EAh	Port 8 register (8-bit)	- - 00h
P5DIDIS**b**	FFA4h	D2h	Port 5 digital disable register	0000h
PECC0	FEC0h	60h	PEC channel 0 control register	0000h
PECC1	FEC2h	61h	PEC channel 1 control register	0000h
PECC2	FEC4h	62h	PEC channel 2 control register	0000h
PECC3	FEC6h	63h	PEC channel 3 control register	0000h
PECC4	FEC8h	64h	PEC channel 4 control register	0000h
PECC5	FECAh	65h	PEC channel 5 control register	0000h
PECC6	FECCh	66h	PEC channel 6 control register	0000h
PECC7	FECEh	67h	PEC channel 7 control register	0000h
PICON**b**	F1C4h**E**	E2h	Port input threshold control register	- - 00h
PP0	F038h**E**	1Ch	PWM module period register 0	0000h
PP1	F03Ah**E**	1Dh	PWM module period register 1	0000h
PP2	F03Ch**E**	1Eh	PWM module period register 2	0000h
PP3	F03Eh**E**	1Fh	PWM module period register 3	0000h
PSW**b**	FF10h	88h	CPU program status word	0000h
PT0	F030h**E**	18h	PWM module up/down counter 0	0000h
PT1	F032h**E**	19h	PWM module up/down counter 1	0000h
PT2	F034h**E**	1Ah	PWM module up/down counter 2	0000h
PT3	F036h**E**	1Bh	PWM module up/down counter 3	0000h
PW0	FE30h	18h	PWM module pulse width register 0	0000h

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
XPT2	EC14h	XPWM module up/down counter 2	0000h
XPT3	EC16h	XPWM module up/down counter 3	0000h
XPW0	EC30h	XPWM module pulse width register 0	0000h
XPW1	EC32h	XPWM module pulse width register 1	0000h
XPW2	EC34h	XPWM module pulse width register 2	0000h
XPW3	EC36h	XPWM module pulse width register 3	0000h
XPWMCON0	EC00h	XPWM module control register 0	0000h
XPWMCON0CLR	EC08h	XPWM module clear control reg. 0 (write only)	0000h
XPWMCON0SET	EC06h	XPWM module set control register 0 (write only)	0000h
XPWMCON1	EC02h	XPWM module control register 1	0000h
XPWMCON1CLR	EC0Ch	XPWM module clear control reg. 0 (write only)	0000h
XPWMCON1SET	EC0Ah	XPWM module set control register 0 (write only)	0000h
XPWMPORT	EC80h	XPWM module port control register	0000h
XS1BG	E906h	XASC Baud rate generator reload register	0000h
XS1CON	E900h	XASC control register	0000h
XS1CONCLR	E904h	XASC clear control register (write only)	0000h
XS1CONSET	E902h	XASC set control register (write only)	0000h
XS1PORT	E980h	XASC port control register	0000h
XS1RBUF	E90Ah	XASC receive buffer register	0000h
XS1TBUF	E908h	XASC transmit buffer register	0000h
XSSCBR	E80Ah	XSSC Baud rate register	0000h
XSSCCON	E800h	XSSC control register	0000h
XSSCCONCLR	E804h	XSSC clear control register (write only)	0000h
XSSCCONSET	E802h	XSSC set control register (write only)	0000h
XSSCPORT	E880h	XSSC port control register	0000h
XSSCRB	E808h	XSSC receive buffer	XXXXh
XSSCTB	E806h	XSSC transmit buffer	0000h

Table 62. Thermal characteristics

Symbol	Description	Value (typical)	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient PQFP 144 - 28 x 28 x 3.4 mm / 0.65 mm pitch LQFP 144 - 20 x 20 mm / 0.5 mm pitch LQFP 144 - 20 x 20 mm / 0.5 mm pitch on four layer FR4 board (2 layers signals / 2 layers power)	 30 40 35	°C/W

Based on thermal characteristics of the package and with reference to the power consumption figures provided in next tables and diagrams, the following product classification can be proposed. Anyhow, the exact power consumption of the device inside the application must be computed according to different working conditions, thermal profiles, real thermal resistance of the system (including printed circuit board or other substrata), I/O activity, and so on.

Table 63. Package characteristics

Package	Ambient temperature range	CPU frequency range
PQFP 144	–40 / +125°C	1 – 64MHz
LQFP 144	–40 / +125°C	1 – 40MHz

24.4 Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10F272 and its demands on the system.

Where the ST10F272 logic provides signals with their respective timing characteristics, the symbol “**CC**” for Controller Characteristics, is included in the “Symbol” column. Where the external system must provide signals with their respective timing characteristics to the ST10F272, the symbol “**SR**” for System Requirement, is included in the “Symbol” column.

accepted (minimum phase, high or low, again equal to 7.8ns).

3. The limits on input frequency are 4-8MHz since the usage of the internal oscillator amplifier is required. Also when the PLL is not used and the CPU clock corresponds to $F_{XTAL}/2$, an external crystal or resonator shall be used: it is not possible to force any clock though an external clock source.

24.8.4 Prescaler operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCL therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

24.8.5 Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled, the on-chip oscillator amplifier is bypassed and the CPU clock is directly driven by the input clock signal on XTAL1 pin.

The frequency of CPU clock (f_{CPU}) directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

Equation 18

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

DC= duty cycle

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$.

The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

Equation 19

$$2TCL = 1/f_{XTAL}$$

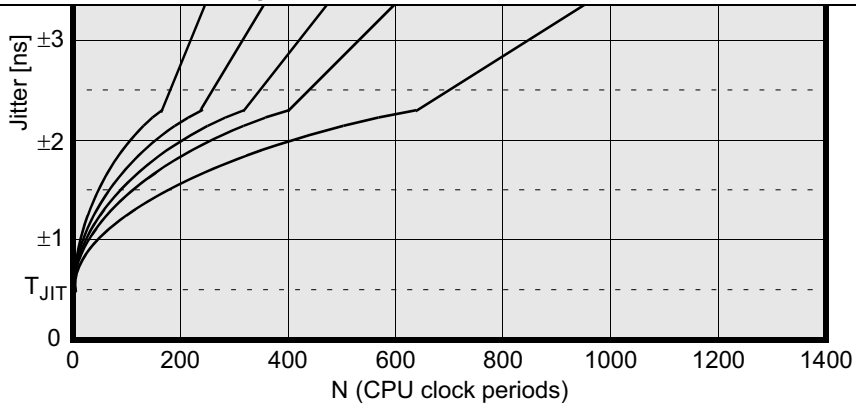
The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} \times DC_{max}$) instead of TCL_{min}.
Similarly to what happen for Prescaler Operation, if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

24.8.6 Oscillator watchdog (OWD)

An on-chip watchdog oscillator is implemented in the ST10F272. This feature is used for safety operation with external crystal oscillator (available only when using direct drive mode with or without prescaler, so the PLL is not used to generate the CPU clock multiplying the frequency of the external crystal oscillator). This watchdog oscillator operates as following.

contribution of the digital noise to the global jitter is widely taken into account in the curves provided in *Figure 45*.

Figure 45. ST10F272 PLL jitter



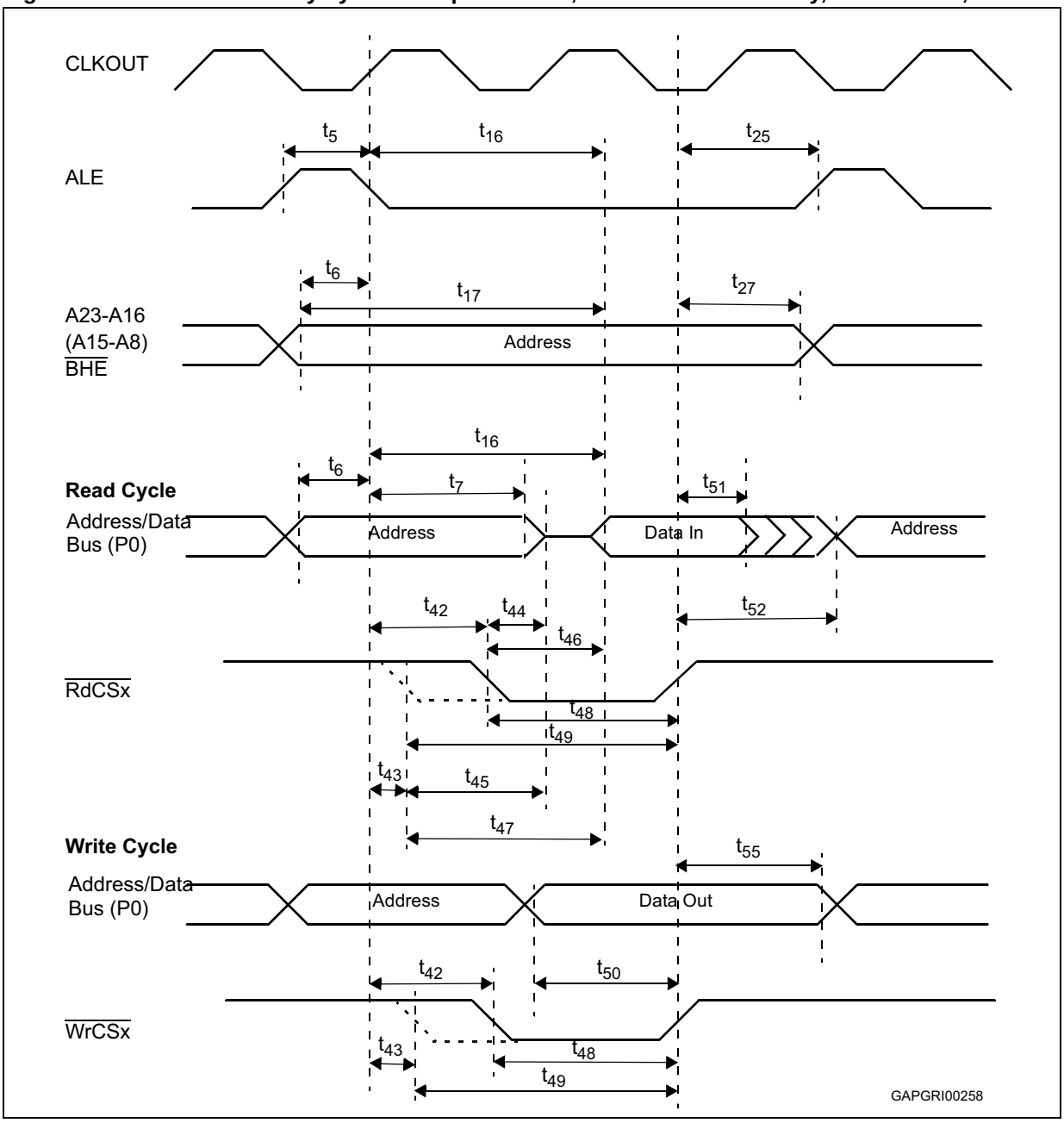
24.8.10 PLL lock / unlock

During normal operation, if the PLL gets unlocked for any reason, an interrupt request to the CPU is generated, and the reference clock (oscillator) is automatically disconnected from the PLL input: in this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency F_{free}). This feature allows to recover from a crystal failure occurrence without risking to go in an undefined configuration: the system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the $\overline{\text{RSTIN}}$ pin low.

Note: The external RC circuit on $\overline{\text{RSTIN}}$ pin shall be properly sized in order to extend the duration of the low pulse to grant the PLL gets locked before the level at $\overline{\text{RSTIN}}$ pin is recognized high: bidirectional reset internally drives $\overline{\text{RSTIN}}$ pin low for just 1024 TCL (definitively not sufficient to get the PLL locked starting from free-running mode).

Figure 51. External memory cycle: Multiplexed bus, with/without r/w delay, normal ALE, r/w CS



24.8.18 CLKOUT and $\overline{\text{READY}}$

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to + 125°C, CL = 50pF

Table 80. CLKOUT and $\overline{\text{READY}}$ timings

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU Clock 1/2 TCL = 1 to 64MHz		Unit
			min.	max.	min.	max.	
t_{29}	CC	CLKOUT cycle time	25	25	2TCL	2TCL	ns
t_{30}	CC	CLKOUT high time	9	–	TCL – 3.5	–	ns
t_{31}	CC	CLKOUT low time	10	–	TCL – 2.5	–	ns
t_{32}	CC	CLKOUT rise time	–	4	–	4	ns
t_{33}	CC	CLKOUT fall time	–	4	–	4	ns
t_{34}	CC	CLKOUT rising edge to ALE falling edge	$-2 + t_A$	$8 + t_A$	$-2 + t_A$	$8 + t_A$	ns
t_{35}	SR	Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	17	–	17	–	ns
t_{36}	SR	Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	2	–	2	–	ns
t_{37}	SR	Asynchronous $\overline{\text{READY}}$ low time	35	–	2TCL + 10	–	ns
t_{58}	SR	Asynchronous $\overline{\text{READY}}$ setup time [1]	17	–	17	–	ns
t_{59}	SR	Asynchronous $\overline{\text{READY}}$ hold time [1]	2	–	2	–	ns
t_{60}	SR	Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	0	$2t_A + t_C + t_F$	0	$2t_A + t_C + t_F$	ns

1. These timings are given for characterization purposes only, in order to assure recognition at a specific clock edge.
2. Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY. $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

26 Ordering information

Table 84. Order codes

Part number	Package	Packing	B/E Type	Temperature range (°C)	CPU frequency range (MHz)
F272-BAR-P	PQFP144	Tray	E	-40 to +125°C	1 to 64
F272-BAR-P-TX		Tape and reel			
F272-BAR-T	LQFP144	Tray	B	-40 to +125°C	1 to 40
F272-BAR-T-TX		Tape and reel			