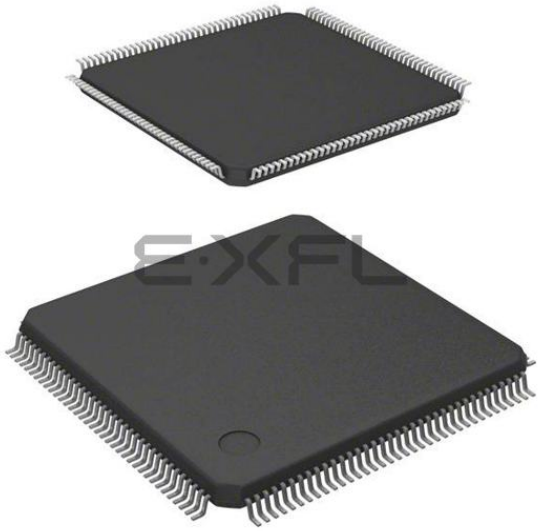

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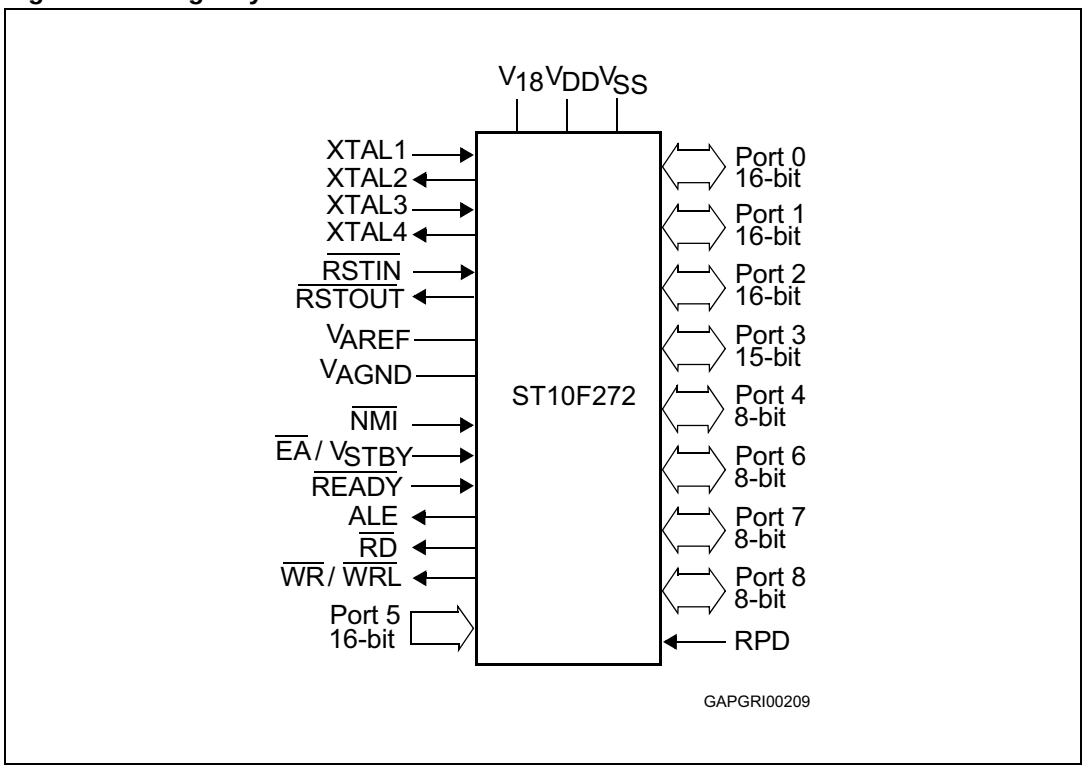
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f272-bage-t-tr

Figure 1. Logic symbol



4 Memory organization

The memory space of the ST10F272 is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Bytes. The entire memory space can be accessed Byte wise or Word wise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

IFLASH: 256K Bytes of on-chip Flash memory. It is divided in 8 blocks (B0F0...B0F7) that constitute the Bank 0. When Bootstrap mode is selected, the Test-Flash Block B0TF (8Kbyte) appears at address 00'0000h: refer to *Section 5: Internal Flash memory* for more details on memory mapping in boot mode. The summary of address range for IFLASH is the following:

Table 2. Summary of IFLASH address range

Blocks	User Mode	Size
B0TF	Not visible	8K
B0F0	00'0000h - 00'1FFFh	8K
B0F1	00'2000h - 00'3FFFh	8K
B0F2	00'4000h - 00'5FFFh	8K
B0F3	00'6000h - 00'7FFFh	8K
B0F4	01'8000h - 01'FFFFh	32K
B0F5	02'0000h - 02'FFFFh	64K
B0F6	03'0000h - 03'FFFFh	64K
B0F7	04'0000h - 04'FFFFh	64K

IRAM: 2K Bytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers group.

XRAM: 8K/16K+2K Bytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is divided into 2 areas, the first 2K Bytes named XRAM1 and the second 8K/16K Bytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (31.25ns access at 64MHz CPU clock). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set. If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The XRAM2 address range is the one selected programming XADRS3 register, if XPEN (bit 2 of SYSCON register), and XRAM2EN (bit 3 of XPERCON register) are set. If bit XPEN is cleared, then any access in the address range programmed for XRAM2 will be directed to

7.1 Multiplier-accumulator unit (MAC)

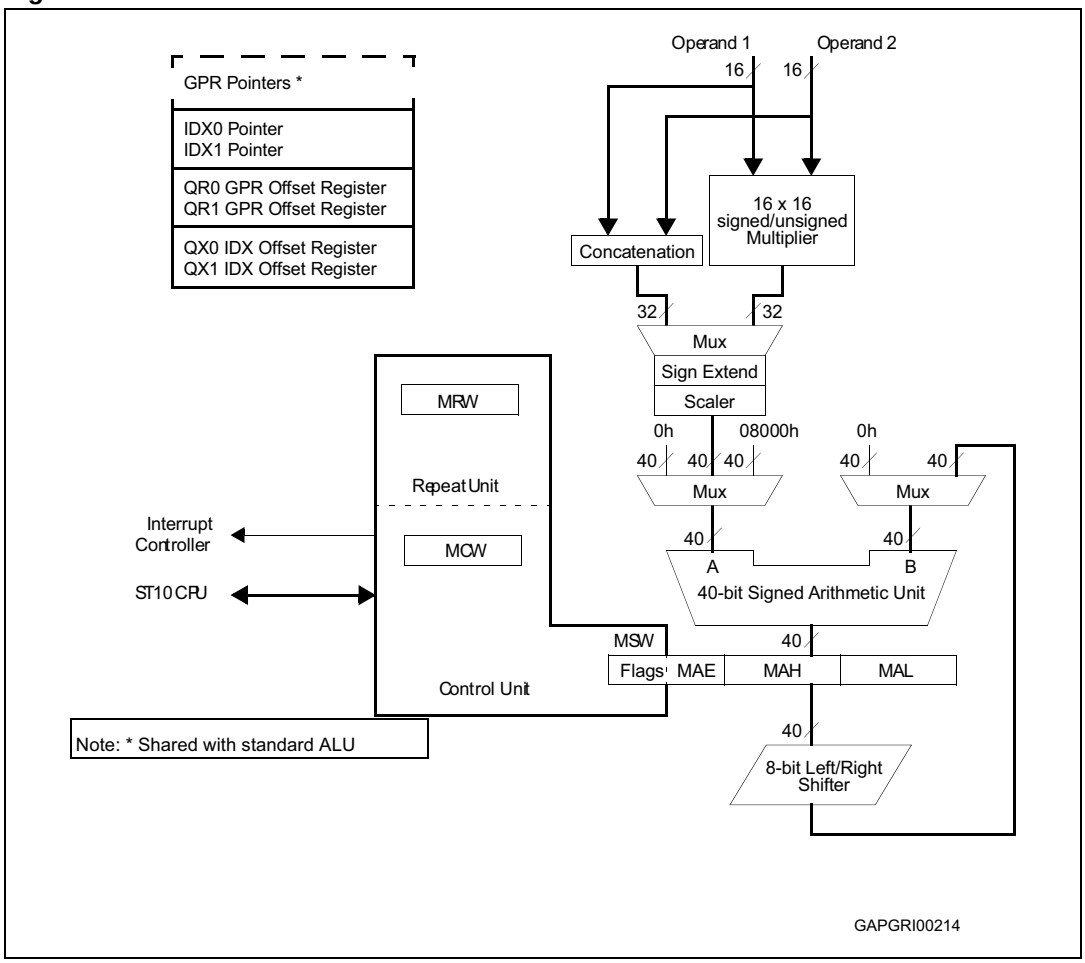
The MAC co-processor is a specialized co-processor added to the ST10 CPU Core in order to improve the performances of the ST10 Family in signal processing algorithms.

The standard ST10 CPU has been modified to include new addressing capabilities which enable the CPU to supply the new co-processor with up to 2 operands per instruction cycle.

This new co-processor (so-called MAC) contains a fast multiply-accumulate unit and a repeat unit.

The co-processor instructions extend the ST10 CPU instruction set with multiply, multiply-accumulate, 32-bit signed arithmetic operations.

Figure 7. MAC unit architecture



8 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16- / 18- / 20- / 24-bit addresses and 16-bit data, demultiplexed
- 16- / 18- / 20- / 24-bit addresses and 16-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input / output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a ‘Ready’ function.

A $\overline{HOLD}$ / $\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, HLDA, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the HLDA pin is an output. By setting bit DP6.7 to’1’ the slave mode is selected where pin HLDA is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16M Bytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

Table 29. Interrupt sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4h	2Dh
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8h	2Eh
SSC Error	SCEIR	SCEIE	SCEINT	00'00BCh	2Fh
PWM Channel 0...3	PWMIR	PWMIE	PWMINT	00'00FCh	3Fh
See *Section 9.1*	XP0IR	XP0IE	XP0INT	00'0100h	40h
See *Section 9.1*	XP1IR	XP1IE	XP1INT	00'0104h	41h
See *Section 9.1*	XP2IR	XP2IE	XP2INT	00'0108h	42h
See *Section 9.1*	XP3IR	XP3IE	XP3INT	00'010Ch	43h

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any other program execution. Hardware trap services cannot not be interrupted by standard interrupt or by PEC interrupts.

9.1 X-Peripheral interrupt

The limited number of X-Bus interrupt lines of the present ST10 architecture, imposes some constraints on the implementation of the new functionality. In particular, the additional X-Peripherals SSC1, ASC1, I^2C, PWM1 and RTC need some resources to implement interrupt and PEC transfer capabilities. For this reason, a multiplexed structure for the interrupt management is proposed. In the next *Figure 8*, the principle is explained through a simple diagram, which shows the basic structure replicated for each of the four X-interrupt available vectors (XP0INT, XP1INT, XP2INT and XP3INT).

It is based on a set of 16-bit registers XIRxSEL (x=0,1,2,3), divided in two portions each:

- Byte High XIRxSEL[15:8] Interrupt Enable bits
- Byte Low XIRxSEL[7:0] Interrupt Flag bits

Table 30. X-Interrupt detailed mapping (continued)

	XP0INT	XP1INT	XP2INT	XP3INT
ASC1 Transmit	x	x	x	
ASC1 Transmit Buffer	x	x	x	
ASC1 Error				x
PLL Unlock / OWD				x
PWM1 Channel 3...0			x	x

9.2 Exception and error traps list

Table 31 shows all of the possible exceptions or error conditions that can arise during run-time.

Table 31. Trap priorities

Exception condition	Trap flag	Trap vector	Vector location	Trap number	Trap* priority
Reset Functions: Hardware Reset Software Reset Watchdog Timer Overflow		 RESET RESET RESET	 00'0000h 00'0000h 00'0000h	 00h 00h 00h	 III III III
Class A Hardware Traps: Non-Maskable Interrupt Stack Overflow Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 00'0008h 00'0010h 00'0018h	 02h 04h 06h	 II II II
Class B Hardware Traps: Undefined Opcode MAC Interruption Protected Instruction Fault Illegal word Operand Access Illegal Instruction Access Illegal External Bus Access	 UNDOPC MACTRP PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP BTRAP	 00'0028h 00'0028h 00'0028h 00'0028h 00'0028h 00'0028h	 0Ah 0Ah 0Ah 0Ah 0Ah 0Ah	 I I I I I I
Reserved			[002Ch - 003Ch]	[0Bh - 0Fh]	
Software Traps TRAP Instruction			Any 0000h – 01FCh in steps of 4h	Any [00h - 7Fh]	Current CPU Priority

*Note: * - All the class B traps have the same trap number (and vector) and the same lower priority compare to the class A traps and to the resets.*

- Each class A traps has a dedicated trap number (and vector). They are prioritized in the second priority level.

- The resets have the highest priority level and the same trap number.

- The PSW.ILVL CPU priority is forced to the highest level (15) when these exceptions are serviced.

12 PWM modules

Two pulse width modulation modules are available on ST10F272: standard PWM0 and XBUS PWM1. They can generate up to four PWM output signals each, using edge-aligned or centre-aligned PWM. In addition, the PWM modules can generate PWM burst signals and single shot outputs. The *Table 39* and *Table 40* show the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM modules can generate interrupt requests.

Figure 11. Block diagram of PWM module

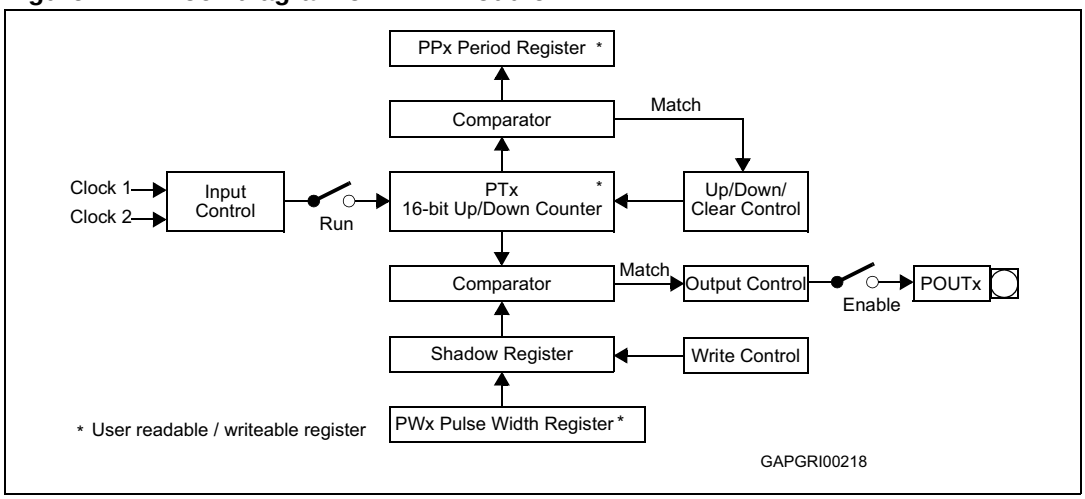
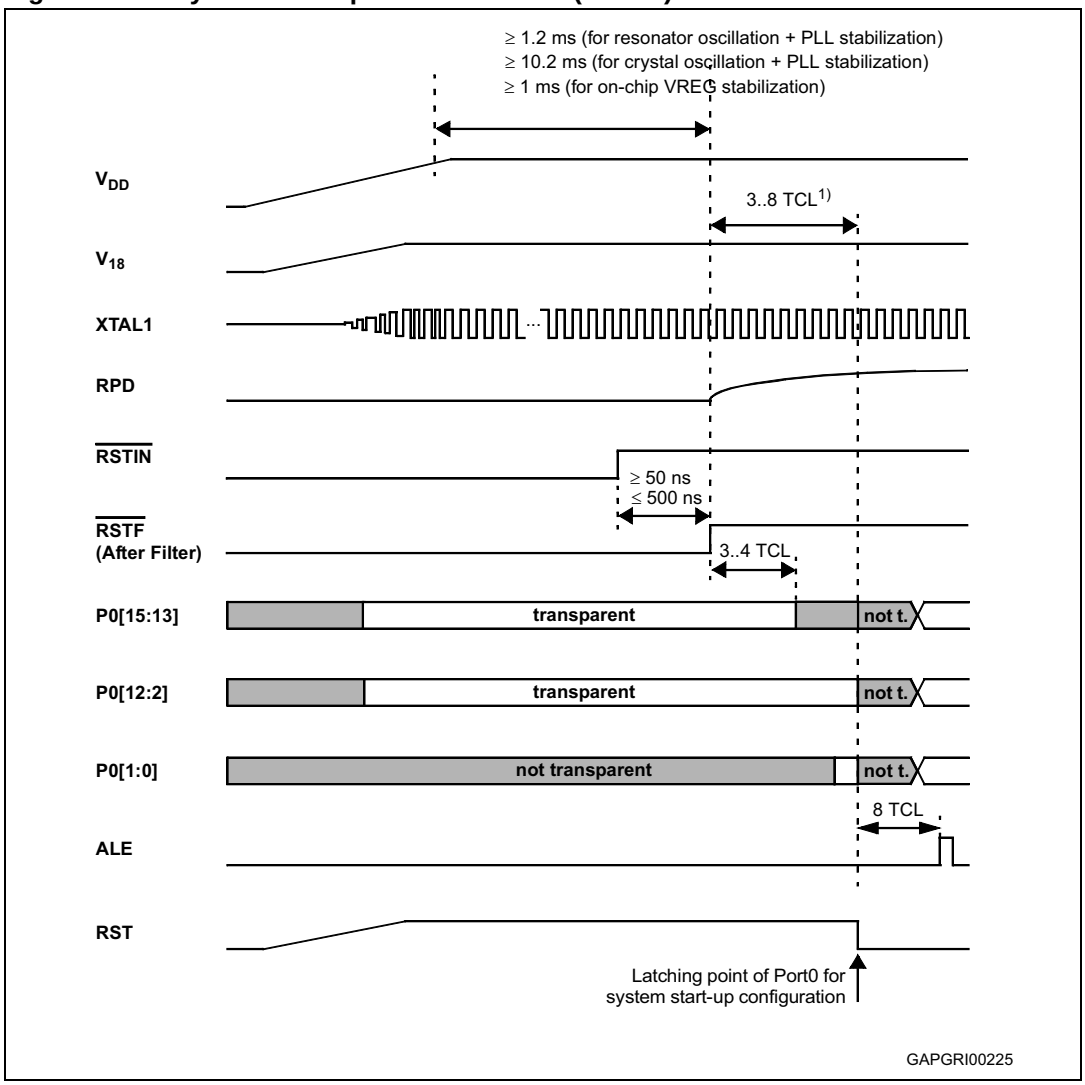


Table 39. PWM unit frequencies and resolutions at 40 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	25ns	156.25 kHz	39.1 kHz	9.77 kHz	2.44Hz	610Hz
CPU Clock/64	1.6µs	2.44 kHz	610Hz	152.6Hz	38.15Hz	9.54Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	25ns	78.12 kHz	19.53 kHz	4.88 kHz	1.22 kHz	305.2Hz
CPU Clock/64	1.6µs	1.22 kHz	305.17Hz	76.29Hz	19.07Hz	4.77Hz

Figure 17. Asynchronous power-on RESET ($\overline{EA}$ = 0)

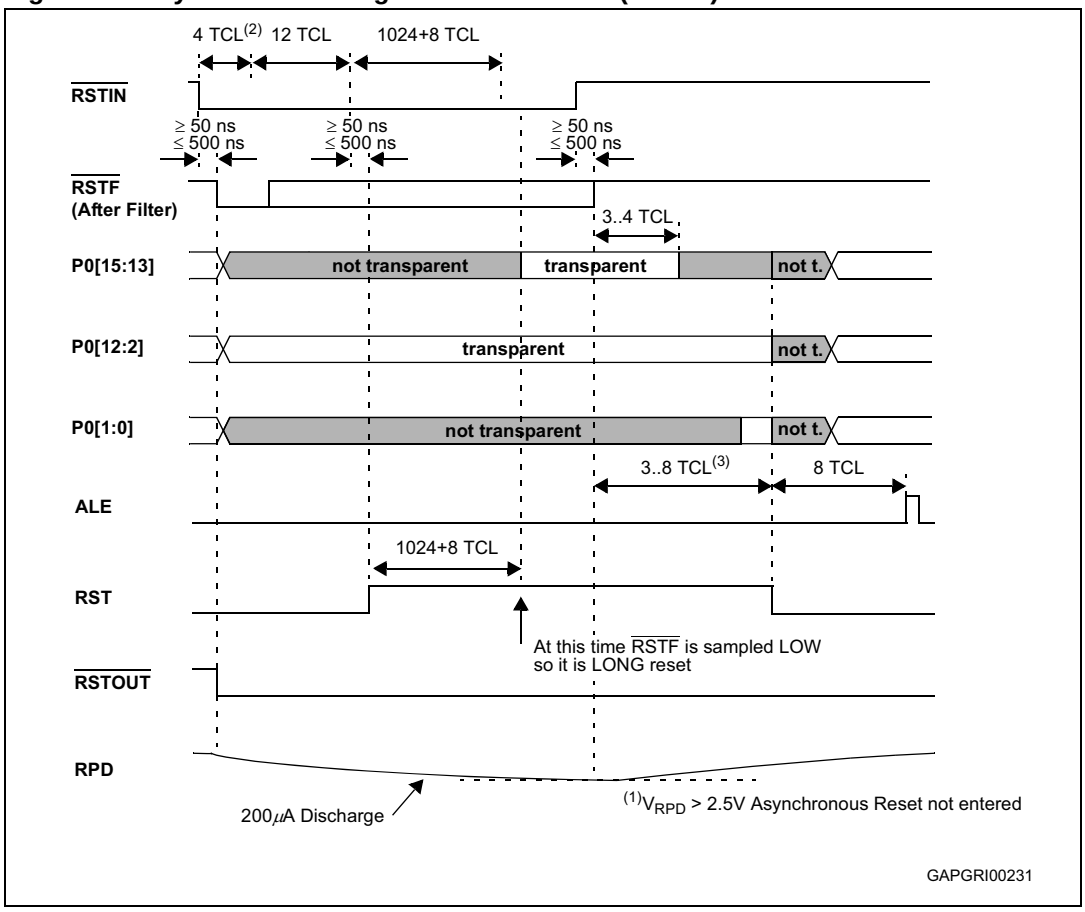


1. 3 to 8 TLC depending on clock source selection.

Hardware reset

The asynchronous reset must be used to recover from catastrophic situations of the application. It may be triggered by the hardware of the application. Internal hardware logic and application circuitry are described in *Section 20.7: Reset circuitry* and *Figure 29*, *Figure 30* and *Figure 31*. It occurs when $\overline{RSTIN}$ is low and RPD is detected (or becomes) low as well.

Figure 23. Synchronous long hardware RESET ($\overline{EA}$ = 0)



1. If during the reset condition (RSTIN low), RPD voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.
2. Minimum RSTIN low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to *Section 21.1*).
3. 3 to 8 TCL depending on clock source selection.

20.4 Software reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (that is written at '1').

A Software reset is always taken as synchronous: there is no influence on Software Reset behavior with RPD status. In case Bidirectional Reset is selected, a Software Reset event pulls $\overline{RSTIN}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{RSTIN}$ pin is not pulled low even though Bidirectional Reset is selected.

Refer to *Figure 24* and *Figure 25* for unidirectional SW reset timing, and to *Figure 26*, *Figure 27* and *Figure 28* for bidirectional.

or Watchdog Reset become a Short Hardware Reset. On the contrary, if RSTF remains low for less than 4 TCL, the device simply exits reset state.

The Bidirectional reset is not effective in case RPD is held low, when a Software or Watchdog reset event occurs. On the contrary, if a Software or Watchdog Bidirectional reset event is active and RPD becomes low, the RSTIN pin is immediately released, while the internal reset sequence is completed regardless of RPD status change (1024 TCL).

Note: The bidirectional reset function is disabled by any reset sequence (bit BDRSTEN of SYSCON is cleared). To be activated again it must be enabled during the initialization routine.

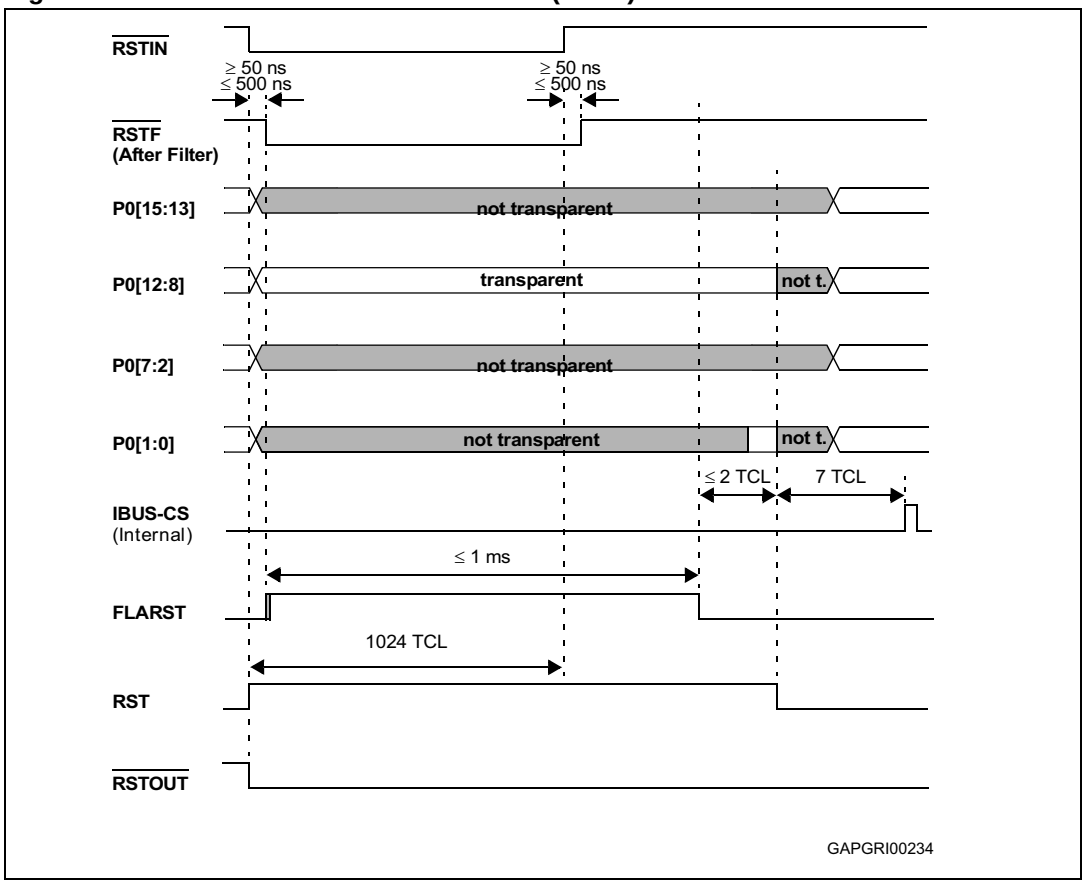
WDTCON flags

Similarly to what already highlighted in the previous section when discussing about Short reset and the degeneration into Long reset, similar situations may occur when Bidirectional reset is enabled. The presence of the internal filter on RSTIN pin introduces a delay: when RSTIN is released, the internal signal after the filter (see RSTF in the drawings) is delayed, so it remains still active (low) for a while. It means that depending on the internal clock speed, a short reset may be recognized as a long reset: the WDTCON flags are set accordingly.

Besides, when either Software or Watchdog bidirectional reset events occur, again when the RSTIN pin is released (at the end of the internal reset sequence), the RSTF internal signal (after the filter) remains low for a while, and depending on the clock frequency it is recognized high or low: 8TCL after the completion of the internal sequence, the level of RSTF signal is sampled, and if recognized still low a Hardware reset sequence starts, and WDTCON will flag this last event, masking the previous one (Software or Watchdog reset). Typically, a Short Hardware reset is recognized, unless the RSTIN pin (and consequently internal signal RSTF) is sufficiently held low by the external hardware to inject a Long Hardware reset. After this occurrence, the initialization routine is not able to recognize a Software or Watchdog bidirectional reset event, since a different source is flagged inside WDTCON register. This phenomenon does not occur when internal FLASH is selected during reset (EA = 1), since the initialization of the FLASH itself extend the internal reset duration well beyond the filter delay.

Figure 26, *Figure 27* and *Figure 28* summarize the timing for Software and Watchdog Timer Bidirectional reset events: in particular *Figure 28* shows the degeneration into Hardware reset.

Figure 26. SW / WDT bidirectional RESET ($\overline{EA}$=1)



20.9 Reset summary

A summary of the different reset events is reported in *Table 50*.

Table 50. Reset event

Event	RPD	EA	Bidir	Synch. Asynch.	RSTIN		WDTCON Flags				
					min	max	PONR	LHWR	SHWR	SWR	WDTR
Power-on Reset	0	0	N	Asynch.	1 ms (VREG) 1.2 ms (Reson. + PLL) 10.2 ms (Crystal + PLL)	-	1	1	1	1	0
	0	1	N	Asynch.	1ms (VREG)	-	1	1	1	1	0
	1	x	x	FORBIDDEN							
	x	x	Y	NOT APPLICABLE							
Hardware Reset (Asynchronous)	0	0	N	Asynch.	500ns	-	0	1	1	1	0
	0	1	N	Asynch.	500ns	-	0	1	1	1	0
	0	0	Y	Asynch.	500ns	-	0	1	1	1	0
	0	1	Y	Asynch.	500ns	-	0	1	1	1	0
Short Hardware Reset (Synchronous) (1)	1	0	N	Synch.	max (4 TCL, 500ns)	1032 + 12 TCL + max(4 TCL, 500ns)	0	0	1	1	0
	1	1	N	Synch.	max (4 TCL, 500ns)	1032 + 12 TCL + max(4 TCL, 500ns)	0	0	1	1	0
	1	0	Y	Synch.	max (4 TCL, 500ns)	1032 + 12 TCL + max(4 TCL, 500ns)	0	0	1	1	0
					Activated by internal logic for 1024 TCL						
	1	1	Y	Synch.	max (4 TCL, 500ns)	1032 + 12 TCL + max(4 TCL, 500ns)	0	0	1	1	0
					Activated by internal logic for 1024 TCL						
Long Hardware Reset (Synchronous)	1	0	N	Synch.	1032 + 12 TCL + max(4 TCL, 500ns)	-	0	1	1	1	0
	1	1	N	Synch.	1032 + 12 TCL + max(4 TCL, 500ns)	-	0	1	1	1	0
	1	0	Y	Synch.	1032 + 12 TCL + max(4 TCL, 500ns)	-	0	1	1	1	0
					Activated by internal logic only for 1024 TCL						
	1	1	Y	Synch.	1032 + 12 TCL + max(4 TCL, 500ns)	-	0	1	1	1	0
					Activated by internal logic only for 1024 TCL						

active: the portion of XRAM (16Kbytes for ST10F272E), the RTC counters and 32 kHz on-chip oscillator amplifier.

In normal running mode (that is when main V_{DD} is on) the V_{STBY} pin can be tied to V_{SS} during reset to exercise the $\overline{EA}$ functionality associated with the same pin: the voltage supply for the circuitries which are usually biased with V_{STBY} (see in particular the 32 kHz oscillator used in conjunction with Real Time Clock module), is granted by the active main V_{DD}.

It must be noted that Stand-by Mode can generate problems associated with the usage of different power supplies in CMOS systems; particular attention must be paid when the ST10F272 I/O lines are interfaced with other external CMOS integrated circuits: if V_{DD} of ST10F272 becomes (for example in Stand-by Mode) lower than the output level forced by the I/O lines of these external integrated circuits, the ST10F272 could be directly powered through the inherent diode existing on ST10F272 output driver circuitry. The same is valid for ST10F272 interfaced to active/inactive communication buses during Stand-by mode: current injection can be generated through the inherent diode.
Furthermore, the sequence of turning on/off of the different voltage could be critical for the system (not only for the ST10F272 device). The device Stand-by mode current (I_{STBY}) may vary while V_{DD} to V_{STBY} (and vice versa) transition occurs: some current flows between V_{DD} and V_{STBY} pins. System noise on both V_{DD} and V_{STBY} can contribute to increase this phenomenon.

21.3.1 Entering stand-by mode

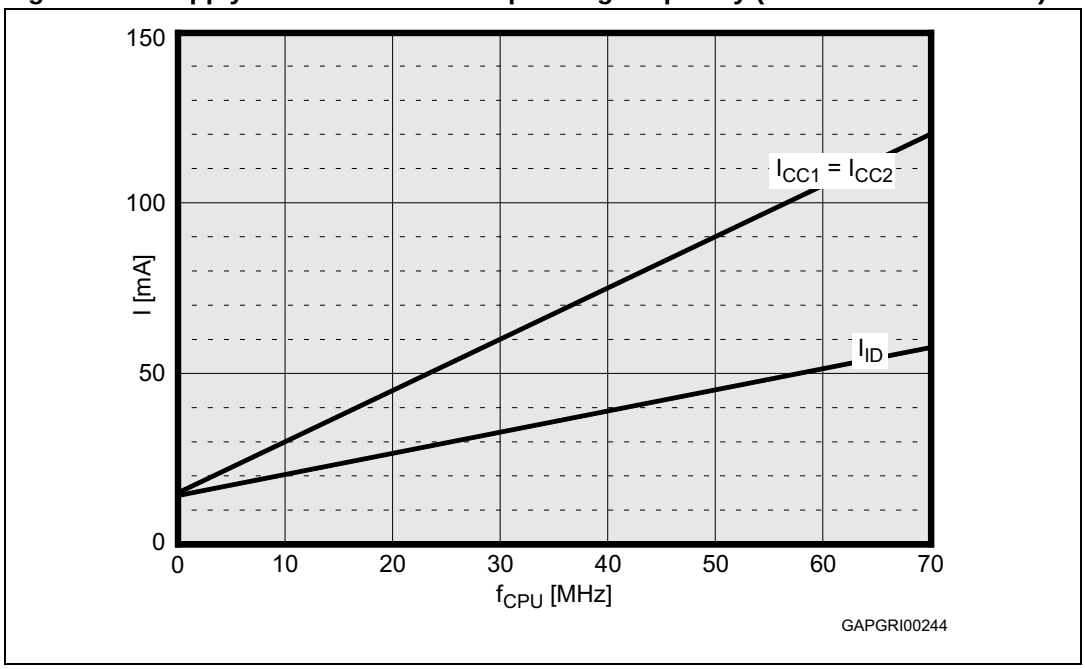
As already said, to enter Stand-by Mode XRAM2EN bit in the XPERCON Register must be cleared: this allows to freeze immediately the RAM interface, avoiding any data corruption. As a consequence of a RESET event, the RAM Power Supply is switched to the internal low-voltage supply V_{18SB} (derived from V_{STBY} through the low-power voltage regulator). The RAM interface will remain frozen until the bit XRAM2EN is set again by software initialization routine (at next exit from main V_{DD} power-on reset sequence).

Since V_{18} is falling down (as a consequence of V_{DD} turning off), it can happen that the XRAM2EN bit is no longer able to guarantee its content (logic “0”), being the XPERCON Register powered by internal V_{18}. This does not generate any problem, because the Stand-by Mode switching dedicated circuit continues to confirm the RAM interface freezing, irrespective the XRAM2EN bit content; XRAM2EN bit status is considered again when internal V_{18} comes back over internal stand-by reference V_{18SB}.

If internal V_{18} becomes lower than internal stand-by reference (V_{18SB}) of about 0.3 to 0.45V with bit XRAM2EN set, the RAM Supply switching circuit is not active: in case of a temporary drop on internal V_{18} voltage versus internal V_{18SB} during normal code execution, no spurious Stand-by Mode switching can occur (the RAM is not frozen and can still be accessed).

The ST10F272 Core module, generating the RAM control signals, is powered by internal V_{18} supply; during turning off transient these control signals follow the V_{18}, while RAM is switched to V_{18SB} internal reference. It could happen that a high level of RAM write strobe from ST10F272 Core (active low signal) is low enough to be recognized as a logic “0” by the RAM interface (due to V_{18} lower than V_{18SB}): The bus status could contain a valid address for the RAM and an unwanted data corruption could occur. For this reason, an extra interface, powered by the switched supply, is used to prevent the RAM from this kind of potential corruption mechanism.

Figure 37. Supply current versus the operating frequency (RUN and IDLE modes)



(sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the following relation:

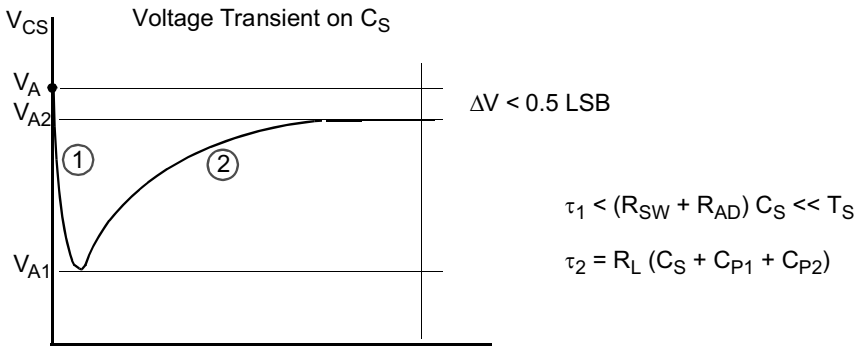
Equation 1

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

The formula above provides a constraints for external network design, in particular on resistive path.

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 39*), when the sampling phase is started (A/D switch close), a charge sharing phenomena is installed.

Figure 40. Charge sharing timing diagram during sampling phase



In particular two different transient periods can be distinguished (see *Figure 40*):

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitance C_P and C_S are in series, and the time constant is:

Equation 2

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

- This relation can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D Converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 3

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S < \quad < T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to the following equation:

Equation 4

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 5

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 6

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) \leq T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. The following equation must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 7

$$V_{A2}(C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1}(C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing (see *Figure 41*).

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

Example of external network sizing

The following hypothesis are formulated in order to proceed in designing the external network on A/D Converter input pins:

- Analog Signal Source Bandwidth (f_0):10kHz
- conversion Rate (f_C):25kHz
- Sampling Time (T_S):1µs
- Pin Input Capacitance (C_{P1}):5pF
- Pin Input Routing Capacitance (C_{P2}):1pF
- Sampling Capacitance (C_S):4pF
- Maximum Input Current Injection (I_{INJ}):3mA
- Maximum Analog Source Voltage ($V_{AM)}$:12V
- Analog Source Impedance (R_S):100Ω
- Channel Switch Resistance (R_{SW}):500Ω
- Sampling Switch Resistance (R_{AD}):200Ω

1. Supposing to design the filter with the pole exactly at the maximum frequency of the signal, the time constant of the filter is:

Equation 10

$$R_C C_F = \frac{1}{2\pi f_0} = 15.9\mu s$$

2. Using the relation between C_F and C_S and taking some margin (4000 instead of 2048), it is possible to define C_F:

Equation 11

$$C_F = 4000\, C_S = 16nF$$

3. As a consequence of step 1 and 2, RC can be chosen:

Equation 12

$$R_F = \frac{1}{2\pi f_0 C_F} = 995\Omega \cong 1k\Omega$$

4. Considering the current injection limitation and supposing that the source can go up to 12V, the total series resistance can be defined as:

Equation 13

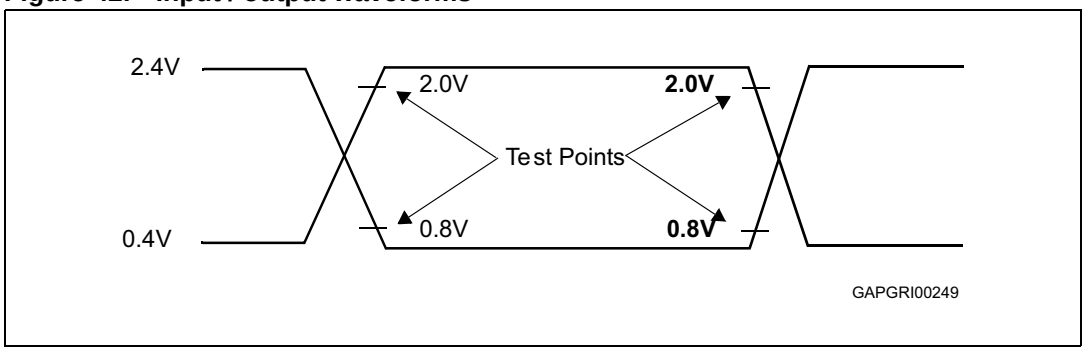
$$R_S + R_F + R_L = \frac{V_{AM}}{I_{INJ}} = 4k\Omega$$

from which is now simple to define the value of R_L:

24.8 AC characteristics

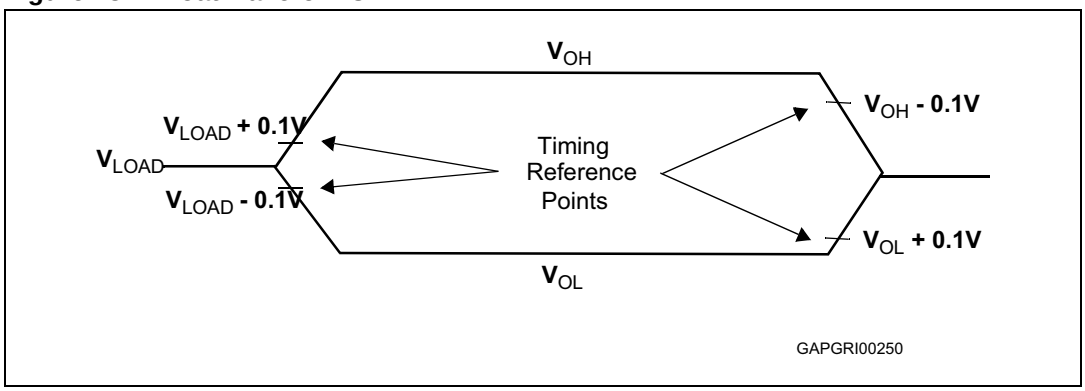
24.8.1 Test waveforms

Figure 42. Input / output waveforms



Note: AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at V_{IH} min. for a logic '1' and V_{IL} max for a logic '0'.

Figure 43. Float waveforms



Note: For timing purposes a port pin is no longer floating when V_{LOAD} changes of ±100mV.
It begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20mA).

24.8.2 Definition of internal timing

The internal operation of the ST10F272 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL".

The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}.

This influence must be regarded when calculating the timings for the ST10F272.

The example for PLL operation shown in *Figure 44* refers to a PLL factor of 4.

Table 73. Main oscillator negative resistance (module)

	C_A = 15pF			C_A = 25pF			C_A = 35pF		
	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.
4 MHz	545 Ω	1035 Ω	–	550 Ω	1050 Ω	–	430 Ω	850 Ω	–
8 MHz	240 Ω	450 Ω	–	170 Ω	350 Ω	–	120 Ω	250 Ω	–

The given values of C_A do not include the stray capacitance of the package and of the printed circuit board: the negative resistance values are calculated assuming additional 5pF to the values in the table. The crystal shunt capacitance (C_0) and the package capacitance between XTAL1 and XTAL2 pins is globally assumed equal to 10pF.

The external resistance between XTAL1 and XTAL2 is not necessary, since already present on the silicon.

24.8.12 32 kHz oscillator specifications

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = –40 to +125°C

Table 74. 32kHz oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			min.	typ.	max.	
g_{m32}	Oscillator Transconductance [1]	Start-up	20	31	50	µA/V
		Normal run	8	17	30	µA/V
V_{OSC32}	Oscillation Amplitude [2]	Peak to Peak	0.5	1.0	2.4	V
V_{AV32}	Oscillation Voltage level [2]	Sine wave middle	0.7	0.9	1.2	V
t_{STUP32}	Oscillator Start-up Time [2]	Stable V_{DD}	–	1	5	s

1. At power-on a high current biasing is applied for faster oscillation start-up. Once the oscillation is started, the current biasing is reduced to lower the power consumption of the system.
2. Not 100% tested, guaranteed by design characterization.

24.8.19 External bus arbitration

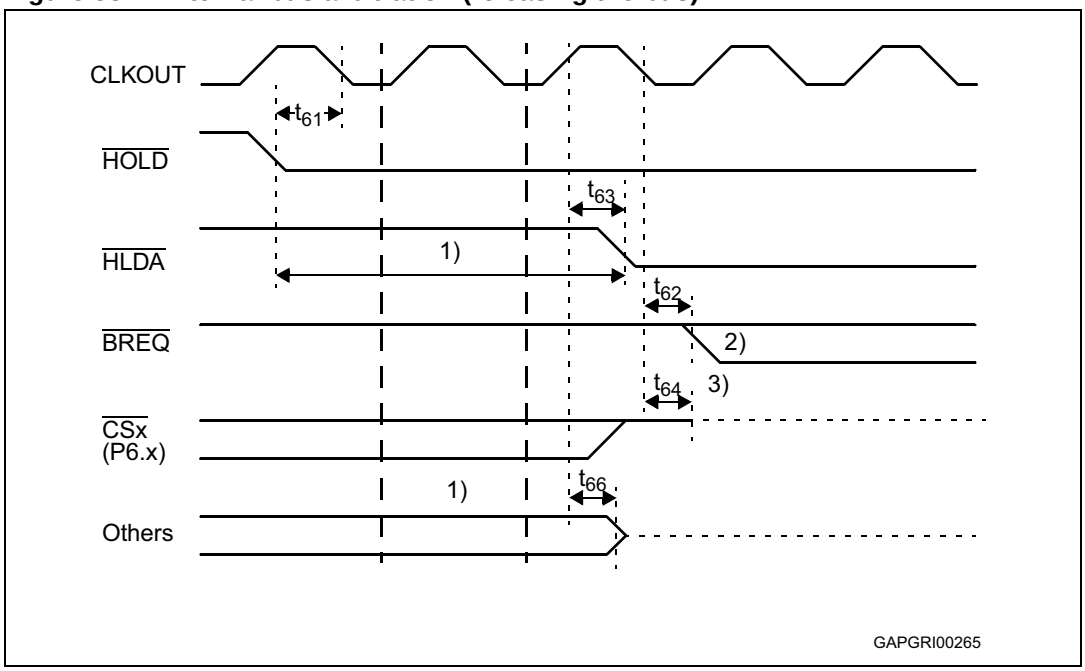
V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C, C_L = 50pF

Table 81. External bus arbitration timings

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU Clock 1/2 TCL = 1 to 64MHz		Unit
			min.	max.	min.	max.	
t_{61}	SR	$\overline{HOLD}$ input setup time to CLKOUT	18.5	–	18.5	–	ns
t_{62}	CC	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	12.5	–	12.5	ns
t_{63}	CC	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	–	12.5	–	12.5	ns
t_{64}	CC	$\overline{CSx}$ release [1]	–	20	–	20	ns
t_{65}	CC	$\overline{CSx}$ drive	– 4	15	– 4	15	ns
t_{66}	CC	Other signals release [1]	–	20	–	20	ns
t_{67}	CC	Other signals drive	– 4	15	– 4	15	ns

1. Partially tested, guaranteed by design characterization.

Figure 58. External bus arbitration (releasing the bus)



1. The ST10F272 will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.