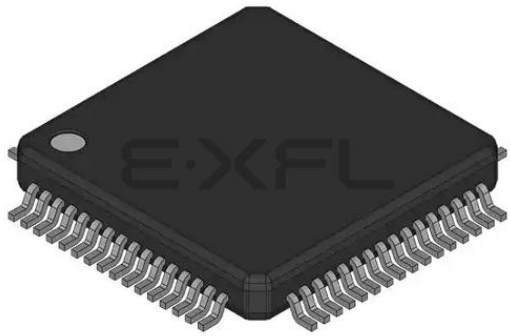


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | SIO, UART/USART |
| Peripherals | LCD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-BQFP |
| Supplier Device Package | 64-QIPE (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/sanyo-denki-sanups-products/lc87f7j32au-qip-e |

■Ports

- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units 15 (P1n, P30 to P31, P70 to P73, XT2)
  Ports whose I/O direction can be designated in 4 bit units 8 (P0n)
  (When N-channel open drain output is selected, data can be input in bit units.)
- Normal withstand voltage input port 1 (XT1)
- LCD ports
  Segment output 24 (S00 to S23)
  Common output 4 (COM0 to COM3)
  Bias terminals for LCD driver 3 (V1 to V3)
  Other functions
  Input/output ports 24 (PAn, PBn, PCn,)
  Input ports 7 (PLn)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pin 1 ($\overline{\text{RES}}$)
- Power pins 6 ($V_{SS}1$ to $V_{SS}3$, $V_{DD}1$ to $V_{DD}3$)

■LCD Controller

1) Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
2) Segment output and common output can be switched to general-purpose input/output ports

■Timers

- Timer 0: 16-bit timer/counter with two capture registers.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers)
  + 8-bit counter (with two 8-bit capture registers)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs)
  + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)
  (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8: 16-bit timer
  Mode 0: 8-bit timer with an 8-bit prescaler × 2 channels (with toggle output)
  Mode 1: 16-bit timer with an 8-bit prescaler (with toggle output)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes
- Day and time counter
  1) Using with a base timer,it can be used as 65000 day + minute + second counter.

■High-speed Clock Counter

1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Can generate output real-time.

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8-data bits, 1-stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8-data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8-data bits, stop detect)

■UART
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD Converter: 12-bits/8-bits × 12 channels
- 12 bits/8 bits AD converter resolution selectable

■PWM: Multi frequency 12-bit PWM × 2 channels

■Infrared Remote Control Receiver Circuit
1) Noise reduction function
   (noise filter time constant: Approx. 120μs, when the 32.768kHz crystal oscillator is selected as the reference voltage source.)
2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding
3) X'tal HOLD mode release function

■Watchdog Timer
- External RC watchdog timer
- Basetimer watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
2) Able to output oscillation clock of sub clock.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  (Some parts of the serial transfer function stops operation)
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, X'tal, and frequency variable RC oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5, pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and the remote control circuit.
  1) The CF, RC, and frequency variable RC oscillators automatically stop operation
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4,and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an interrupt source established in the infrared remote control receiver circuit

■On-chip Debugger

- Supports software debugging with the IC mounted on the target board.

■Package Form

- QIP64E(14×14): Lead-free type
- TQFP64J(10×10): Lead-free type

■Development Tools

- On-chip debugger: TCB87-TypeB + LC87F7J32A

■Flash ROM Programming Board

| Package | Programming boards |
|---|---|
| QIP64E(14×14) | W87F50256Q |
| TQFP64J(10×10) | W87F57256SQ |

■Flash ROM Programmer

| Maker | Model | | Supported Version (Note) | Device |
|---|---|---|---|---|
| Flash Support Group, Inc. (Formerly Ando Electric Co., Ltd.) | Single | AF9708/AF9709/ AF9709B | After 0x.xx | |
| | Gang | AF9723 (Main body) | After 0x.xx | |
| | | AF9833 (Unit) | After 0x.xx | |
| Our company | SKK (SANYO FWS) | | After x.xxA | LC87F7J32A |

Note: Please check the latest version.

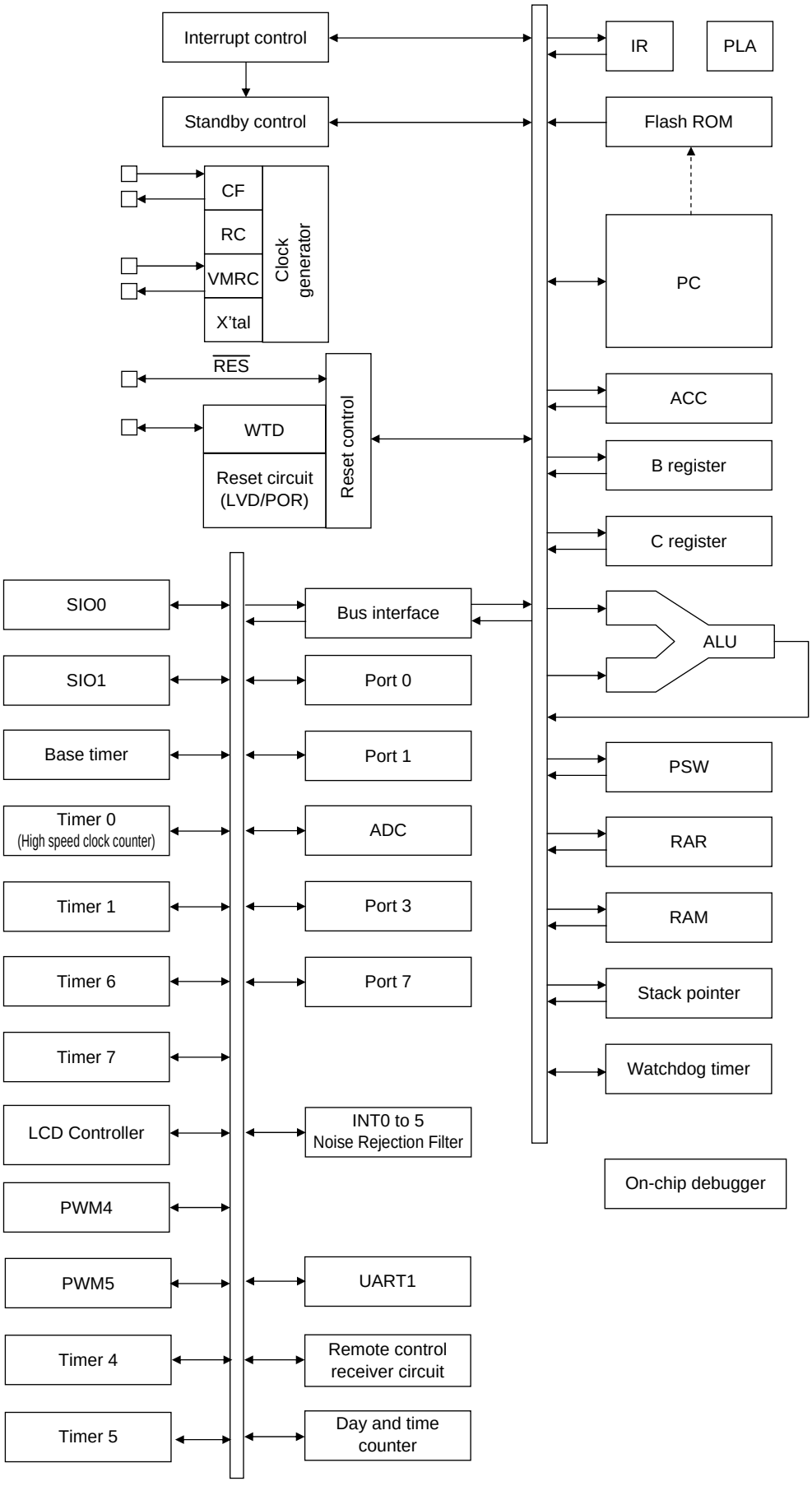
■Same Package and Pin Assignment as Mask ROM Version.

1) LC877J00 series options can be set by using flash ROM data. Thus the board used for mass production can be used for debugging and evaluation without modifications.
2) If the program for the mask ROM version is used, the usable ROM/RAM capacity is the same as the mask ROM version.

| PIN No. | NAME |
|---|---|
| 1 | P12/SCK0 |
| 2 | P13/SO1 |
| 3 | P14/SI1/SB1 |
| 4 | P15/SCK1 |
| 5 | P16/T1PWML |
| 6 | P17/T1PWMH/BUZ |
| 7 | P30/INT4/T1IN/T0LCP1/PWM4 |
| 8 | P31/INT5/T1IN/T0HCP1/PWM5 |
| 9 | $V_{DD}2$ |
| 10 | $V_{SS}2$ |
| 11 | P00/AN3 |
| 12 | P01/AN4 |
| 13 | P02/AN5 |
| 14 | P03/AN6 |
| 15 | P04/AN7 |
| 16 | P05/CKO |
| 17 | P06/T6O |
| 18 | P07/T7O |
| 19 | S0/PA0/UTX1 |
| 20 | S1/PA1/URX1 |
| 21 | S2/PA2 |
| 22 | S3/PA3 |
| 23 | S4/PA4 |
| 24 | S5/PA5 |
| 25 | S6/PA6 |
| 26 | S7/PA7 |
| 27 | S8/PB0 |
| 28 | S9/PB1 |
| 29 | S10/PB2 |
| 30 | S11/PB3 |
| 31 | S12/PB4 |
| 32 | S13/PB5 |

| PIN No. | NAME |
|---|---|
| 33 | S14/PB6 |
| 34 | S15/PB7 |
| 35 | $V_{SS}3$ |
| 36 | $V_{DD}3$ |
| 37 | S16/PC0 |
| 38 | S17/PC1 |
| 39 | S18/PC2 |
| 40 | S19/PC3 |
| 41 | S20/PC4 |
| 42 | S21/PC5 |
| 43 | S22/PC6 |
| 44 | S23/PC7 |
| 45 | COM0/PL0 |
| 46 | COM1/PL1 |
| 47 | COM2/PL2 |
| 48 | COM3/PL3 |
| 49 | P70/INT0/T0LCP/AN8 |
| 50 | P71/INT1/T0HCP/AN9 |
| 51 | P72/INT2/T0IN |
| 52 | P73/INT3/T0IN |
| 53 | $\overline{RES}$ |
| 54 | XT1/AN10 |
| 55 | XT2/AN11 |
| 56 | $V_{SS}1$ |
| 57 | CF1 |
| 58 | CF2 |
| 59 | $V_{DD}1$ |
| 60 | V1/PL4/AN0/DBGP0 |
| 61 | V2/PL5/AN1/DBGP1 |
| 62 | V3/PL6/AN2/DBGP2 |
| 63 | P10/SO0 |
| 64 | P11/SI0/SB0 |

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$<br>$V_{SS}2$<br>$V_{SS}3$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$<br>$V_{DD}2$<br>$V_{DD}3$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>PORT0<br>P00 to P07</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 4-bit units<br>• Pull-up resistors can be turned on and off in 4-bit units.<br>• Input for HOLD release<br>• Input for port 0 interrupt<br>• Shared pins<br>P00 to P04: AD converter input (AN3 to AN7)<br>P05: Clock output (system clock/can selected from sub clock)<br>P06: Timer 6 toggle output<br>P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>PORT1<br>P10 to P17</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Shared pins<br>P10: SIO0 data output<br>P11: SIO0 data input/bus I/O<br>P12: SIO0 clock I/O<br>P13: SIO1 data output<br>P14: SIO1 data input/bus I/O<br>P15: SIO1 clock I/O<br>P16: Timer 1PWML output<br>P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>PORT3<br>P30 to P31</td><td>I/O</td><td>• 2-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Shared pins<br>P30: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/PWM4<br>P31: INT5 input/HOLD release input/timer 1 event input/timer 0L capture input/PWM5<br>• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>PORT7<br>P70 to P73</td><td>I/O</td><td>• 4-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Shared pins<br>P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output<br>P71: INT1 input/HOLD release input/timer 0H capture input<br>P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/<br>high speed clock counter input<br>P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/<br>remote control receiver input<br>AD converter input ports: AN8 (P70), AN9 (P71)<br>• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
</table>

Continued on next page.

Continued from preceding page.

| Pin Name | I/O | Description | Option |
|---|---|---|---|
| S0/PA0 to S7/PA7 | I/O | • Segment output for LCD<br>• Can be used as general-purpose I/O port (PA) | No |
| S8/PB0 to S15/PB7 | I/O | • Segment output for LCD<br>• Can be used as general-purpose I/O port (PB) | No |
| S16/PC0 to S23/PC7 | I/O | • Segment output for LCD<br>• Can be used as general-purpose I/O port (PC) | No |
| COM0/PL0 to COM3/PL3 | I/O | • Common output for LCD<br>• Can be used as general-purpose input port (PL) | No |
| V1/PL4 to V3/PL7 | I/O | • LCD output bias power supply<br>• Can be used as general-purpose input port (PL)<br>• Shared pins<br>AD converter input ports: AN0 (V1) to AN2 (V3)<br>On-chip debugger pins: DBGP0 (V1) to DBGP2 (V3) | No |
| $\overline{RES}$ | Input | Reset pin | No |
| XT1 | Input | • 32.768kHz crystal oscillator input pin<br>• Shared pins<br>General-purpose input port<br>AD converter input port: AN10<br>Must be connected to $V_{DD}1$ if not to be used. | No |
| XT2 | I/O | • 32.768kHz crystal oscillator output pin<br>• Shared pins<br>General-purpose I/O port<br>AD converter input port: AN11<br>Must be set for oscillation and kept open if not to be used. | No |
| CF1 | Input | Ceramic resonator input pin | No |
| CF2 | Output | Ceramic resonator output pin | No |

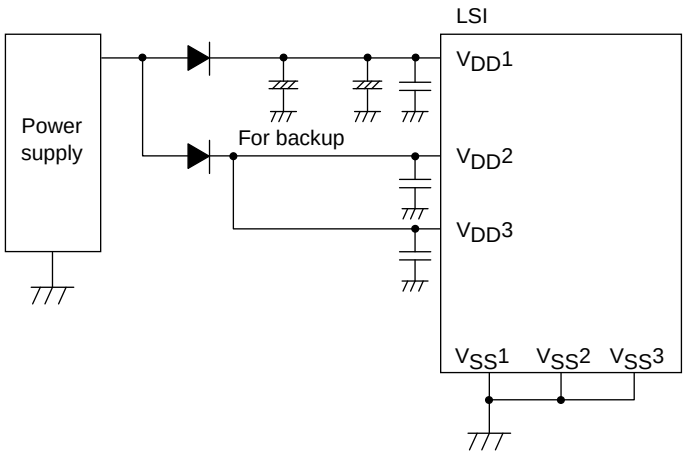
## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port Name | Option Selected in Units of | Option Type | Output Type | Pull-up Resistor |
|---|---|---|---|---|
| P00 to P07 | 1 bit | 1 | CMOS | Programmable (Note) |
| | | 2 | N-channel open drain | No |
| P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P30 to P31 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P70 | - | No | N-channel open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| S0/PA0 to S23/PC7 | - | No | CMOS | Programmable |
| COM0/PL0 to COM3/PL3 | - | No | Input only | No |
| V1/PL4 to V3/PL6 | - | No | Input only | No |
| XT1 | - | No | Input for 32.768 kHz crystal oscillator (Input only) | No |
| XT2 | - | No | Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode) | No |

Note1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

*1 Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.




*2 The internal memory is sustained by $V_{DD}1$. If none of $V_{DD}2$ and $V_{DD}3$ are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | | -0.3 | | +6.5 | V |
| supply voltage for LCD | | VLCD | V1/PL4, V2/PL5, V3/PL6 | $V_{DD}1=V_{DD}2=V_{DD}3$ | | -0.3 | | $V_{DD}$ | |
| Input voltage | | $V_I$(1) | Port L<br>XT1, CF1, $\overline{RES}$ | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$(1) | Port 0, 1, 3, 7<br>Port A, B, C<br>XT2 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1<br>Ports A, B, C | • CMOS output selected<br>• Current at each pin | | -10 | | | mA |
| | | IOPH(2) | Port 3 | • CMOS output selected<br>• Current at each pin | | -20 | | | |
| | | IOPH(3) | Port 71 to 73 | Current at each pin | | -5 | | | |
| | Mean output current (Note 1-1) | IOMH(1) | Ports 0, 1<br>Ports A, B, C | • CMOS output selected<br>• Current at each pin | | -7.5 | | | |
| | | IOMH(2) | Port 3 | • CMOS output selected<br>• Current at each pin | | -15 | | | |
| | | IOMH(3) | Ports 71 to 73 | Current at each pin | | -3 | | | |
| | Total output current | ΣIOAH(1) | Ports 71 to 73 | Total of all pins | | -5 | | | |
| | | ΣIOAH(2) | Port 1 | Total of all pins | | -20 | | | |
| | | ΣIOAH(3) | Ports 1, 71 to 73 | Total of all pins | | -20 | | | |
| | | ΣIOAH(4) | Port 3 | Total of all pins | | -25 | | | |
| | | ΣIOAH(5) | Port 0 | Total of all pins | | -20 | | | |
| | | ΣIOAH(6) | Ports 0, 3 | Total of all pins | | -40 | | | |
| | | ΣIOAH(7) | Ports A, B | Total of all pins | | -25 | | | |
| | | ΣIOAH(8) | Port C | Total of all pins | | -20 | | | |
| | | ΣIOAH(9) | Ports A, B, C | Total of all pins | | -10 | | | |
| Low level output current | Peak output current | IOPL(1) | Ports 0, 1<br>Ports A, B, C | Current at each pin | | | | 20 | |
| | | IOPL(2) | Port 3 | Current at each pin | | | | 30 | |
| | | IOPL(3) | Ports 7, XT2 | Current at each pin | | | | 10 | |
| | Mean output current (Note 1-1) | IOML(1) | Ports 0, 1<br>Ports A, B, C | Current at each pin | | | | 15 | |
| | | IOML(2) | Port 3 | Current at each pin | | | | 20 | |
| | | IOML(3) | Ports 7, XT2 | Current at each pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | Ports 7, XT2 | Total of all pins | | | | 15 | |
| | | ΣIOAL(2) | Ports 1 | Total of all pins | | | | 40 | |
| | | ΣIOAL(3) | Ports 1, 7, XT2 | Total of all pins | | | | 50 | |
| | | ΣIOAL(4) | Port 3 | Total of all pins | | | | 45 | |
| | | ΣIOAL(5) | Port 0 | Total of all pins | | | | 40 | |
| | | ΣIOAL(6) | Ports 0, 3 | Total of all pins | | | | 80 | |
| | | ΣIOAL(7) | Ports A, B | Total of all pins | | | | 45 | |
| | | ΣIOAL(8) | Port C | Total of all pins | | | | 40 | |
| | | ΣIOAL(9) | Ports A, B, C | Total of all pins | | | | 80 | |
| Power dissipation | | Pd max | QIP64E(14×14) | Ta=-40 to +85°C | | | | 298 | mW |
| | | | TQFP64J(10×10) | Ta=-40 to +85°C | | | | | |
| Operating ambient temperature | | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Allowable Operating Condtions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Operating supply voltage (Note 2-1) | $V_{DD}(1)$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | 0-237µs≤tCYC≤200µs | | 3.0 | | 5.5 | V |
| | | | 0-356µs≤tCYC≤200µs | | 2.5 | | 5.5 | |
| | | | 0-712µs≤tCYC≤200µs | | 2.2 | | 5.5 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3$ | RAM and register contents sustained in HOLD mode | | 2.0 | | 5.5 | |
| High level input voltage | $V_{IH}(1)$ | • Ports 0, 3<br>• Ports A, B, C<br>• Port L | Output disabled | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(2)$ | • Port 1<br>• Ports 71 to 73<br>• Port 70 port input/ interrupt side | • Output disabled<br>• When INT1VTSL=0 (P71only) | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(3)$ | Port 71 interrupt side | • Output disabled<br>• When INT1VTSL=1 | 2.2 to 5.5 | $0.85V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(4)$ | Port 70 watchdog timer side | Output disabled | 2.2 to 5.5 | $0.9V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(5)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.2 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | • Ports 0, 3<br>• Ports A, B, C<br>• Port L | Output disabled | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}$ +0.4 | |
| | | | | 2.2 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | VIL(2) | • Port 1<br>• Ports 71 to 73<br>• Port 70 port input/interrupt side | • Output disabled<br>• When INT1VTSL=0 (P71 only) | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}$ +0.4 | |
| | | | | 2.2 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 71 interrupt side | • Output disabled<br>• When INT1VTSL=1 | 2.2 to 5.5 | $V_{SS}$ | | $0.45V_{DD}$ | |
| | $V_{IL}(4)$ | Port 70 watchdog timer side | | 2.2 to 5.5 | $V_{SS}$ | | $0.8V_{DD}$ -1.0 | |
| | $V_{IL}(5)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.2 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-2) | tCYC | | | 3.0 to 5.5 | 0.237 | | 200 | µs |
| | | | | 2.5 to 5.5 | 0.356 | | 200 | |
| | | | | 2.2 to 5.5 | 0.712 | | 200 | |
| External system clock frequency | FEXCF(1) | CF1 | • CF2 pin open<br>• System clock frequency division ratio=1/1<br>• External system clock DUTY=50±5% | 3.0 to 5.5 | 0.1 | | 12 | MHz |
| | | | | 2.5 to 5.5 | 0.1 | | 8 | |
| | | | | 2.2 to 5.5 | 0.1 | | 4 | |
| | | | • CF2 pin open<br>• System clock frequency division ratio=1/2 | 3.0 to 5.5 | 0.2 | | 24.4 | |
| | | | | 2.5 to 5.5 | 0.2 | | 16 | |
| | | | | 2.2 to 5.5 | 0.2 | | 8 | |

Note 2-1: $V_{DD}$ must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Oscillation frequency range (Note 2-3) | FmCF(1) | CF1, CF2 | • 12MHz ceramic oscillation<br>• See figure 1. | 3.0 to 5.5 | | 12 | | MHz |
| | FmCF(2) | CF1, CF2 | • 8MHz ceramic oscillation<br>• See figure 1. | 2.5 to 5.5 | | 8 | | |
| | FmCF(3) | CF1, CF2 | • 4MHz ceramic oscillation<br>• See figure 1. | 2.2 to 5.5 | | 4 | | |
| | FmRC | | Internal RC oscillation | 2.2 to 5.5 | 0.3 | 1.0 | 2.0 | |
| | FmVMRC(1) | | • Frequency variable RC source oscillation<br>• When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=0 | 2.2 to 5.5 | | 10 | | |
| | FmVMRC(2) | | • Frequency variable RC source oscillation<br>• When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=1 | 2.2 to 5.5 | | 4 | | |
| | FsX'tal | XT1, XT2 | • 32.768kHz crystal oscillation<br>• See figure 2. | 2.2 to 5.5 | | 32.768 | | kHz |
| Frequency variable RC oscillation usable range | OpVMRC(1) | | When VMSL4M=0 | 2.2 to 5.5 | 8 | 10 | 12 | MHz |
| | OpVMRC(2) | | When VMSL4M=1 | 2.2 to 5.5 | 3.5 | 4 | 4.5 | |
| Frequency variable RC oscillation adjustment range | VmADJ(1) | | Each step of VMRAJn (Wide range) | 2.2 to 5.5 | 8 | 24 | 64 | % |
| | VmADJ(2) | | Each step of VMFAJn (Small range) | 2.2 to 5.5 | 1 | 4 | 8 | |

Note 2-3: See Tables 1 and 2 for the oscillation constants.

## **Electrical Characteristics** at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| High level input current | $I_{IH}(1)$ | • Ports 0, 1, 3, 7<br>• Ports A, B, C<br>• Port L | • Output disabled<br>• Pull-up resistor off<br>• $V_{IN}=V_{DD}$ (including output Tr's off leakage current) | 2.2 to 5.5 | | | 1 | µA |
| | $I_{IH}(2)$ | $\overline{RES}$ | $V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 1 | |
| | $I_{IH}(3)$ | XT1, XT2 | • For input port specification<br>• $V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 1 | |
| | $I_{IH}(4)$ | CF1 | $V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}(1)$ | • Ports 0, 1, 3, 7<br>• Ports A, B, C<br>• Port L | • Output disabled<br>• Pull-up resistor off<br>• $V_{IN}=V_{SS}$ (including output Tr's off leakage current) | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(2)$ | $\overline{RES}$ | $V_{IN}=V_{SS}$ | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(3)$ | XT1, XT2 | • For input port specification<br>• $V_{IN}=V_{SS}$ | 2.2 to 5.5 | -1 | | | |
| | IIL(4) | CF1 | $V_{IN}=V_{SS}$ | 2.2 to 5.5 | -15 | | | |

Continued on next page.

## Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1) | | • Continuous data transmission/reception mode<br>• See Fig. 6.<br>• (Note 4-1-2) | | 4 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected<br>• See Fig. 6. | 2.2 to 5.5 | 4/3 | | | |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| | | | tSCKHA(2) | | • Continuous data transmission/reception mode<br>• CMOS output selected<br>• See Fig. 6. | | tSCKH(2) +2tCYC | | tSCKH(2) +(10/3) tCYC | tCYC |
| Serial input | Data setup time | | tsDI(1) | SB0(P11), SI0(P11) | • Must be specified with respect to rising edge of SIOCLK<br>• See Fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(1) | | | 2.2 to 5.5 | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdDO(1) | SO0(P10), SB0(P11) | • Continuous data transmission/reception mode<br>• (Note 4-1-3) | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |
| | | | tdDO(2) | | • Synchronous 8-bit mode<br>• (Note 4-1-3) | 2.2 to 5.5 | | | 1tCYC +0.05 | |
| | Output clock | | tdDO(3) | | (Note 4-1-3) | 2.2 to 5.5 | | | (1/3)tCYC +0.15 | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig.6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected<br>• See Fig. 6. | 2.2 to 5.5 | 2 | | | |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(2) | | | 2.2 to 5.5 | 0.03 | | | |
| Serial output | Output delay time | | tdDO(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 6. | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

## Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70),<br>INT1(P71),<br>INT2(P72)<br>INT4(P30),<br>INT5(P31) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 2.2 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P73) when noise filter time constant is 1/32 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P73) when noise filter time constant is 1/128 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 256 | | | |
| | tPIH(5)<br>tPIL(5) | RMIN(P73) | Recognized by the infrared remote controller receiver circuit as a signal. | 2.2 to 5.5 | 4 | | | RMCK (Note5-1) |
| | tPIL(6) | $\overline{RES}$ | Resetting is enabled. | 2.2 to 5.5 | 200 | | | µs |

Note 5-1: Represents the period of the reference clock (1tCYC to 128tCYC or the source frequency of the subclock) for the infrared remote controller receiver circuit

## AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

**<12bits AD Converter Mode at Ta =-40 to +85°C>**

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(V1) to AN2(V3), AN3(P00) to AN7(P04), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2) | | 3.0 to 5.5 | | 12 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±16 | LSB |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 32 | | 115 | µs |
| | | | | 3.0 to 5.5 | 64 | | 115 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

**<8bits AD Converter Mode at Ta =-40 to +85°C>**

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(V1) to AN2(V3), AN3(P00) to AN7(P04), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2) | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 20 | | 90 | µs |
| | | | | 3.0 to 5.5 | 40 | | 90 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time)=((52/(division ratio)) + 2) × (1/3) ×tCYC

8bits AD Converter Mode: TCAD(Conversion time)=((32/(division ratio)) + 2) × (1/3) ×tCYC

| External oscillation (FmCF) | Operating supply voltage range (VDD) | System division ratio (SYSDIV) | Cycle time (tCYC) | AD division ratio (ADDIV) | AD conversion time (TCAD) | |
|---|---|---|---|---|---|---|
| | | | | | 12bit AD | 8bit AD |
| CF-12MHz | 4.0V to 5.5V | 1/1 | 250ns | 1/8 | 34.8µs | 21.5µs |
| | 3.0V to 5.5V | 1/1 | 250ns | 1/16 | 69.5µs | 42.8µs |
| CF-8MHz | 4.0V to 5.5V | 1/1 | 375ns | 1/8 | 52.2µs | 32.3µs |
| | 3.0V to 5.5V | 1/1 | 375ns | 1/16 | 104.3µs | 64.2µs |
| CF-4MHz | 3.0V to 5.5V | 1/1 | 750ns | 1/8 | 104.5µs | 64.5µs |

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

## Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Normal mode consumption current (Note 9-1) | IDDOP(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • FmCF=12MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 8.5 | 23 | mA |
| | IDDOP(2) | | | 3.0 to 3.6 | | 4.8 | 13 | |
| | IDDOP(3) | | • FmCF=8MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 8MHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 6.9 | 19 | |
| | IDDOP(4) | | | 3.0 to 3.6 | | 3.9 | 11 | |
| | IDDOP(5) | | | 2.5 to 3.0 | | 3.1 | 8.8 | |
| | IDDOP(6) | | • FmCF=4MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 4MHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 2.4 | 6.6 | |
| | IDDOP(7) | | | 3.0 to 3.6 | | 1.3 | 3.5 | |
| | IDDOP(8) | | | 2.2 to 3.0 | | 1.1 | 3.2 | |
| | IDDOP(9) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal RC oscillation<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 0.7 | 3.3 | |
| | IDDOP(10) | | | 3.0 to 3.6 | | 0.4 | 1.9 | |
| | IDDOP(11) | | | 2.2 to 3.0 | | 0.3 | 1.5 | |
| | IDDOP(12) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• Internal RC oscillation stopped.<br>• System clock set to 10MHz wifh frequency variable RC oscillation<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 7.8 | 21 | |
| | IDDOP(13) | | | 3.0 to 3.6 | | 4.5 | 12 | |
| | IDDOP(14) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• Internal RC oscillation stopped.<br>• System clock set to 4MHz wifh frequency variable RC oscillation<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 3.6 | 10 | |
| | IDDOP(15) | | | 3.0 to 3.6 | | 2.8 | 7.7 | |
| | IDDOP(16) | | | 2.2 to 3.0 | | 1.8 | 5.5 | |
| | IDDOP(17) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 35 | 120 | µA |
| | IDDOP(18) | | | 3.0 to 3.6 | | 18 | 72 | |
| | IDDOP(19) | | | 2.2 to 3.0 | | 13 | 53 | |
| HALT mode consumption current (Note 9-1) | IDDHALT(1) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 3.8 | 9.2 | mA |
| | IDDHALT(2) | | | 3.0 to 3.6 | | 2.0 | 5.0 | |
| | IDDHALT(3) | | • HALT mode<br>• FmCF=8MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 8MHz side<br>• Internal RC oscillation stopped.<br>• Frequency variable RC oscillation stopped.<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 2.8 | 7.7 | |
| | IDDHALT(4) | | | 3.0 to 3.6 | | 1.4 | 3.9 | |
| | IDDHALT(5) | | | 2.5 to 3.0 | | 1.1 | 3.1 | |

Note 9-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

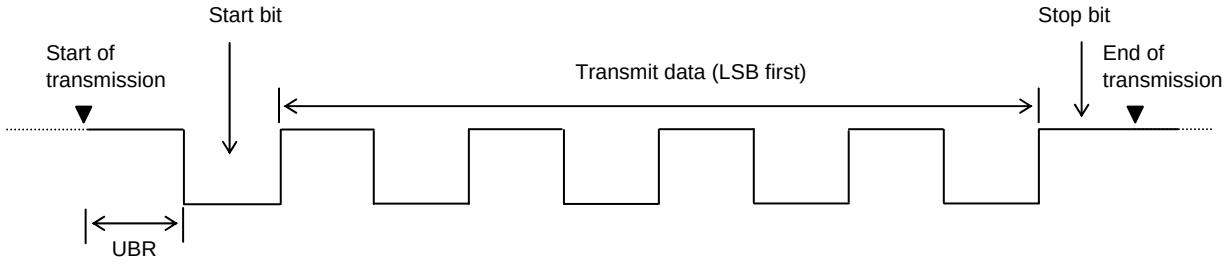
Continued on next page.

## UART (Full Duplex) Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

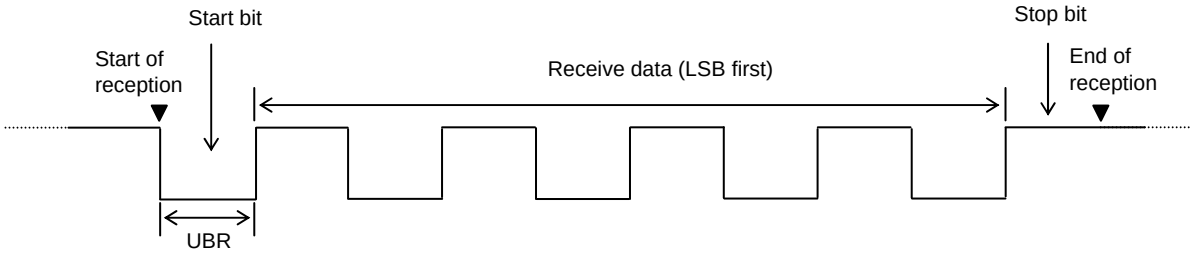
| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$[V] | min | typ | max | unit |
| Transfer ate | UBR | UTX(S0), URX(S1) | 2.2 to 5.5 | 16/3 | | 8192/3 | tCYC |

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)




Example of 8-bit Data Reception Mode Processing (Receive Data=55H)




## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rf1 [Ω] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0G52-R0 | (10) | (10) | Open | 470 | 3.0 to 5.5 | 0.05 | 0.15 | Internal C1, C2 |
| 8MHz | MURATA | CSTCE8M00G52-R0 | (10) | (10) | Open | 2.2k | 2.7 to 5.5 | 0.05 | 0.15 | Internal C1, C2 |
| | | CSTLS8M00G53-B0 | (15) | (15) | Open | 680 | 2.5 to 5.5 | 0.05 | 0.15 | |
| 4MHz | MURATA | CSTCR4M00G53-R0 | (15) | (15) | Open | 3.3k | 2.2 to 5.5 | 0.05 | 0.15 | Internal C1, C2 |
| | | CSTLS4M00G53-B0 | (15) | (15) | Open | 3.3k | 2.2 to 5.5 | 0.05 | 0.15 | |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after $V_{DD}$ goes above the operating voltage lower limit (see Figure 4).

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C3 [pF] | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | EPSON TOYOKOMU | MC-306 | 18 | 18 | Open | 560 | 2.2 to 5.5 | 1.4 | 3.0 | Applicable CL value= 12.5pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

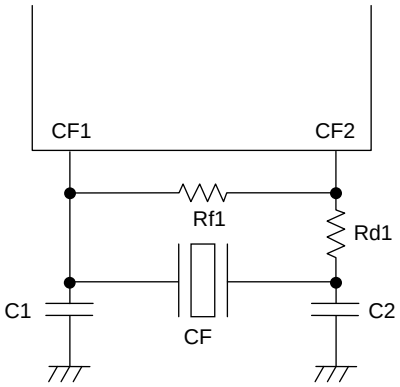



Figure 1 CF Oscillator Circuit

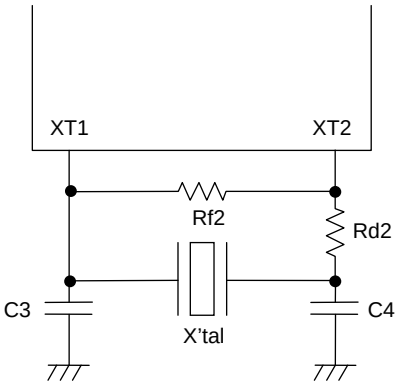



Figure 2 XT Oscillator Circuit

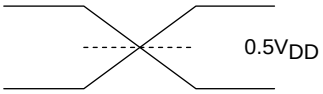
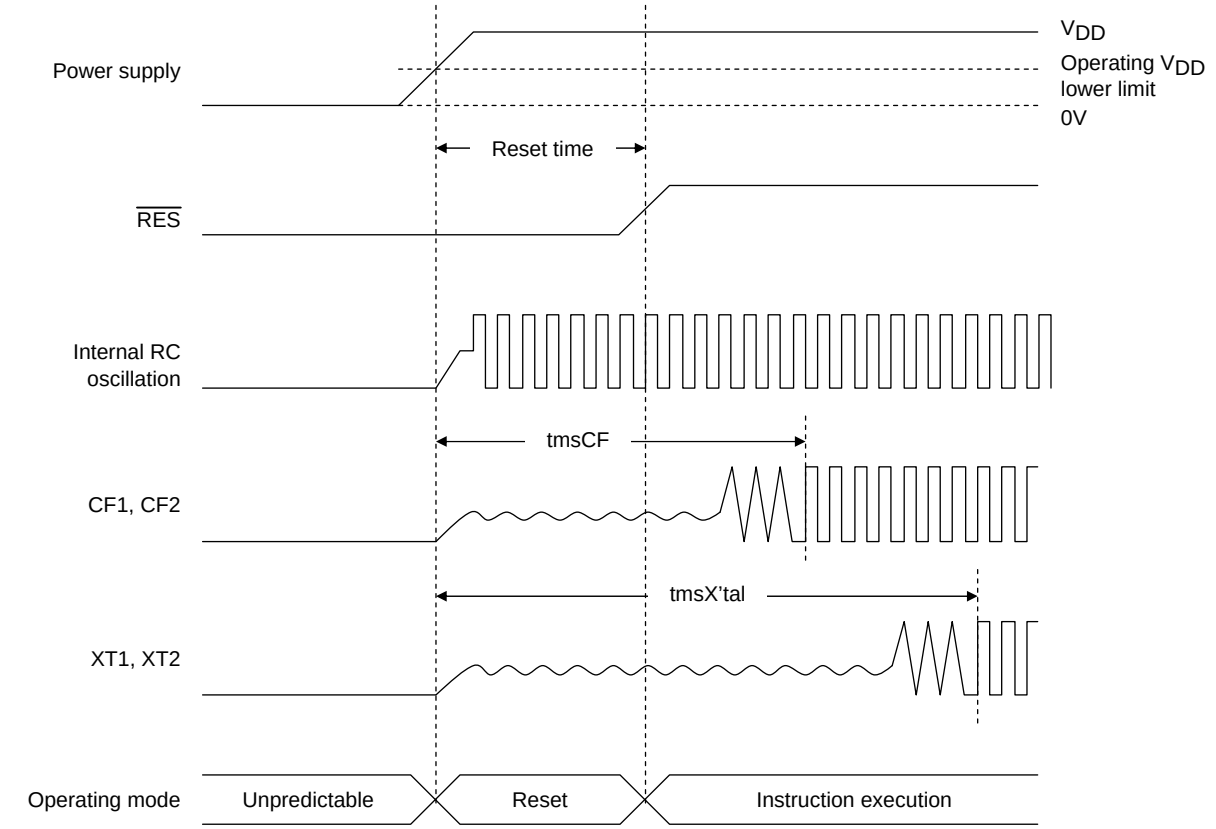
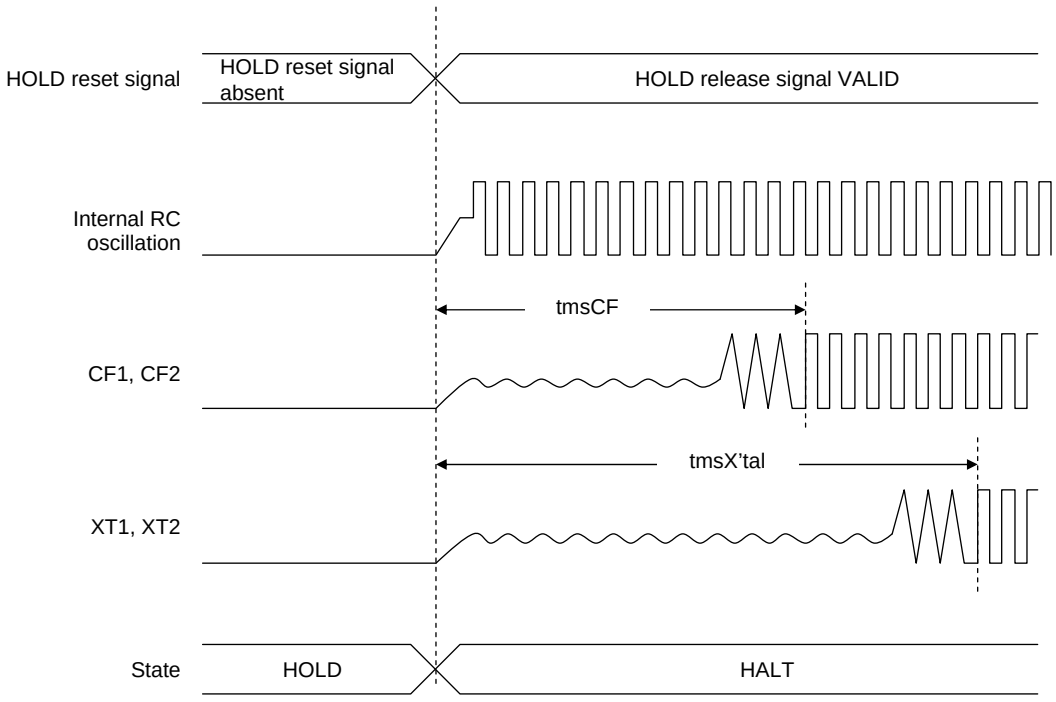



Figure 3 AC Timing Measurement Point

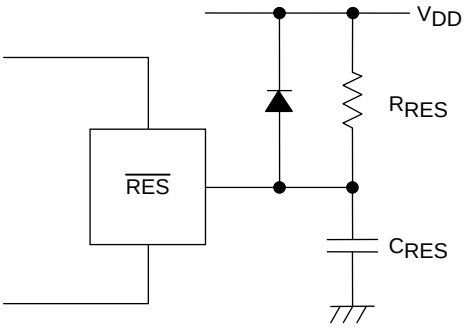



Reset Time and Oscillation Stabilization Time




HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times




Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 5 Reset Circuit

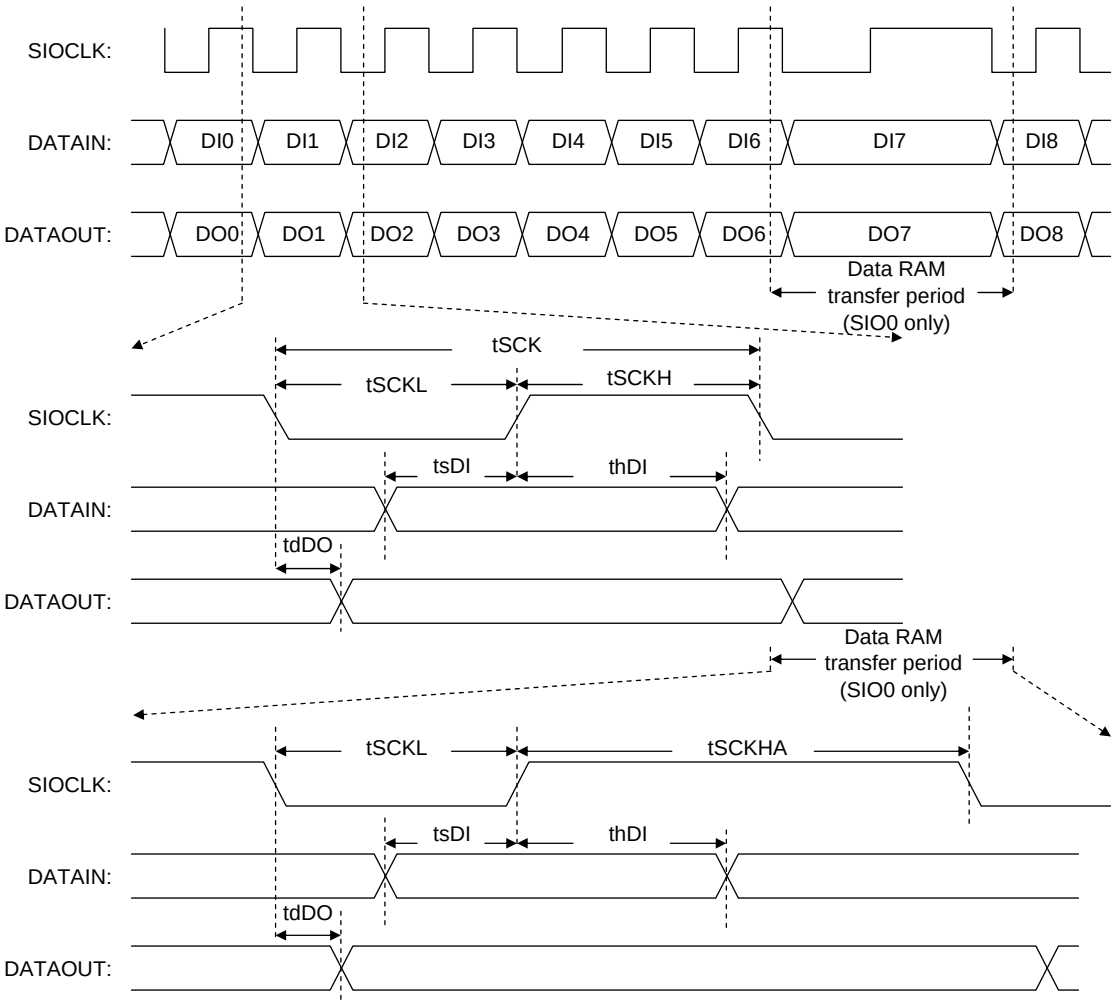



Figure 6 Serial I/O Waveforms

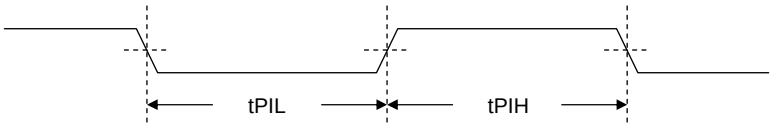



Figure 7 Pulse Input Timing Signal Waveform