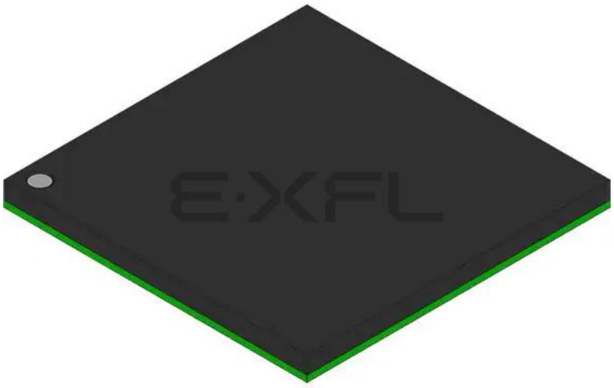

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	266MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	400kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc7116vm1000

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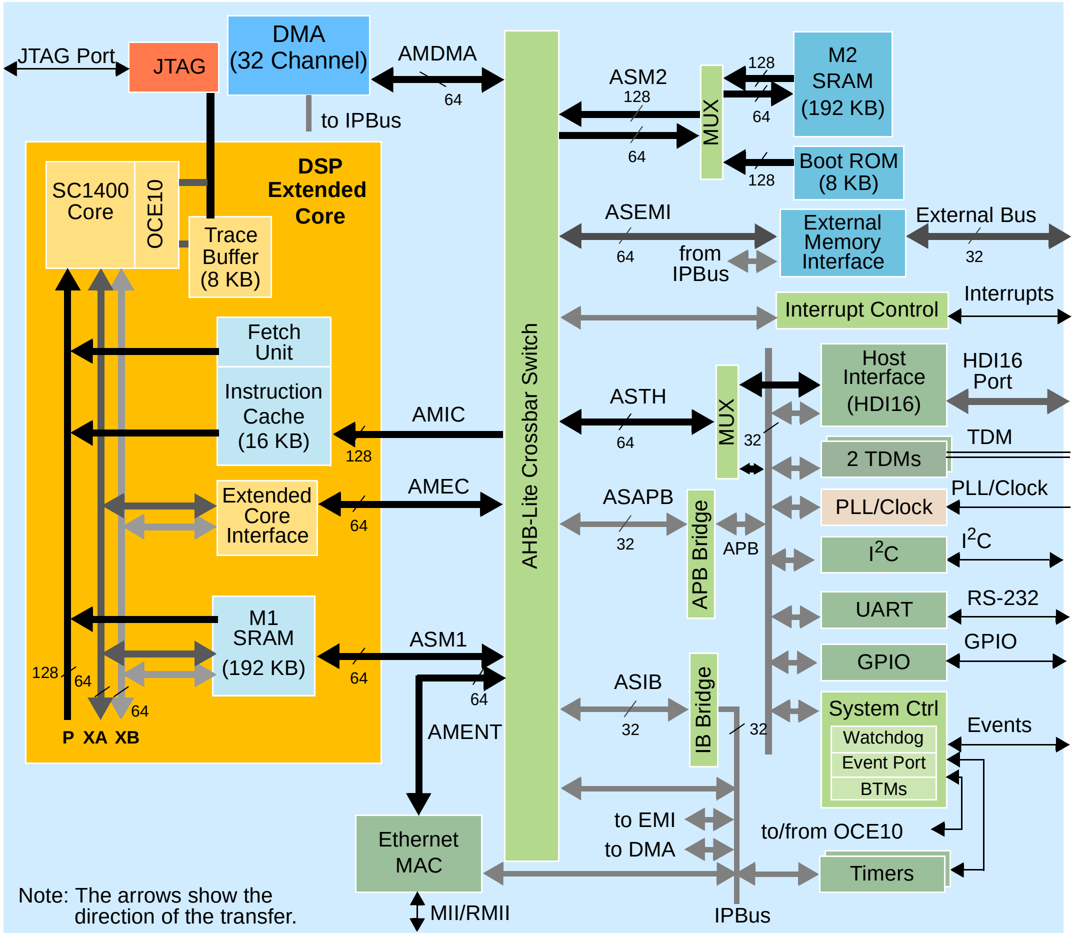

Figure 1. MSC7116 Block Diagram

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7116 Signals by Ball Designator

<table>
<tr><th rowspan="3">Number</th><th colspan="6">Signal Names</th></tr>
<tr><th rowspan="2">End of Reset</th><th colspan="3">Software Controlled</th><th colspan="2">Hardware Controlled</th></tr>
<tr><th>GPI Enabled (Default)</th><th>Interrupt Enabled</th><th>GPO Enabled</th><th>Primary</th><th>Alternate</th></tr>
<tr><td>A1</td><td colspan="6">GND</td></tr>
<tr><td>A2</td><td colspan="6">GND</td></tr>
<tr><td>A3</td><td colspan="6">DQM1</td></tr>
<tr><td>A4</td><td colspan="6">DQS2</td></tr>
<tr><td>A5</td><td colspan="6">CK</td></tr>
<tr><td>A6</td><td colspan="6">$\overline{CK}$</td></tr>
<tr><td>A7</td><td colspan="3">GPIC7</td><td>GPOC7</td><td colspan="2">HD15</td></tr>
<tr><td>A8</td><td colspan="3">GPIC4</td><td>GPOC4</td><td colspan="2">HD12</td></tr>
<tr><td>A9</td><td colspan="3">GPIC2</td><td>GPOC2</td><td colspan="2">HD10</td></tr>
<tr><td>A10</td><td colspan="4">reserved</td><td colspan="2">HD7</td></tr>
<tr><td>A11</td><td colspan="4">reserved</td><td colspan="2">HD6</td></tr>
<tr><td>A12</td><td colspan="4">reserved</td><td colspan="2">HD4</td></tr>
<tr><td>A13</td><td colspan="4">reserved</td><td colspan="2">HD1</td></tr>
<tr><td>A14</td><td colspan="4">reserved</td><td colspan="2">HD0</td></tr>
<tr><td>A15</td><td colspan="6">GND</td></tr>
<tr><td>A16</td><td>BM3</td><td colspan="2">GPID8</td><td>GPOD8</td><td colspan="2">reserved</td></tr>
<tr><td>A17</td><td colspan="6">NC</td></tr>
<tr><td>A18</td><td colspan="6">NC</td></tr>
<tr><td>A19</td><td colspan="6">NC</td></tr>
<tr><td>A20</td><td colspan="6">NC</td></tr>
<tr><td>B1</td><td colspan="6">V_{DDM}</td></tr>
<tr><td>B2</td><td colspan="6">NC</td></tr>
<tr><td>B3</td><td colspan="6">$\overline{CS0}$</td></tr>
<tr><td>B4</td><td colspan="6">DQM2</td></tr>
<tr><td>B5</td><td colspan="6">DQS3</td></tr>
<tr><td>B6</td><td colspan="6">DQS0</td></tr>
<tr><td>B7</td><td colspan="6">CKE</td></tr>
<tr><td>B8</td><td colspan="6">$\overline{WE}$</td></tr>
<tr><td>B9</td><td colspan="3">GPIC6</td><td>GPOC6</td><td colspan="2">HD14</td></tr>
<tr><td>B10</td><td colspan="3">GPIC3</td><td>GPOC3</td><td colspan="2">HD11</td></tr>
<tr><td>B11</td><td colspan="3">GPIC0</td><td>GPOC0</td><td colspan="2">HD8</td></tr>
<tr><td>B12</td><td colspan="4">reserved</td><td colspan="2">HD5</td></tr>
<tr><td>B13</td><td colspan="4">reserved</td><td colspan="2">HD2</td></tr>
</table>

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
J18	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{HACK}$/HACK or $\overline{HRRQ}$/HRRQ	
J20	HDSP	reserved			$\overline{HREQ}$/HREQ or $\overline{HTRQ}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{HDS}$/HDS or $\overline{HWR}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{PORESET}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7116 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7116.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by –2 percent).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage[1]	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage[2]	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage[3]	VTT	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	–0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	–1.0	0.09	1	µA
V_{REF} input leakage current	I_{VREF}	—	—	5	µA

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the divided input clock frequency as shown in **Table 10**.

Table 10. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
266 ≤ [Divided Input Clock × (PLLMLTF + 1)] ≤ 532 MHz	266/Divided Input Clock	532/Divided Input Clock
Note: This table results from the allowed range for F_{Loop}. The minimum and maximum multiplication factors are dependent on the frequency of the Divided Input Clock.		

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripherals depends on the value of the CLKCTRL[RNG] bit as shown in **Table 11**.

Table 11. F_{vco} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{vco}
1	266 ≤ F_{vco} ≤ 532 MHz
0	133 ≤ F_{vco} ≤ 266 MHz
Note: This table results from the allowed range for F_{vco}, which is F_{Loop} modified by CLKCTRL[RNG].	

This bit along with the CKSEL determines the frequency range of the core clock.

Table 12. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	Reserved	Reserved
11	0	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	1	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	0	4	66.5 ≤ core clock ≤ 133 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 13** summarizes this restriction.

Table 13. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100) DDR 333 (PC-2600)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7116 device has several inputs to the reset logic. All MSC7116 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7116 and configures various attributes of the MSC7116. On PORESET, the entire MSC7116 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7116. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7116 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7116 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7116 reaches at least 2/3 V_{DD}.

Table 18. DDR DRAM Output AC Timing (continued)

No.	Parameter	Symbol	Min	Max	Unit
209	Dn/DQMn output setup with respect to DQSn[3]	t_{DDKHDS}, t_{DDKLDS}	$0.25 \times t_{CK} - 750$	—	ps
210	Dn/DQMn output hold with respect to DQSn[3]	t_{DDKHDX}, t_{DDKLDX}	$0.25 \times t_{CK} - 750$	—	ps
211	DQSn preamble start[4]	t_{DDKHMP}	$-0.25 \times t_{CK}$	—	ps
212	DQSn epilogue end[5]	t_{DDKHME}	–600	600	ps

Notes:

1. All CK/$\overline{CK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
2. t_{DDKHMH} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the CK/$\overline{CK}$ crossing occurs in the middle of the control signal (An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 600 ps before the CK/$\overline{CK}$ crossing and no later than 600 ps after the crossing time; the device uses 1200 ps of the skew budget (the interval from –600 to +600 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
3. Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
4. Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from CK(r), but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
5. All outputs are referenced to the rising edge of CK. Note that this is essentially the CK/DQSn skew in spec 208. In addition there is no real "maximum" time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write-to-read turn-around times. This is already guaranteed by the memory controller operation.

Figure 6 shows the DDR DRAM output timing diagram.

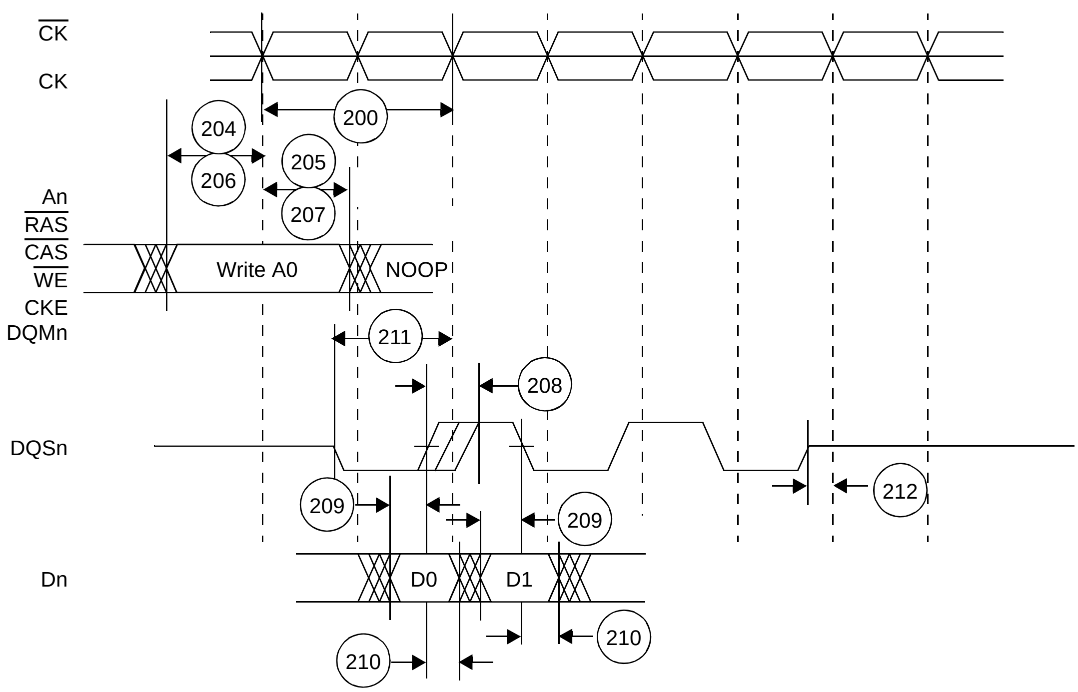

Figure 6. DDR DRAM Output Timing Diagram

2.5.6.2 Transmit Signal Timing

Table 22. Transmit Signal Timing

No.	Characteristics	Min	Max	Unit
800	Transmit clock period: • MII: TXCLK • RMII: REFCLK	 40 20	 — —	 ns ns
801	Transmit clock pulse width high—as a percent of clock period • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
802	Transmit clock pulse width low—as a percent of clock period: • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
805	Transmit clock to TXDn, TX_EN, TX_ER invalid	4	—	ns
806	Transmit clock to TXDn, TX_EN, TX_ER valid	—	14	ns

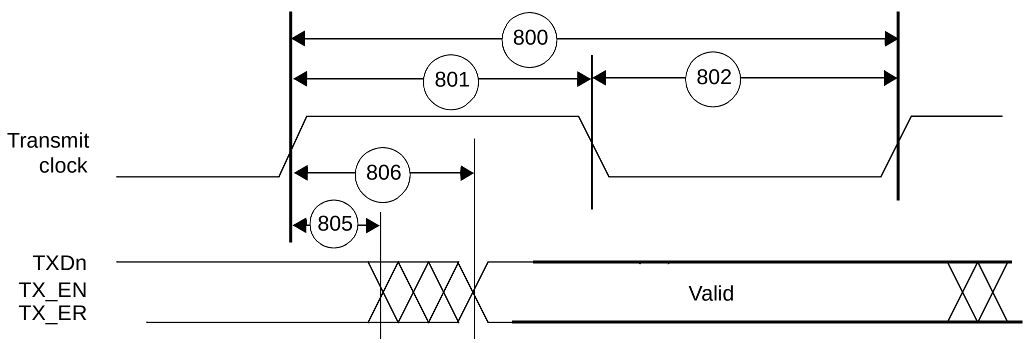

Figure 11. Ethernet Receive Signal Timing

2.5.6.3 Asynchronous Input Signal Timing

Table 23. Asynchronous Input Signal Timing

No.	Characteristics	Min	Max	Unit
807	• MII: CRS and COL minimum pulse width (1.5 × TXCLK period) • RMII: CRS_DV minimum pulse width (1.5 x REFCLK period)	60 30	— —	ns ns

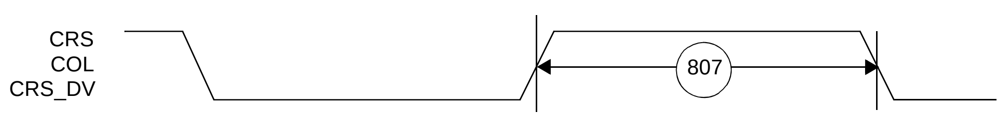

Figure 12. Asynchronous Input Signal Timing

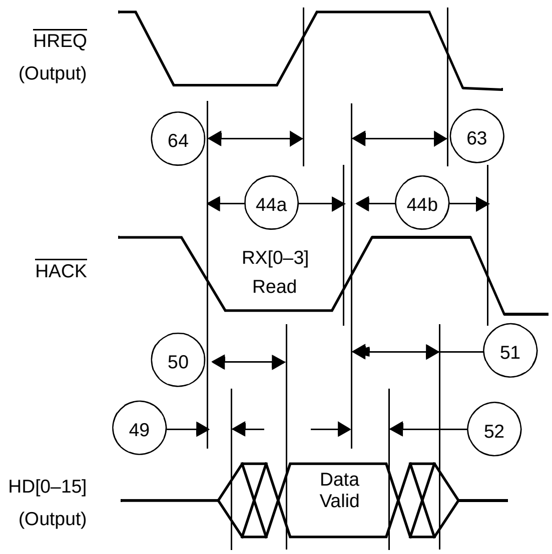

Figure 18. Host DMA Read Timing Diagram, HPCR[OAD] = 0

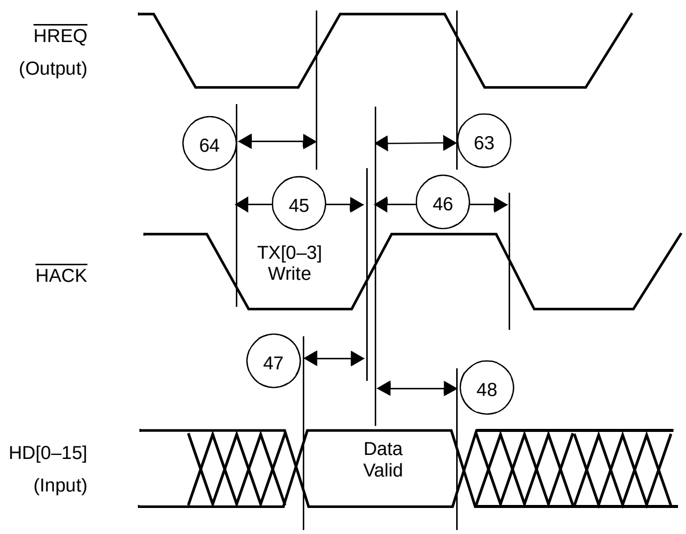

Figure 19. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.13 JTAG Signals

Table 31. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 3$)) **Note:** T_C = 1/CLOCK which is the period of the core clock. The TCK frequency must less than 1/3 of the core frequency with an absolute maximum limit of 40 MHz.	0.0	40.0	MHz
701	TCK cycle time	25.0	—	ns
702	TCK clock pulse width measured at V_{M} = 1.6 V	11.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	14.0	—	ns
706	TCK low to output data valid	0.0	20.0	ns
707	TCK low to output high impedance	0.0	20.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	14.0	—	ns
710	TCK low to TDO data valid	0.0	24.0	ns
711	TCK low to TDO high impedance	0.0	10.0	ns
712	$\overline{TRST}$ assert time	100.0	—	ns
Note:	All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface.			

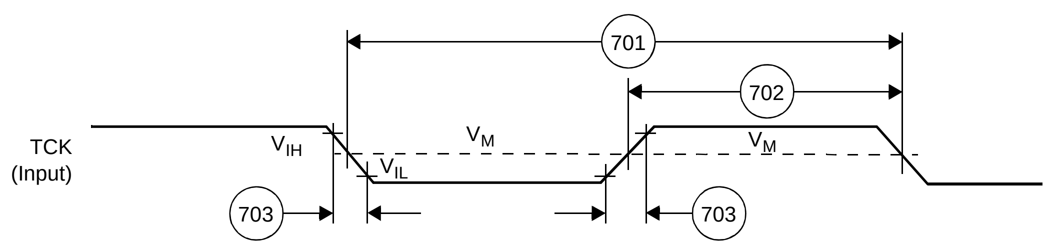

Figure 26. Test Clock Input Timing Diagram

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7116 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 1}$$

where
T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7116 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 2}$$

where
T_T = thermocouple (or infrared) temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 1.

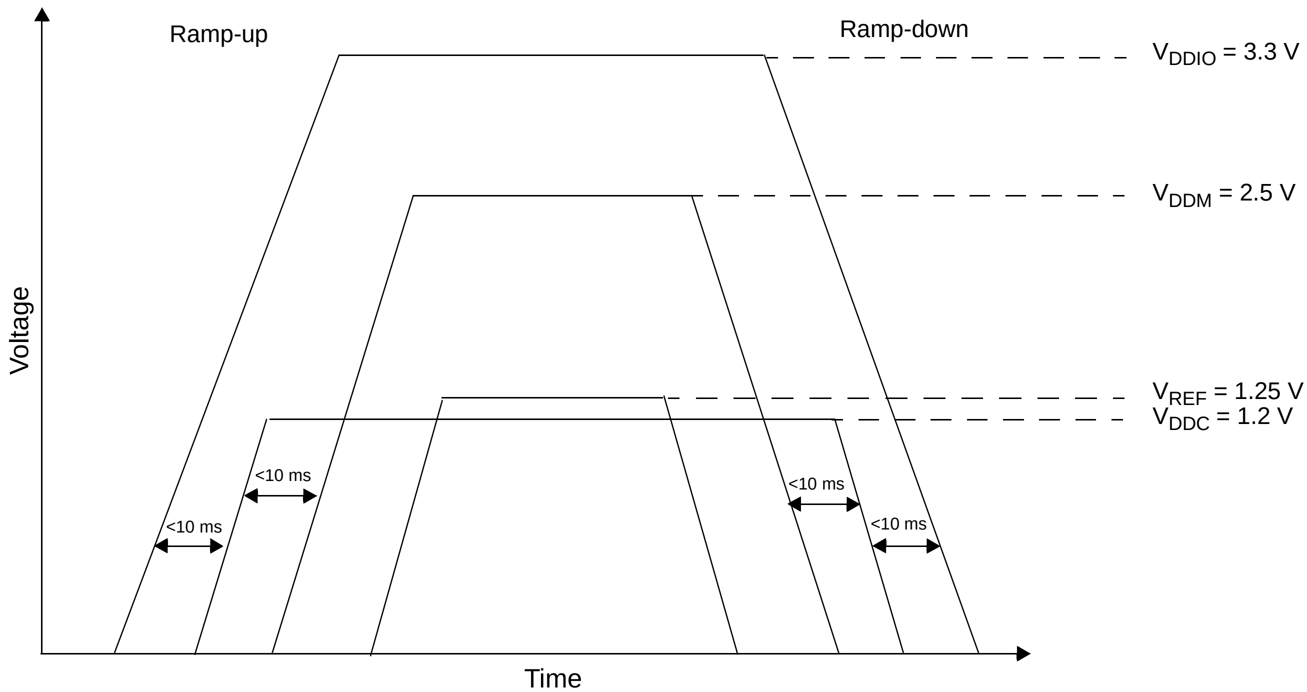

Figure 30. Voltage Sequencing Case 1

3.3.2 Peripheral Power

Peripherals include the DDR memory controller, Ethernet controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the I^2C module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 133 MHz. This yields:

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 133\ MHz \times 10^{-3} = 3.83\ mW\ per\ peripheral \qquad \text{Eqn. 6}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption.

3.3.3 External Memory Power

Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC7116 device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. The dynamic power is computed, however, using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$P_{DDRIO} = P_{STATIC} + P_{DYNAMIC} \qquad \text{Eqn. 7}$$

$$P_{STATIC} = (unused\ pins \times \%\ driven\ high) \times 16\ mA \times 2.5\ V \qquad \text{Eqn. 8}$$

$$P_{DYNAMIC} = (pin\ activity\ value) \times 20\ pF \times (0.4\ V)^2 \times 266\ MHz \times 10^{-3}\ mW \qquad \text{Eqn. 9}$$

$$pin\ activity\ value = (active\ data\ lines \times \%\ activity \times \%\ data\ switching) + (active\ address\ lines \times \%\ activity) \qquad \text{Eqn. 10}$$

As an example, assume the following:

unused pins = 16 (DDR uses 16-pin mode)
% driven high = 50%
active data lines = 16
% activity = 60%
% data switching = 50%
active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 266 \times 10^{-3}) = 326.3\ mW \qquad \text{Eqn. 11}$$

3.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 33 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 33\ MHz \times 10^{-3} = 7.19\ mW\ per\ I/O\ line \qquad \text{Eqn. 12}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

3.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

3.5 DDR Memory System Guidelines

MSC7116 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in Figure 36. Technique B is the most popular termination technique.

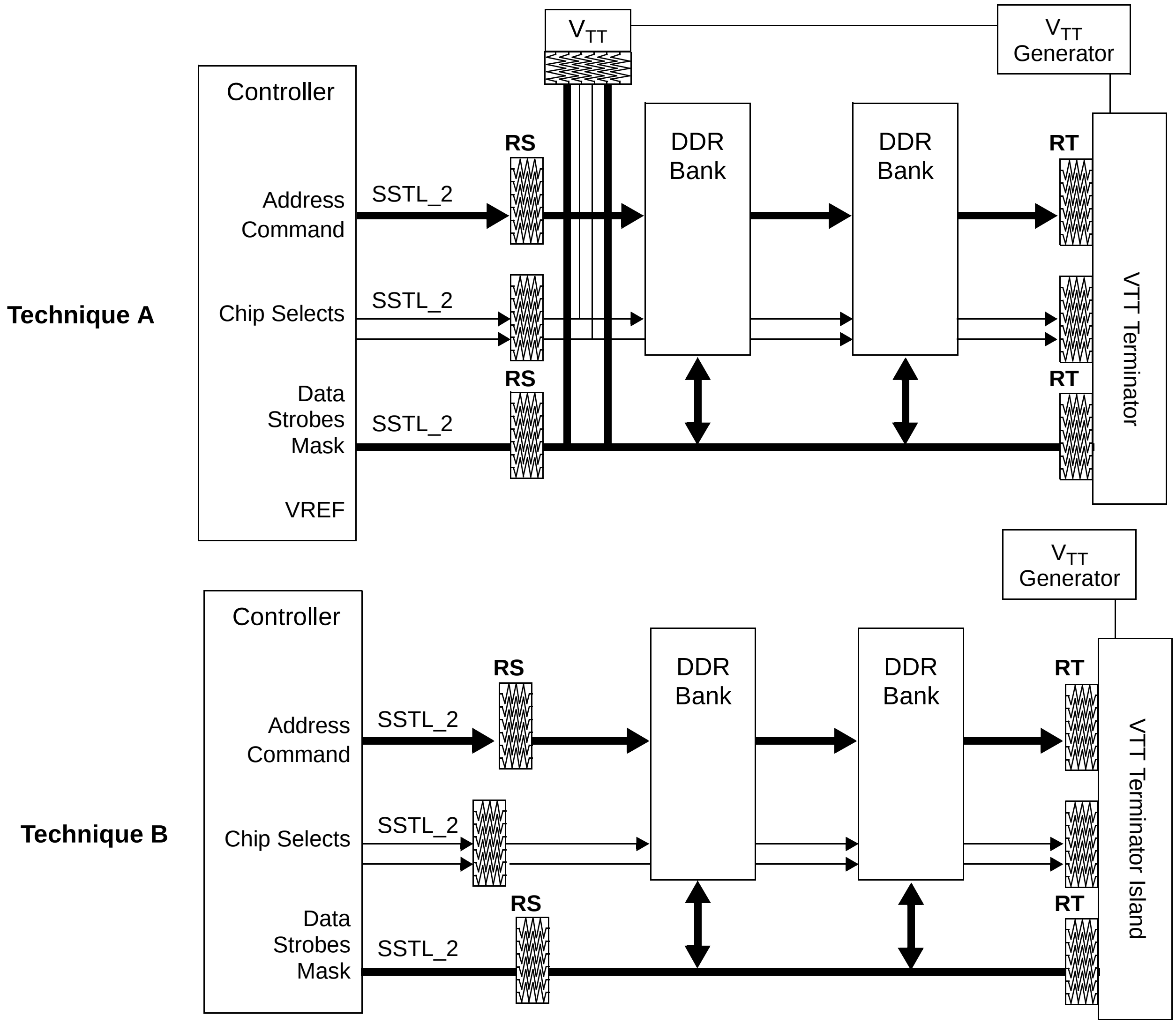

Figure 36. SSTL Termination Techniques

Figure 37 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7116 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals*.
  - SWTE is used to configure the MSC7116 device and is sampled on the deassertion of PORESET, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until PORESET is deasserted. After PORESET, this signal can be left floating.
  - BM[0–1] configure the MSC7116 device and are sampled until PORESET is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - HRESET should be pulled up.
- *Interrupt signals*. When used, IRQ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the HREQ/HREQ or HTRQ/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the HRESET signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *Ethernet MAC/TDM2 signals*. The MDIO signal requires an external pull-up resistor.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- Other signals.
  - The TEST0 pin must be connected to ground.
  - The TPSEL pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7116	1.2 V core 2.5 V memory 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	266	Lead-free	MSC7116VM1000
					Lead-bearing	MSC7116VF1000

7 Revision History

Table 36 provides a revision history for this data sheet.

Table 36. Document Revision History

Revision	Date	Description
0	Apr 2004	• Initial public release.
1	May 2004	• Added ordering information and new package options.
2	Aug. 2004	• Updated clock parameter values. • Updated DDR timing specifications. • Updated I^2C timing specifications.
3	Sep. 2004	• Updated **Figures 1-2** and **1-2** to correct HDSP and DBREQ. • Corrected EE0 port reference. • Updated ball location for HDSP.
4	Jan. 2005	• Added signal HA3. • Updated absolute maximum ratings, DDR DRAM capacitance specifications, clock parameters, reset timing, and TDM timing. • Added note for timing reference for I^2C interface. • Expanded GPIO timing information. • Corrected pin T20 and K20 signal designation. • Corrected signal names to GPAO15 and $\overline{IRQ2}$. • Expanded design guidelines in Chapter 4.
5	Mar. 2005	• Updated features list. • Updated power specifications. • Changed CLKIN frequency range. • Added clock configuration information. • Updated JTAG timings.
6	Apr. 2005	• Added recommended power supply ratings and updated equations to estimate power consumption.
7	Oct. 2005	• Updated core and total power consumption examples.
8	Dec. 2005	• Added information about the new mask set 1M88B. Affected all sections.
9	Nov. 2006	• Updated arrows in Host DMA Writing Timing figure. • Updated boot overview in **Section 4.4.3**.
10	Apr. 2007	• Removed erroneous references to V_{CCSYN} and V_{CCSYN1}.
11	Jul. 2007	• Updated to new data sheet format. Reorganized and renumbered sections, figures, and tables. • Removed all references to obsolete mask set 1L44X and corresponding specification values. • Added a note to clarify the definition of TCK timing 700 in new **Table 31**. • Reworked reset and boot sections. • Expanded I^2C boot information and added SPI boot information. • Removed obsolete part numbers.
12	Aug 2007	• The power-up and power-down sequences described in **Section 3.2** starting on page 42 have been expanded to five possible design scenarios/cases. These cases replace the previously recommended power-up/power-down sequence recommendations. **Section 3.2** has been clarified by adding subsection headings.
13	Apr 2008	• Change the PLL filter resistor from 20 Ω to 2 Ω in **Section 3.2.5**.