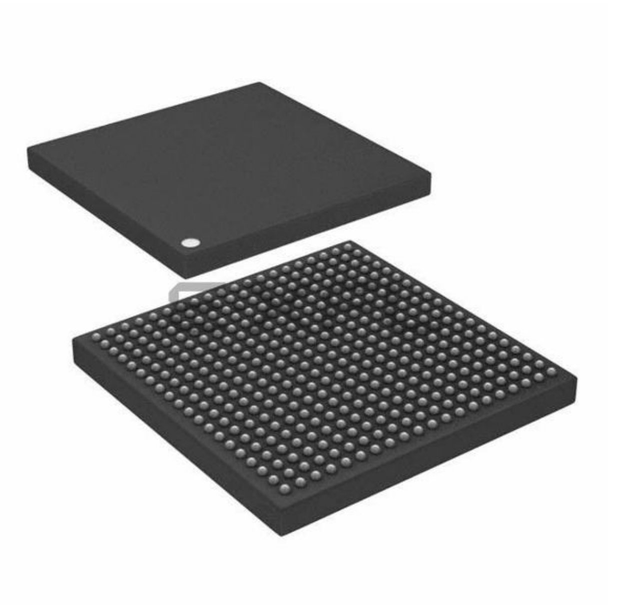

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC1400 Core
Interface	Host Interface, I²C, UART
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	400kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7116vm800

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1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7116 Signals by Ball Designator

<table>
<tr><th rowspan="3">Number</th><th colspan="6">Signal Names</th></tr>
<tr><th rowspan="2">End of Reset</th><th colspan="3">Software Controlled</th><th colspan="2">Hardware Controlled</th></tr>
<tr><th>GPI Enabled (Default)</th><th>Interrupt Enabled</th><th>GPO Enabled</th><th>Primary</th><th>Alternate</th></tr>
<tr><td>A1</td><td colspan="6">GND</td></tr>
<tr><td>A2</td><td colspan="6">GND</td></tr>
<tr><td>A3</td><td colspan="6">DQM1</td></tr>
<tr><td>A4</td><td colspan="6">DQS2</td></tr>
<tr><td>A5</td><td colspan="6">CK</td></tr>
<tr><td>A6</td><td colspan="6">$\overline{CK}$</td></tr>
<tr><td>A7</td><td colspan="3">GPIC7</td><td>GPOC7</td><td colspan="2">HD15</td></tr>
<tr><td>A8</td><td colspan="3">GPIC4</td><td>GPOC4</td><td colspan="2">HD12</td></tr>
<tr><td>A9</td><td colspan="3">GPIC2</td><td>GPOC2</td><td colspan="2">HD10</td></tr>
<tr><td>A10</td><td colspan="4">reserved</td><td colspan="2">HD7</td></tr>
<tr><td>A11</td><td colspan="4">reserved</td><td colspan="2">HD6</td></tr>
<tr><td>A12</td><td colspan="4">reserved</td><td colspan="2">HD4</td></tr>
<tr><td>A13</td><td colspan="4">reserved</td><td colspan="2">HD1</td></tr>
<tr><td>A14</td><td colspan="4">reserved</td><td colspan="2">HD0</td></tr>
<tr><td>A15</td><td colspan="6">GND</td></tr>
<tr><td>A16</td><td>BM3</td><td colspan="2">GPID8</td><td>GPOD8</td><td colspan="2">reserved</td></tr>
<tr><td>A17</td><td colspan="6">NC</td></tr>
<tr><td>A18</td><td colspan="6">NC</td></tr>
<tr><td>A19</td><td colspan="6">NC</td></tr>
<tr><td>A20</td><td colspan="6">NC</td></tr>
<tr><td>B1</td><td colspan="6">V_{DDM}</td></tr>
<tr><td>B2</td><td colspan="6">NC</td></tr>
<tr><td>B3</td><td colspan="6">$\overline{CS0}$</td></tr>
<tr><td>B4</td><td colspan="6">DQM2</td></tr>
<tr><td>B5</td><td colspan="6">DQS3</td></tr>
<tr><td>B6</td><td colspan="6">DQS0</td></tr>
<tr><td>B7</td><td colspan="6">CKE</td></tr>
<tr><td>B8</td><td colspan="6">$\overline{WE}$</td></tr>
<tr><td>B9</td><td colspan="3">GPIC6</td><td>GPOC6</td><td colspan="2">HD14</td></tr>
<tr><td>B10</td><td colspan="3">GPIC3</td><td>GPOC3</td><td colspan="2">HD11</td></tr>
<tr><td>B11</td><td colspan="3">GPIC0</td><td>GPOC0</td><td colspan="2">HD8</td></tr>
<tr><td>B12</td><td colspan="4">reserved</td><td colspan="2">HD5</td></tr>
<tr><td>B13</td><td colspan="4">reserved</td><td colspan="2">HD2</td></tr>
</table>

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{PORESET}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					

Table 1. MSC7116 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
V18	GPIA24		$\overline{IRQ24}$	GPOA24	TX_EN	
V19	reserved				CRS	
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{IRQ13}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{IRQ5}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{IRQ7}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{IRQ8}$	GPOA3	T1RD	
W14	GPIA1		$\overline{IRQ10}$	GPOA1	T1TFS	
W15	GPID4			GPOD4	TXD2	reserved
W16	GPIA27		$\overline{IRQ18}$	GPOA27	RXD3	reserved
W17	GPIA19		$\overline{IRQ19}$	GPOA19	TXD1	
W18	GPIA23		$\overline{IRQ23}$	GPOA23	TXCLK or REFCLK	
W19	GPIA26		$\overline{IRQ26}$	GPOA26	RX_ER	
W20	H8BIT	reserved			MDC	
Y1	V_{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{NMI}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{IRQ4}$	GPOA11	T0RCK	
Y11	GPIA9			GPOA9	T0RD	
Y12	GPIA6			GPOA6	T0TD	
Y13	GPIA5		$\overline{IRQ0}$	GPOA5	T1RCK	

Table 5. DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, V_{IL} = 0.4 V	I_L	–1.0	0.09	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	–1.0	0.09	1	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 5 mA	V_{OL}	—	0	0.4	V
Typical power at 266 MHz[5]	P	—	293.0	—	mW

Notes:
1. The value of V_{DDM} at the MSC7116 device must remain within 50 mV of V_{DDM} at the DRAM device at all times.
2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the MSC7116 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}.
4. Output leakage for the memory interface is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ V_{DDM}.
5. The core power values were measured.using a standard EFR pattern at typical conditions (25°C, 300 MHz, 1.2 V core).

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF

Note: These values were measured under the following conditions:
- V_{DDM} = 2.5 V ± 0.125 V
- f = 1 MHz
- T_A = 25°C
- $V_{OUT} = V_{DDM}/2$
- V_{OUT} (peak to peak) = 0.2 V

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7116 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- *PLLDVF field*. Specifies the PLL division factor (PLLDVF + 1) to divide the input clock frequency F_{CLKIN}. The output of the divider block is the input to the multiplier block.
- *PLLMLTF field*. Specifies the PLL multiplication factor (PLLMLTF + 1). The output from the multiplier block is the loop frequency F_{LOOP}.
- *RNG field*. Selects the available PLL frequency range for F_{VCO}, either F_{LOOP} when the RNG bit is set (1) or $F_{LOOP}/2$ when the RNG bit is cleared (0).
- *CKSEL field*. Selects F_{CLKIN}, F_{VCO}, or $F_{VCO}/2$ as the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10–25 MHz.
- The output frequency of the PLL multiplier must be in the range 266–532 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Input Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 9**.

Table 9. CLKIN Frequency Ranges by Divide Factor Value

PLLDVF Field Value	Input Divide Factor	CLKIN Frequency Range	Comments
0x00	1	10 to 25 MHz	Input Division by 1
0x01	2	20 to 50 MHz	Input Division by 2
0x02	3	30 to 75 MHz	Input Division by 3
0x03	4	40 to 100 MHz	Input Division by 4
0x04	5	50 to 100 MHz	Input Division by 5
0x05	6	60 to 100 MHz	Input Division by 6
0x06	7	70 to 100 MHz	Input Division by 7
0x07	8	80 to 100 MHz	Input Division by 8
0x08	9	90 to 100 MHz	Input Division by 9
0x09	10	100 MHz	Input Division by 10
Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–10.			

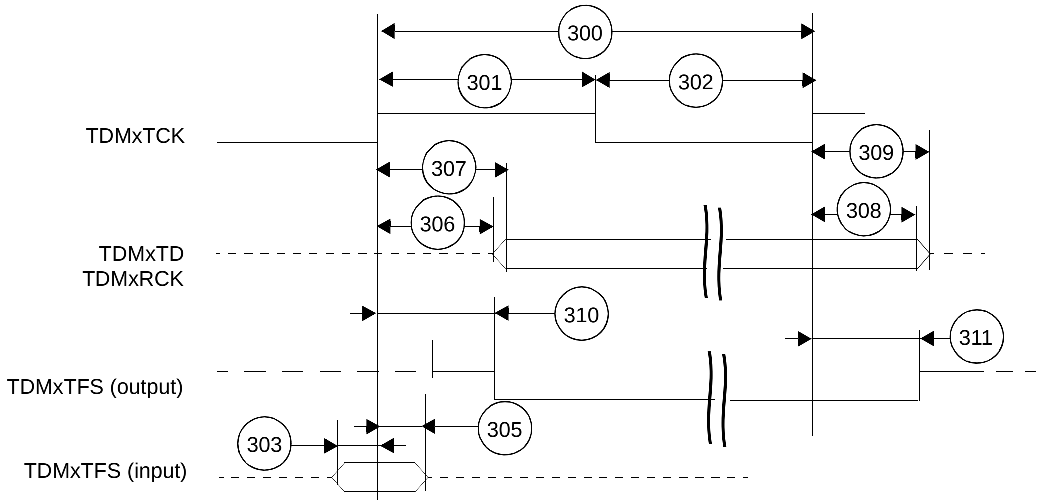

Figure 9. TDM Transmit Signals

2.5.6 Ethernet Timing

2.5.6.1 Receive Signal Timing

Table 21. Receive Signal Timing

No.	Characteristics	Min	Max	Unit
800	Receive clock period: • MII: RXCLK (max frequency = 25 MHz) • RMII: REFCLK (max frequency = 50 MHz)	 40 20	 — —	 ns ns
801	Receive clock pulse width high—as a percent of clock period • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
802	Receive clock pulse width low—as a percent of clock period: • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
803	RXDn, RX_DV, CRS_DV, RX_ER to receive clock rising edge setup time	4	—	ns
804	Receive clock rising edge to RXDn, RX_DV, CRS_DV, RX_ER hold time	2	—	ns

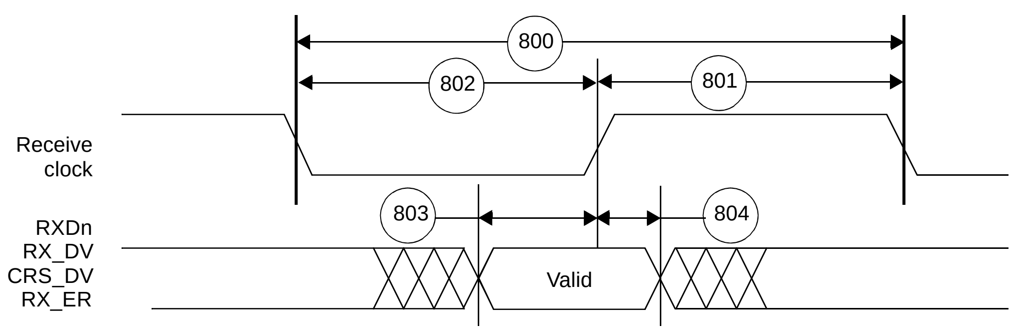

Figure 10. Ethernet Receive Signal Timing

2.5.6.2 Transmit Signal Timing

Table 22. Transmit Signal Timing

No.	Characteristics	Min	Max	Unit
800	Transmit clock period: • MII: TXCLK • RMII: REFCLK	 40 20	 — —	 ns ns
801	Transmit clock pulse width high—as a percent of clock period • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
802	Transmit clock pulse width low—as a percent of clock period: • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
805	Transmit clock to TXDn, TX_EN, TX_ER invalid	4	—	ns
806	Transmit clock to TXDn, TX_EN, TX_ER valid	—	14	ns

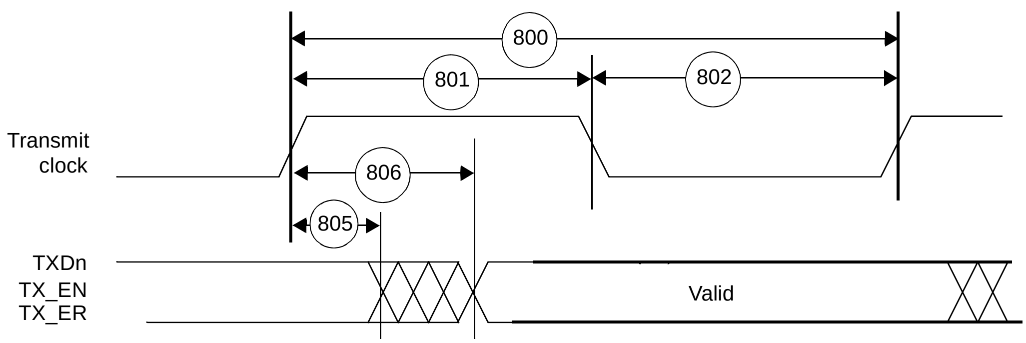

Figure 11. Ethernet Receive Signal Timing

2.5.6.3 Asynchronous Input Signal Timing

Table 23. Asynchronous Input Signal Timing

No.	Characteristics	Min	Max	Unit
807	• MII: CRS and COL minimum pulse width (1.5 × TXCLK period) • RMII: CRS_DV minimum pulse width (1.5 x REFCLK period)	60 30	— —	ns ns

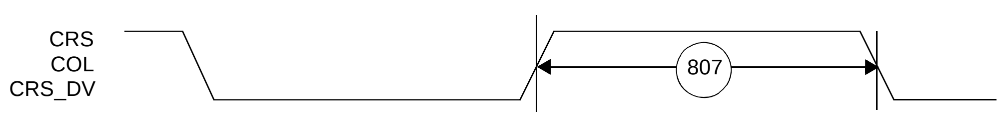

Figure 12. Asynchronous Input Signal Timing

2.5.11 Event Timing

Table 29. EVNT Signal Timing

Number	Characteristics	Type	Min
67	EVNT as input	Asynchronous	1.5 × APBCLK periods
68	EVNT as output	Synchronous to core clock	1 APBCLK period
Notes:	**1.** Refer to **Table 27** for a definition of the APBCLK period. **2.** Direction of the EVNT signal is configured through the GPIO and Event port registers. **3.** Refer to the signal chapter in the *MSC711x Reference Manual* for details on EVNT pin functionality.		

Figure 24 shows the signal behavior of the EVNT pins.

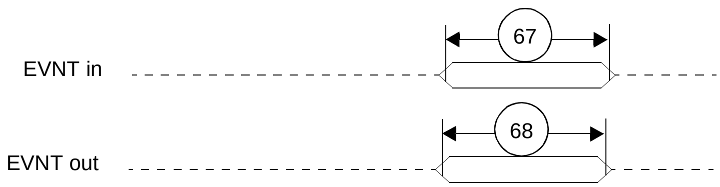

Figure 24. EVNT Pin Timing

2.5.12 GPIO Timing

Table 30. GPIO Signal Timing[1,2,3]

Number	Characteristics	Type	Min
601	GPI[4,5]	Asynchronous	1.5 × APBCLK periods
602	GPO[5]	Synchronous to core clock	1 APBCLK period
603	Port A edge-sensitive interrupt	Asynchronous	1.5 × APBCLK periods
604	Port A level-sensitive interrupt	Asynchronous	3 × APBCLK periods[6]
Notes:	**1.** Refer to **Table 27** for a definition of the APBCLK period. **2.** Direction of the GPIO signal is configured through the GPIO port registers. **3.** Refer to **Section 1.5** for details on GPIO pin functionality. **4.** GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPADR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design. **5.** The output signals cannot toggle faster than 75 MHz. **6.** Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.		

Figure 25 shows the signal behavior of the GPI/GPO pins.

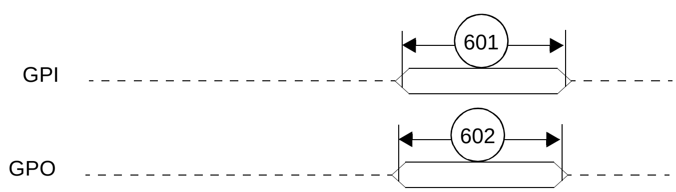

Figure 25. GPI/GPO Pin Timing

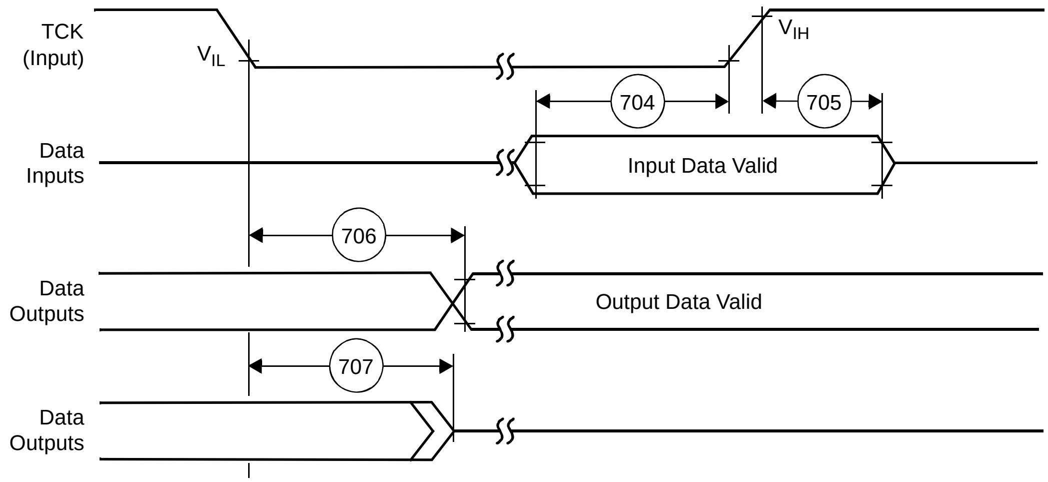

Figure 27. Boundary Scan (JTAG) Timing Diagram

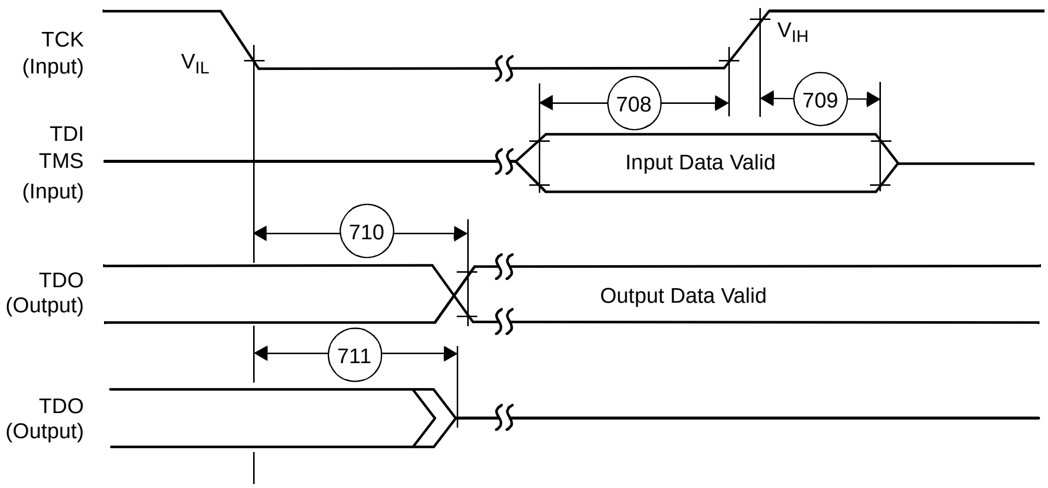

Figure 28. Test Access Port Timing Diagram

Figure 29. $\overline{\text{TRST}}$ Timing Diagram

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7116 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7116 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.2 Power Supply Design Considerations

This section outlines the MSC7116 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7116 requires four input voltages, as shown in **Table 32**.

Table 32. MSC7116 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7116 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 1.

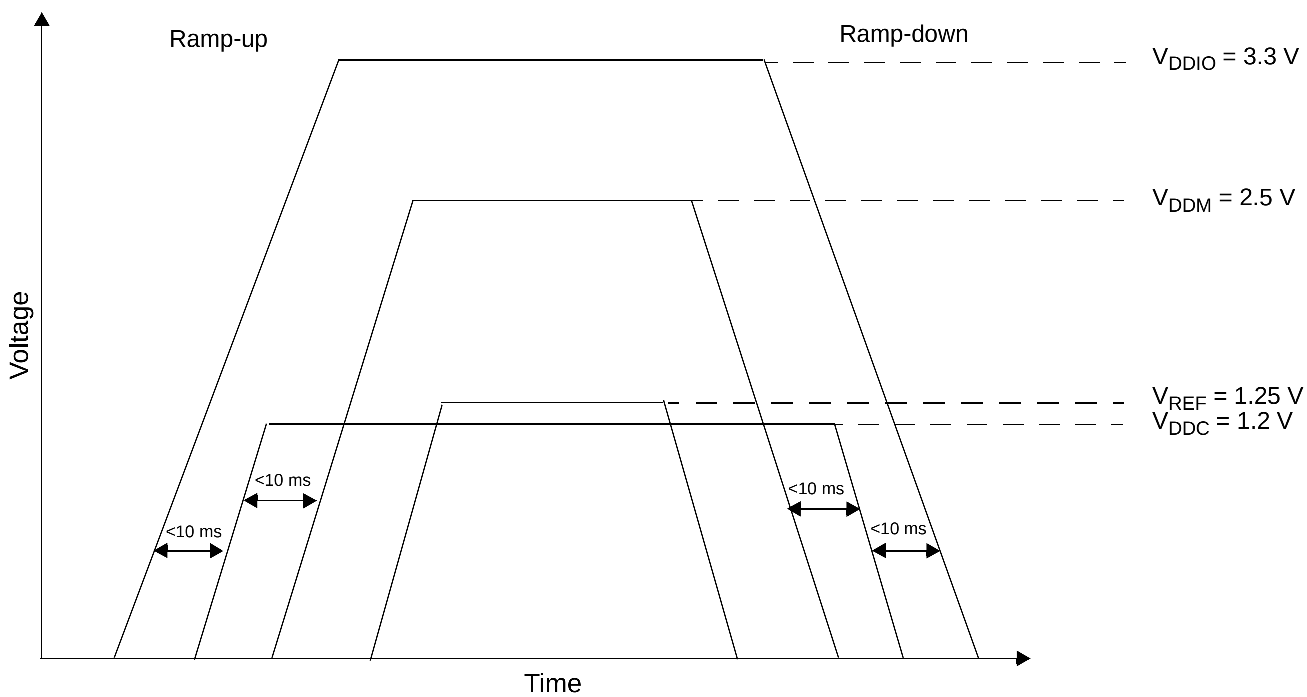

Figure 30. Voltage Sequencing Case 1

3.2.2.4 Case 4

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V), V_{DDM} (2.5 V), and V_{REF} (1.25 V) supplies simultaneously (second).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDC} (1.2 V), V_{REF} (1.25 V), and V_{DDM} (2.5 V) supplies simultaneously (first).
2. Turn of the V_{DDIO} (3.3 V) supply last.

Use the following guidelines:

- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 33** for relative timing for Case 4.

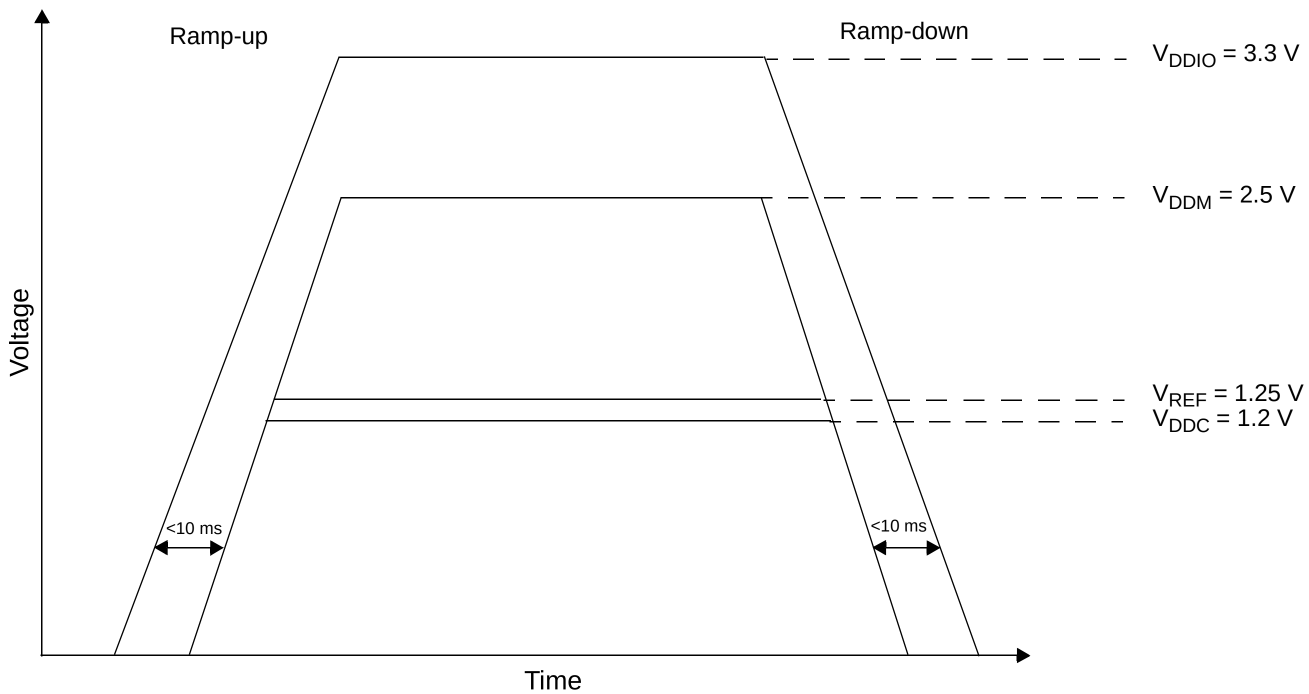

Figure 33. Voltage Sequencing Case 4

3.2.2.5 Case 5 (not recommended for new designs)

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDM} (2.5 V) supply second.
3. Turn on the V_{DDC} (1.2 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn off the V_{DDM} (2.5 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDM} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 2 ms for power-up and power-down.
- Refer to **Figure 34** for relative timing for power sequencing case 5.

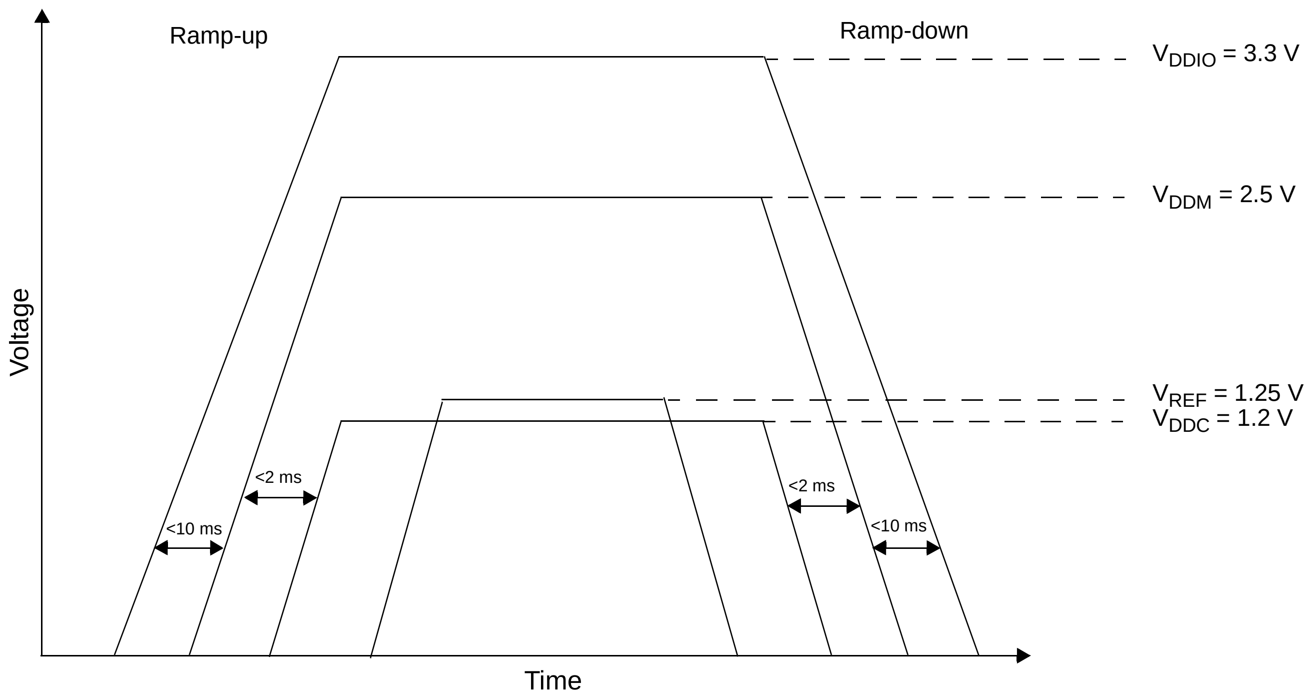

Figure 34. Voltage Sequencing Case 5

Note: Cases 1, 2, 3, and 4 are recommended for system design. Designs that use Case 5 may have large current spikes on the V_{DDM} supply at startup and is not recommended for most designs. If a design uses case 5, it must accommodate the potential current spikes. Verify risks related to current spikes using actual information for the specific application.

3.2.3 Power Planes

Each power supply pin (V_{DDC}, V_{DDM}, and V_{DDIO}) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC7116 V_{DDC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 3.5** for DDR Controller power guidelines.

3.2.4 Decoupling

Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a 0.01 µF high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one 10 µF and one 47 µF, (with low ESR and ESL) mounted as closely as possible to the MSC7116 voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A.

3.2.5 PLL Power Supply Filtering

The MSC7116 V_{DDPLL} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. V_{DDPLL} can be connected to V_{DDC} through a 2 Ω resistor. V_{SSPLL} can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 35** is recommended. The PLL loop filter should be placed as closely as possible to the V_{DDPLL} pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits.The 0.01 µF capacitor should be closest to V_{DDPLL}, followed by the 0.1 µF capacitor, the 10 µF capacitor, and finally the 2-Ω resistor to V_{DDC}. These traces should be kept short.

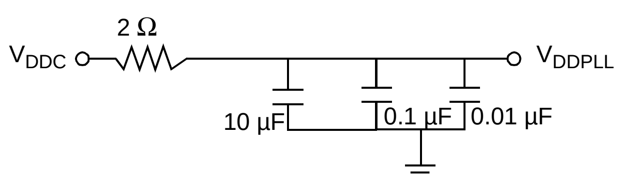

Figure 35. PLL Power Supply Filter Circuits

3.2.6 Power Consumption

You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:

- *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
- *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
- *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
- *Peripheral subsystem*. Halt the individual on-device peripherals such as the DDR memory controller, Ethernet MAC, HDI16, TDM, UART, I^2C, and timer modules.

For details, see the “Clocks and Power Management” chapter of the *MSC711x Reference Manual*.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

3.4.3.2 I²C Boot

When the MSC7116 device is configured to boot from the I²C port, the boot program configures the GPIO pins for I²C operation. Then the MSC7116 device initiates accesses to the I²C module, downloading data to the MSC7116 device. The I²C interface is configured as follows:

- PLL is disabled and bypassed so that the I²C module is clocked with the IPBus clock.
- I²C interface operates in master mode and polling is used.
- EPROM operates in slave mode.
- Clock divider is set to 128.
- Address of slave during boot is 0xA0.

The IPBus clock is internally divided to generate the bit clock, as follows:

- CLKIN must be a maximum of 100 MHz
- PLL is bypassed.
- IPBus clock = CLKIN/2 is a maximum of 50 MHz.
- I²C bit clock must be less than or equal to:
  - IPBus clock/I²C clock divider
  - 50 MHz (max)/128
  - 390.6 KHz

This satisfies the maximum clock rate requirement of 400 kbps for the I²C interface. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.4.3.3 SPI Boot

When the MSC7116 device is configured to boot from the SPI port, the boot program configures the GPIO pins for SPI operation. Then the MSC7116 device initiates accesses to the SPI module, downloading data to the MSC7116 device. When the SPI routines run in the boot ROM, the MSC7116 is always configured as the SPI master. Booting through the SPI is supported for serial EEPROM devices and serial Flash devices. When a READ_ID instruction is issued to the serial memory device and the device returns a value of 0x00 or 0xFF, the routines for accessing a serial EEPROM are used, at a maximum frequency of 4 Mbps. Otherwise, the routines for accessing a serial Flash are used, and they can run at faster speeds. Booting is performed through one of two sets of pins:

- Main set: BM[2–3], HA3, and HCS2, which allow use of the PLL.
- Alternate set: UTXD, URXD, SDA, and SCL, which cannot be used with the PLL.

In either configuration, an error during SPI boot is flagged on the EVNT3 pin. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.5 DDR Memory System Guidelines

MSC7116 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in Figure 36. Technique B is the most popular termination technique.

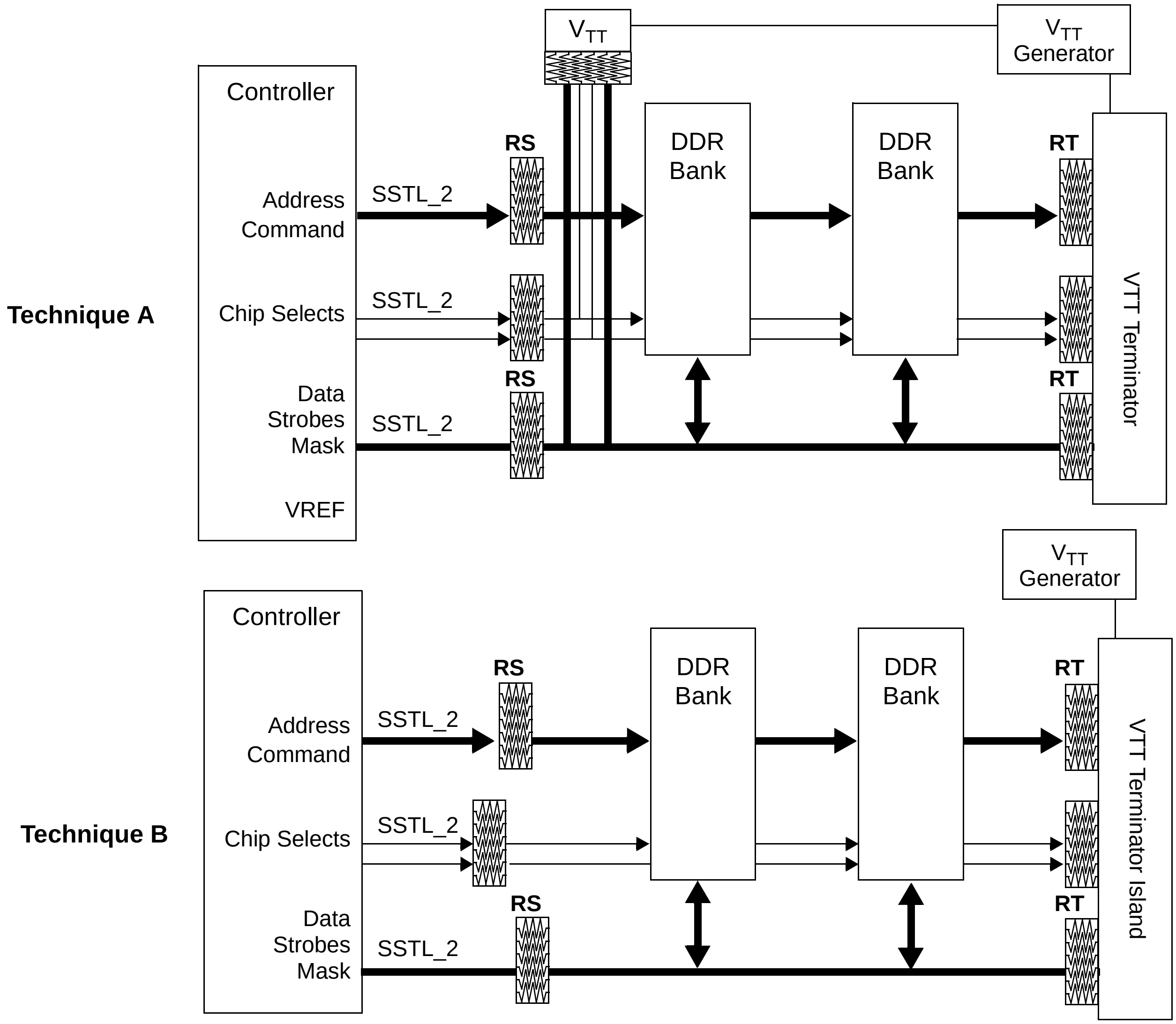

Figure 36. SSTL Termination Techniques

Figure 37 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

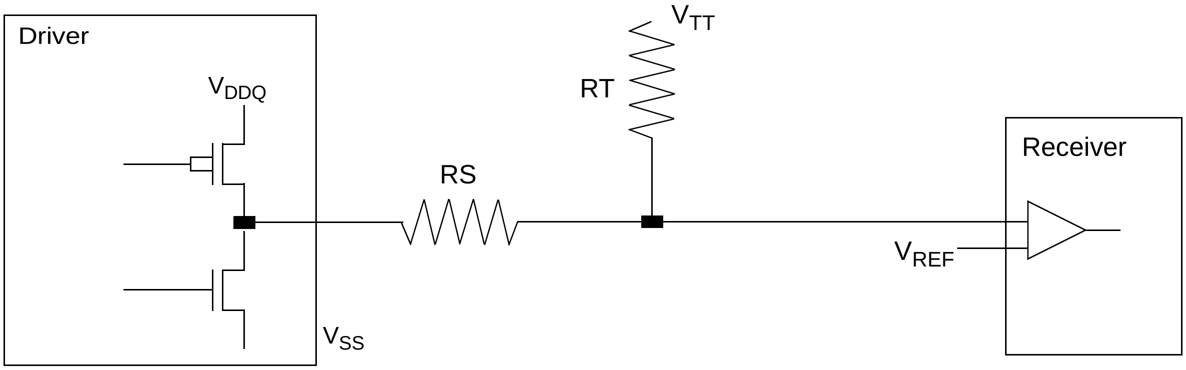

Figure 37. SSTL Power Value

3.5.1 V_{REF} and V_{TT} Design Constraints

V_{TT} and V_{REF} are isolated power supplies at the same voltage, with V_{TT} as a high current power source. This section outlines the voltage supply design needs and goals:

- Minimize the noise on both rails.
- V_{TT} must track variation in the V_{REF} DC offsets. Although they are isolated supplies, one possible solution is to use a single IC to generate both signals.
- Both references should have minimal drift over temperature and source supply.
- It is important to minimize the noise from coupling onto V_{REF} as follows:
  — Isolate V_{REF} and shield it with a ground trace.
  — Use 15–20 mm track.
  — Use 20–30 mm clearance between other traces for isolating.
  — Use the outer layer route when possible.
  — Use distributed decoupling to localize transient currents and return path and decouple with an inductance less than 3 nH.
- Max source/sink transient currents of up to 1.8 A for a 32-bit data bus.
- Use a wide island trace on the outer layer:
  — Place the island at the end of the bus.
  — Decouple both ends of the bus.
  — Use distributed decoupling across the island.
  — Place SSTL termination resistors inside the V_{TT} island and ensure a good, solid connection.
- Place the V_{TT} regulator as closely as possible to the termination island.
  — Reduce inductance and return path.
  — Tie current sense pin at the midpoint of the island.

3.5.2 Decoupling

The DDR decoupling considerations are as follows:

- DDR memory requires significantly more burst current than previous SDRAMs.
- In the worst case, up to 64 drivers may be switching states.
- Pay special attention and decouple discrete ICs per manufacturer guidelines.
- Leverage V_{TT} island topology to minimize the number of capacitors required to supply the burst current needs of the termination rail.
- See the Micron DesignLine publication entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* (`http://download.micron.com/pdf/pubs/designline/3Q00dl1-4.pdf`).