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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5603pef1mll4r

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5603P/4P series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

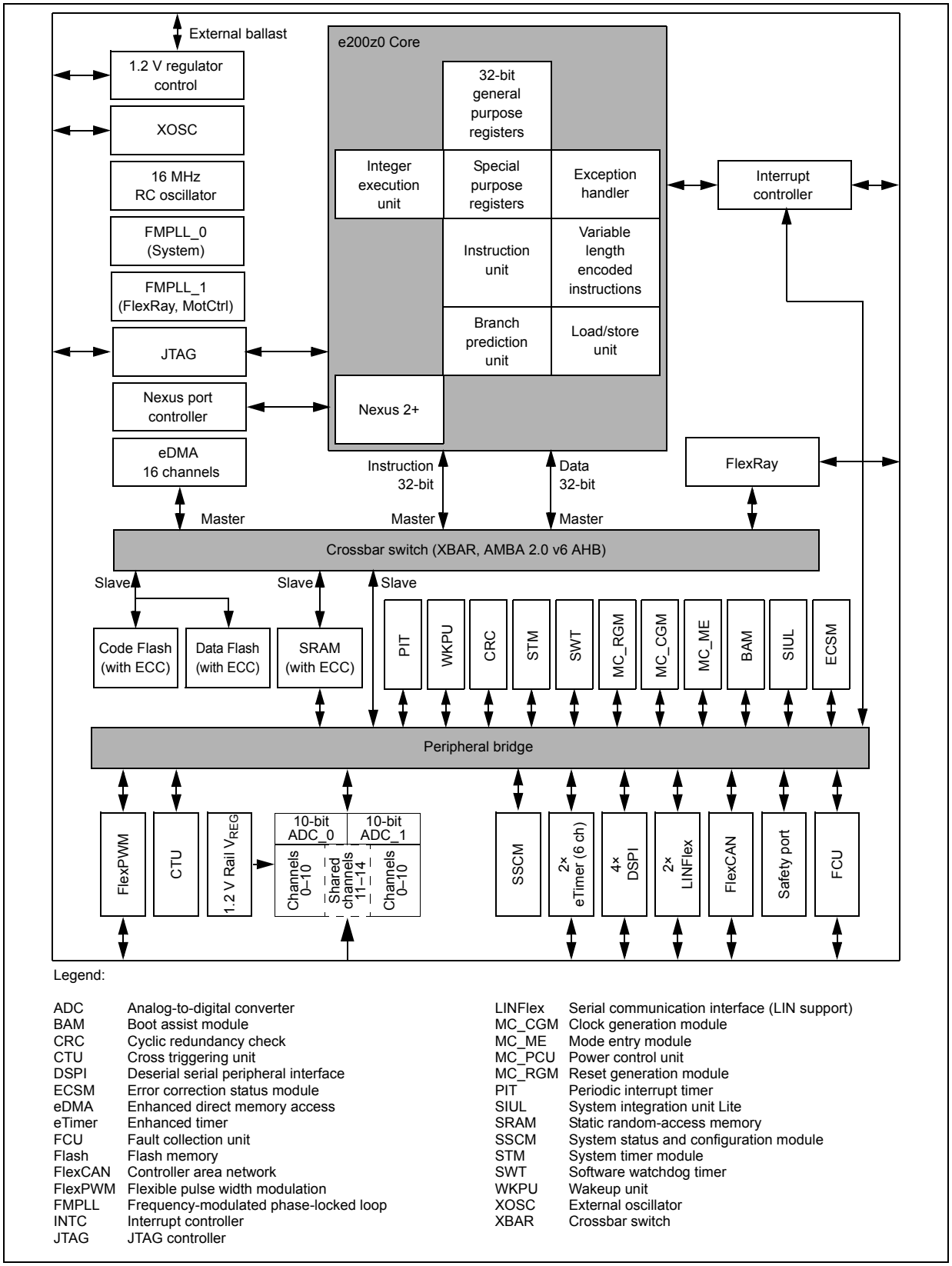
The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 1 provides a summary of different members of the MPC5604P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5604P device comparison

Feature	MPC5603P	MPC5604P
Code flash memory (with ECC)	384 KB	512 KB
Data flash memory / EE option (with ECC)	64 KB (optional feature)	
SRAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	
eDMA (enhanced direct memory access) channels	16	
FlexRay[1]	Optional feature	
FlexCAN (controller area network)	2[2,3]	
Safety port	Yes (via second FlexCAN module)	
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	Yes	



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. MPC5604P block diagram

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 4 master ports:
  - e200z0 core complex Instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
  - FlexRay
- 3 slave ports:
  - Flash memory (code flash and data flash)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer for assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The MPC5604P provides as much as 576 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory

array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

- As much as 576 KB flash memory
  - 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 64-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The MPC5604P SRAM module provides up to 40 KB of general-purpose memory.

ECC handling is done on a 32-bit boundary and is completely software compatible with MPC55xx family devices with an e200z6 core and 64-bit wide ECC.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 40 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5604P:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency: 4–40 MHz

- Input capture trigger
- Output compare
- Double buffer (to capture rising edge and falling edge)
- Separate prescaler for each counter
- Selectable clock source
- 0–100% pulse measurement
- Rotation direction flag (Quad decoder mode)

- Maximum count rate
  - External event counting: max. count rate = peripheral clock/2
  - Internal clock counting: max. count rate = peripheral clock
- Counters are:
  - Cascadable
  - Preloadable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.27 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 2 on-chip AD converters
  - 10-bit AD resolution
  - 1 sample and hold unit per ADC
  - Conversion time, including sampling time, less than 1 µs (at full precision)
  - Typical sampling time is 150 ns min. (at full precision)
  - Differential non-linearity error (DNL) ±1 LSB
  - Integral non-linearity error (INL) ±1.5 LSB
  - TUE <3 LSB
  - Single-ended input signal up to 5.0 V
  - The ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  - The ADC supply can be equal or higher than V_{DDIO}
  - The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel

- ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
- Selectable priority between software and hardware injected commands
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
- DMA compatible interface

- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

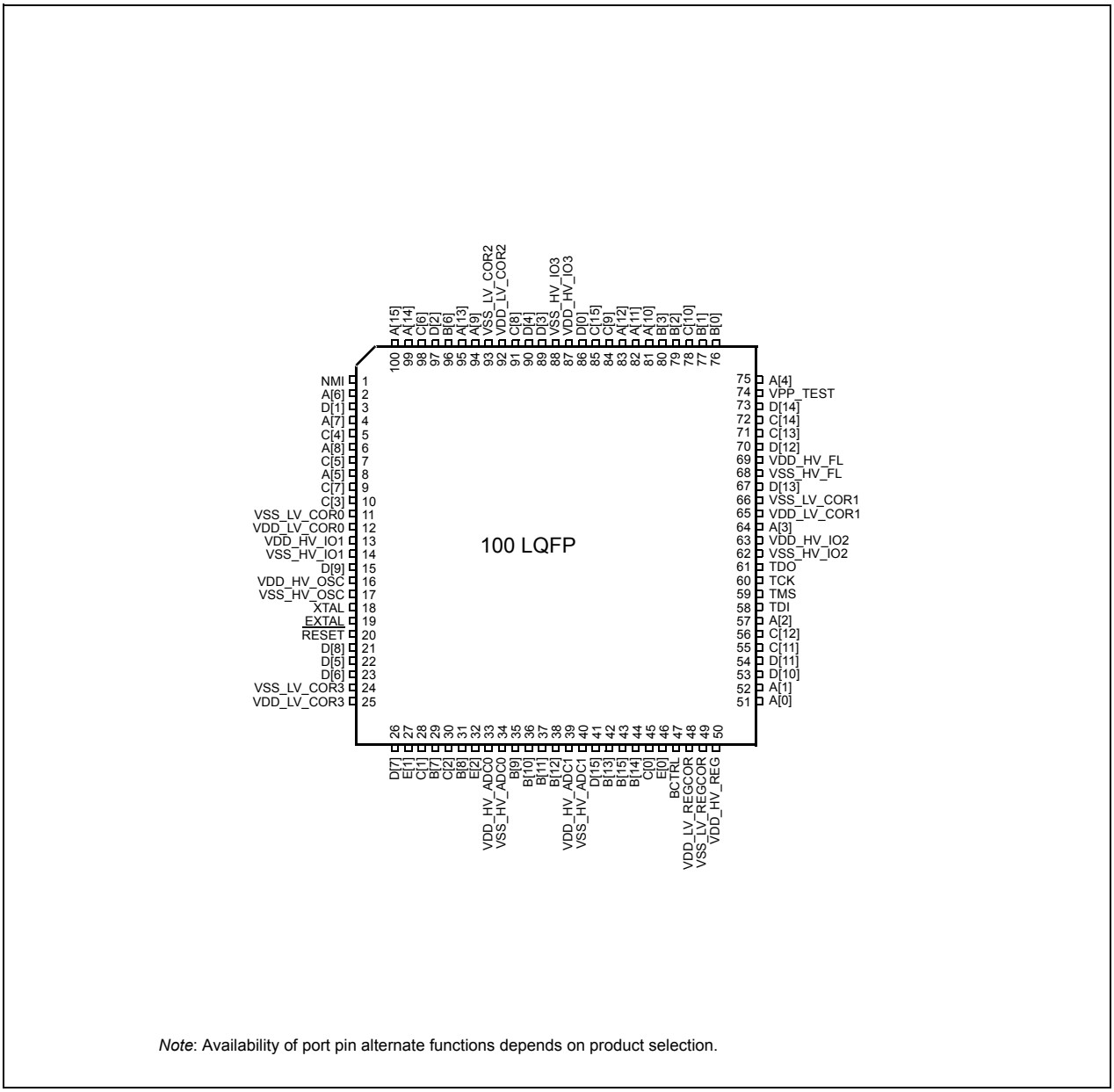
- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the MPC5604P Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information



Note: Availability of port pin alternate functions depends on product selection.

Figure 3. 100-pin LQFP pinout (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5604P devices.

2.2.1 Power supply and reference voltage pins

Table 3 lists the power supply and reference voltage for the MPC5604P devices.

Table 5. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] B[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	90	129
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIUL DSPI_0 FCU_0 DSPI_3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIUL DSPI_0 DSPI_3 — FlexPWM_0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIUL DSPI_1 FCU_0 DSPI_0 DSPI_3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O I/O O —	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIUL FlexPWM_0 DSPI_3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O O	Slow	Medium	67	95

Table 5. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	48
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[6]	SIUL — — — ADC_1	Input only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[7]	SIUL — — — ADC_1	Input only	—	—	—	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[8]	SIUL — — — ADC_1	Input only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[9]	SIUL — — — ADC_1	Input only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[10]	SIUL — — — ADC_1	Input only	—	—	—	67
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

CAUTION

All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

[3] Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.

[4] Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

[5] STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 21 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$, NVUSRO[PAD3V5V] = 1); see Figure 13.

Table 21. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)[1]

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1[2]	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	

[1] These specifications are design targets and subject to change per device characterization.

Table 29. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
C_{JITTER}	T	CLKOUT period jitter[6,7,8,9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (avg. over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4,000 cycles	—	10	ns
t_{lpll}	D	PLL lock time [11, 12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	-18	18	% f_{SYS}
f_{CS} f_{DS}	D	Modulation depth		Center spread	±0.25	±4.0[13]	% f_{SYS}
				Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1 $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified

2 Considering operation with PLL not bypassed

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

6 This value is determined by the crystal manufacturer and board design.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

8 Proper PC board layout procedures must be followed to achieve specifications.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

10 Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.

11 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

12 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

13 This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

14 Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

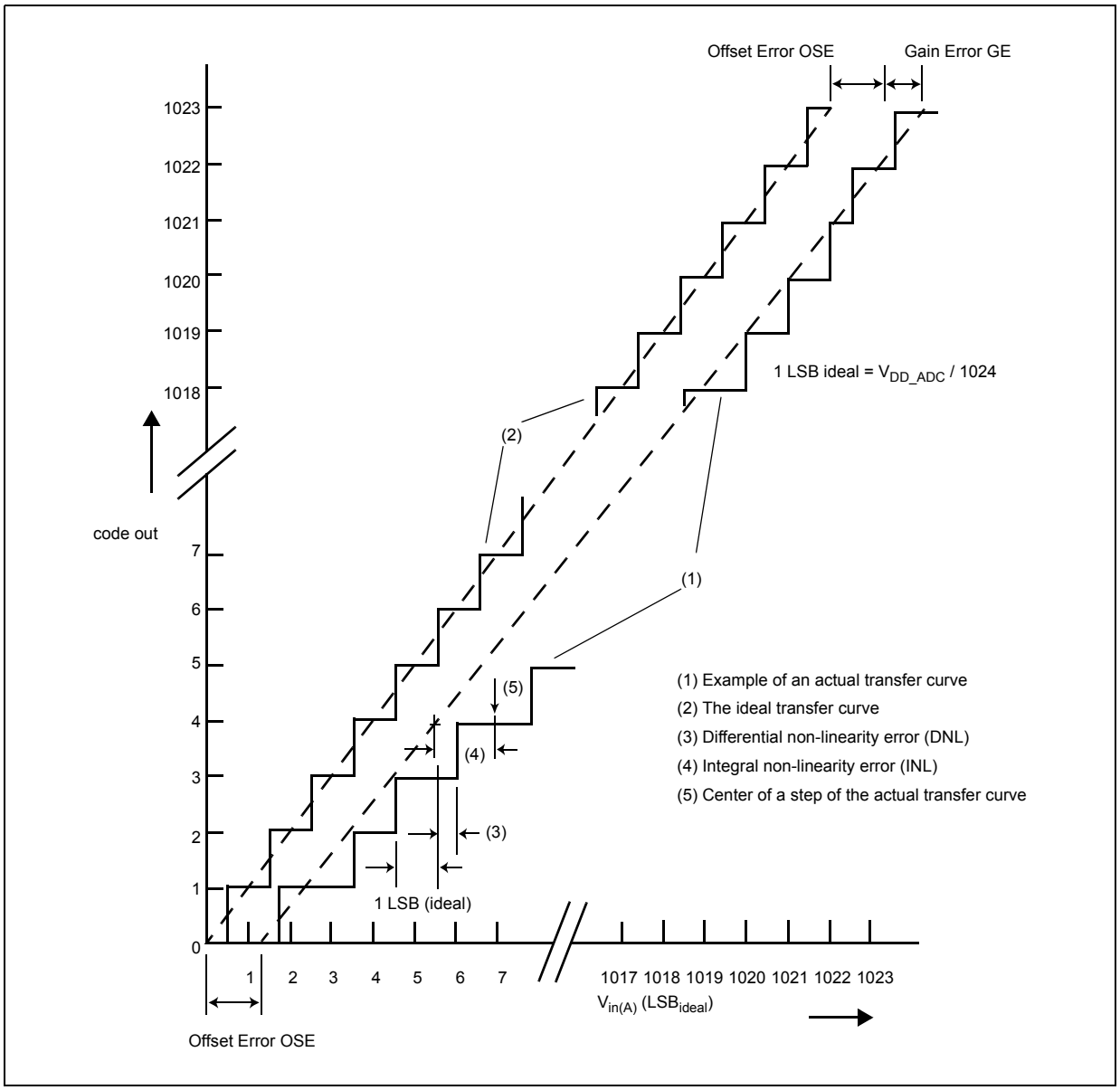


Figure 14. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.

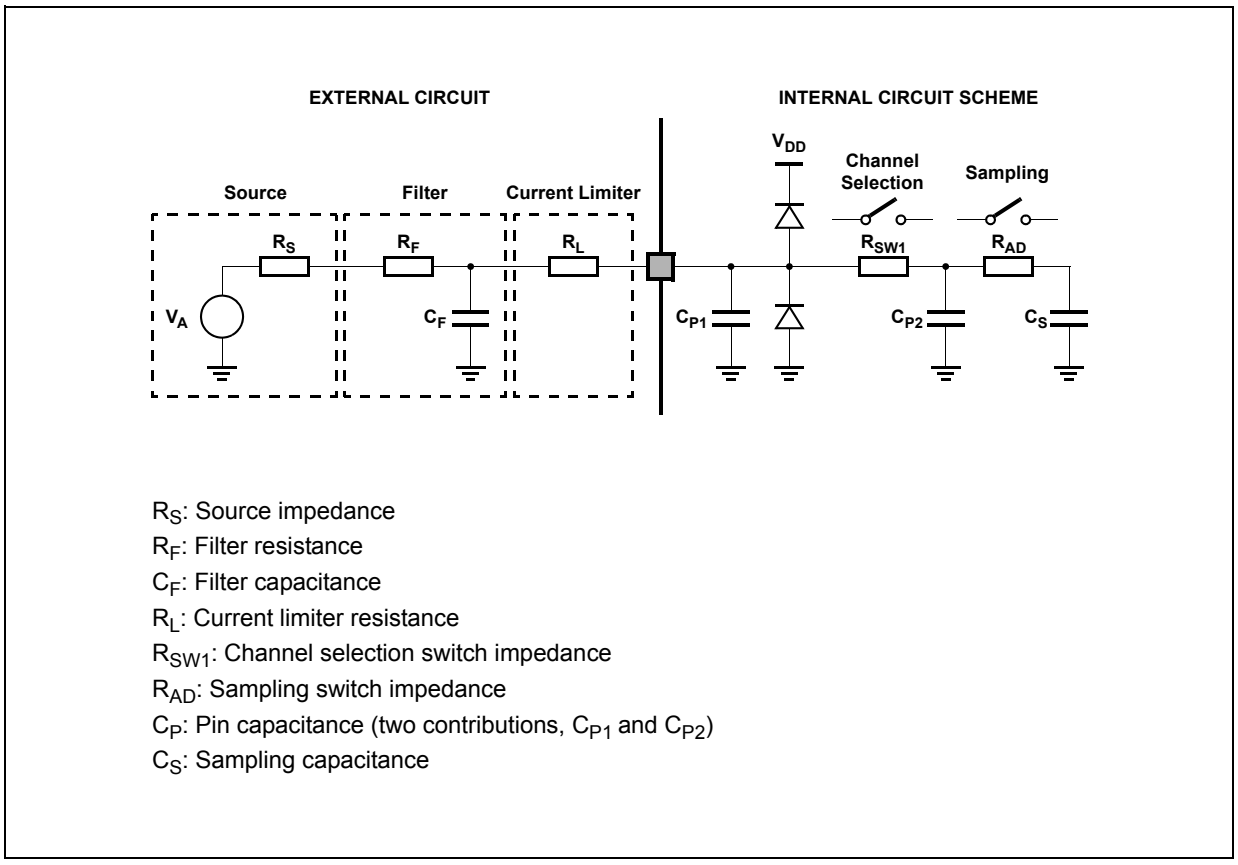


Figure 15. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 15): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 31. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{INAN0}	SR		ADC0 and shared ADC0/1 analog input voltage[2, 3]	—	$V_{SS\_HV\_ADV0} - 0.3$	—	$V_{DD\_HV\_ADV0} + 0.3$	V
V_{INAN1}	SR		ADC1 analog input voltage[2, 4]	—	$V_{SS\_HV\_ADV1} - 0.3$	—	$V_{DD\_HV\_ADV1} + 0.3$	V
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[5] frequency)	—	3[6]	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	—	D	Sample time[7]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	—	P	Conversion time[8]	f_{ADC} = 20 MHz[9], INPCMP = 1	0.650	—	—	µs
t_{ADC_PU}	SR	—	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	—	—	—	1.5	µs
C_S[10]	—	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[10]	—	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[10]	—	D	ADC input pin capacitance 2	—	—	—	1	pF

Table 31. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
R_{SW1}[10]	—	D	Internal resistance of analog source	$V_{DD\_HV\_ADC}$ = 5 V ± 10%	—	—	0.6	kΩ
				$V_{DD\_HV\_ADC}$ = 3.3 V ± 10%	—	—	3	kΩ
R_{AD}[10]	—	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	—	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	CC	P	Integral non-linearity	No overload	–1.5	—	1.5	LSB
DNL	CC	P	Differential non-linearity	No overload	–1.0	—	1.0	LSB
OSE	CC	T	Offset error	—	—	±1	—	LSB
GE	CC	T	Gain error	—	—	±1	—	LSB
TUE	CC	P	Total unadjusted error without current injection	—	–2.5	—	2.5	LSB
TUE	CC	T	Total unadjusted error with current injection	—	–3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_ADCx}$ to $V_{DD\_HV\_ADCx}$.

2 V_{AINx} may exceed $V_{SS\_HV\_AD}$ and $V_{DD\_HV\_AD}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

3 Not allowed to refer this voltage to $V_{DD\_HV\_ADV1}$, $V_{SS\_HV\_ADV1}$

4 Not allowed to refer this voltage to $V_{DD\_HV\_ADV0}$, $V_{SS\_HV\_ADV0}$

5 AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

6 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.

7 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

8 This parameter includes the sample time t_{ADC_S}.

9 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

10 See Figure 15.

3.15 Flash memory electrical characteristics

Table 32. Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typical[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
T_{BKPRG}	P	Bank Program (512 KB)[4, 5]	—	1.45	1.65	33	s
	P	Bank Program (64 KB)[4, 5]	—	0.18	0.21	4.10	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 33. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

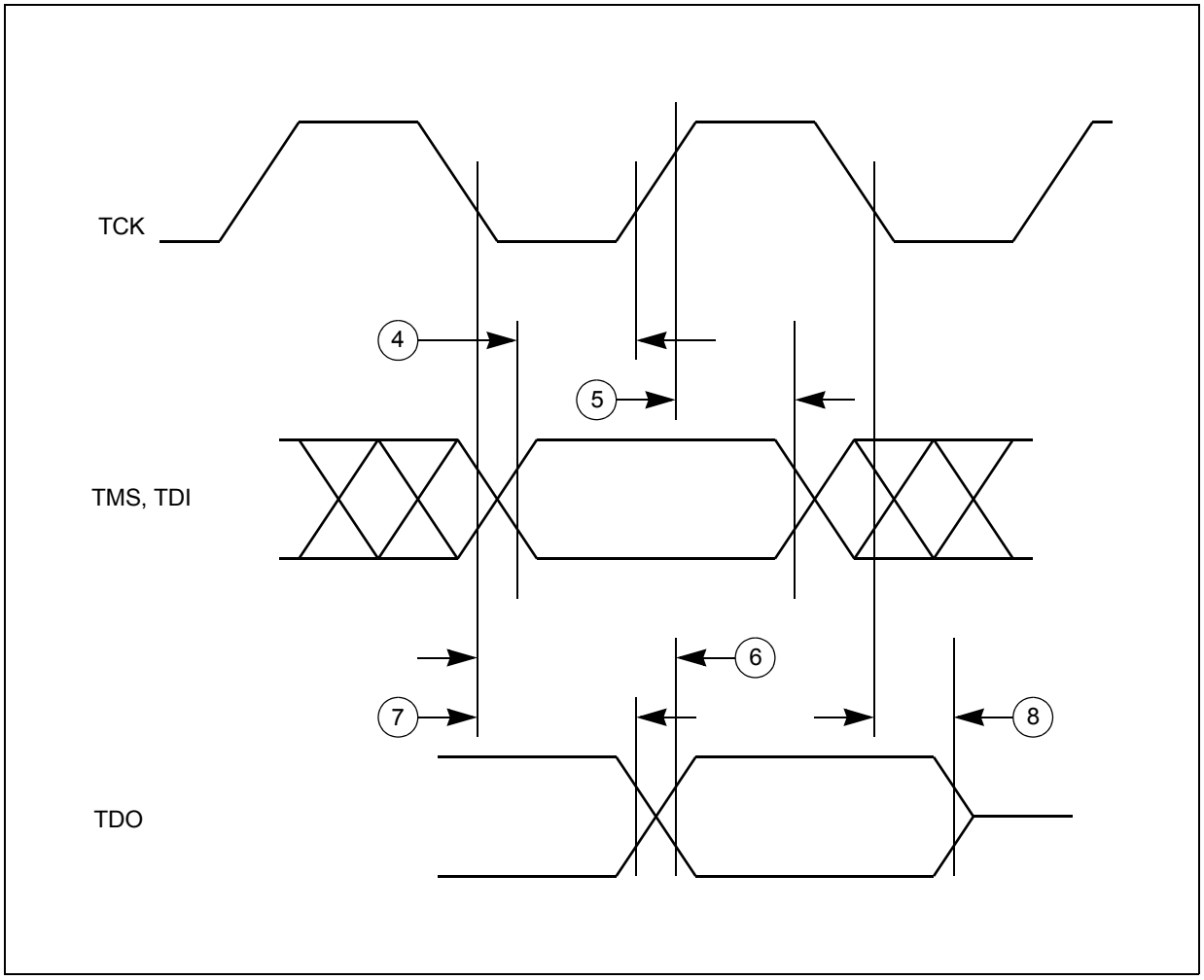
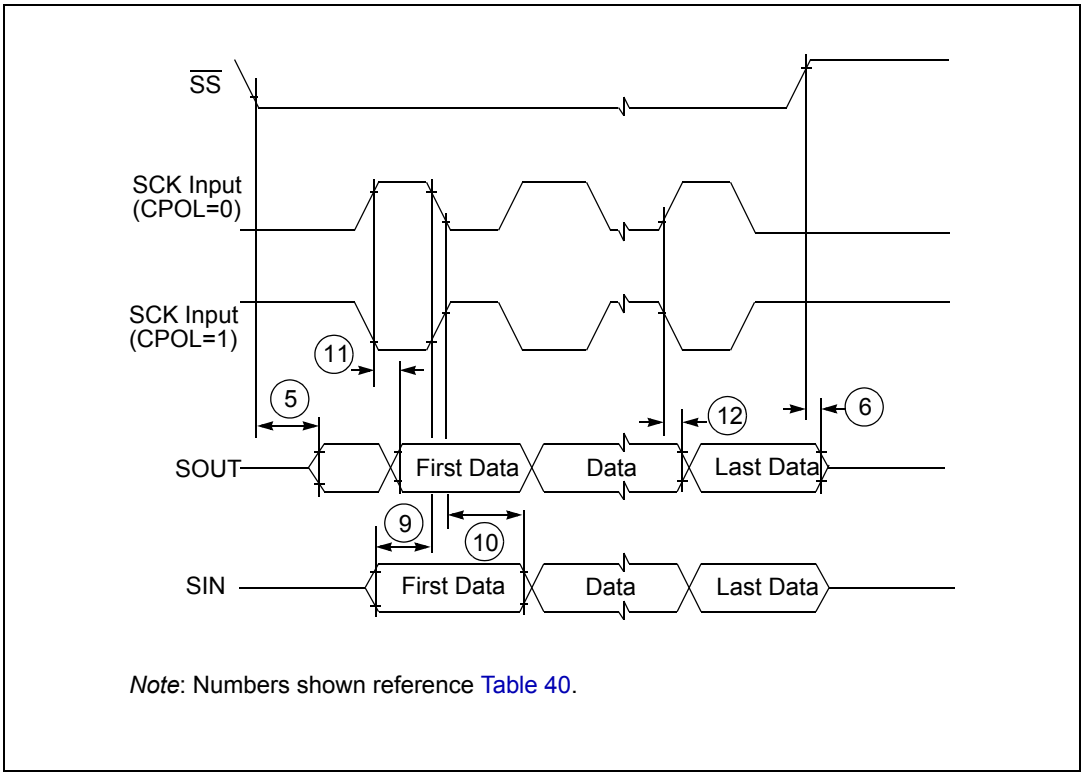
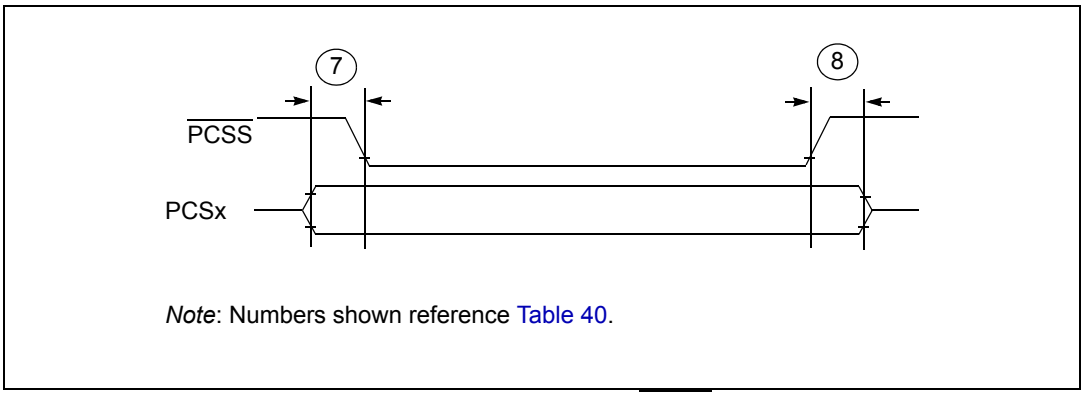


Figure 22. JTAG test access port timing



Note: Numbers shown reference Table 40.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 1



Note: Numbers shown reference Table 40.

Figure 36. DSPI PCS strobe (PCSS) timing