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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	108
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604pgf0mlq6

- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

1.5.13 System timer module (STM)

The STM module implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

— Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  — 4 MDO (Message Data Out) pins
  — MCKO (Message Clock Out) pin
  — 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  — $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  — $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT ($x25$ protocol):
  — $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  — $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  — BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  — ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

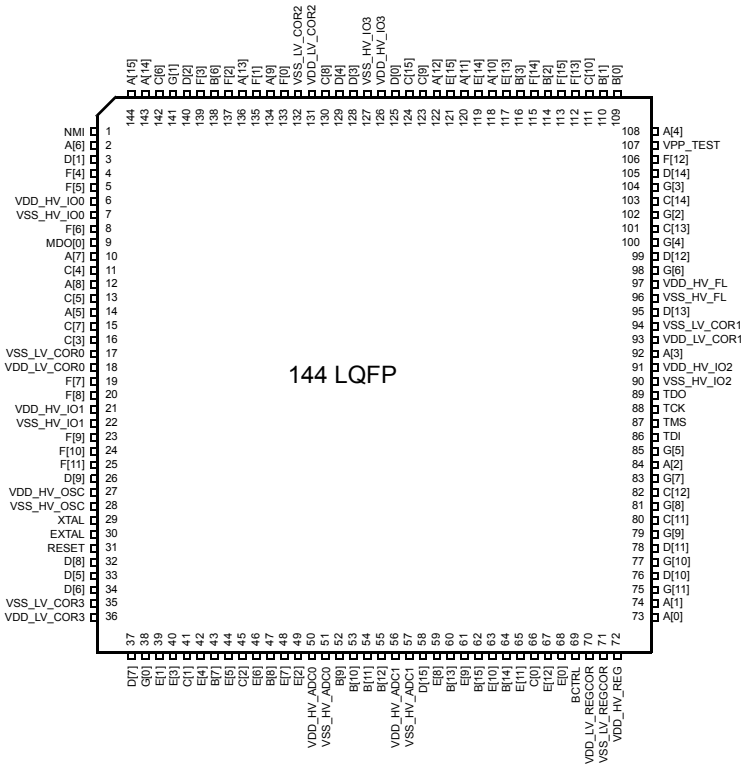
The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



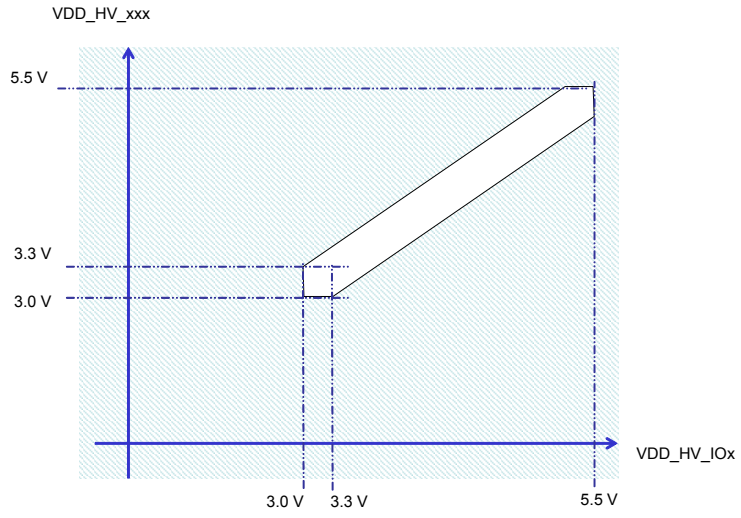
Note: Availability of port pin alternate functions depends on product selection.

Figure 2. 144-pin LQFP pinout (top view)

Table 5. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — — — SIN EIRQ[8]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	Slow	Medium	6	12
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1 — B[3] FAULT[0]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	94	134
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0 B[0] X[2] EIRQ[9]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O I/O I	Slow	Medium	81	118
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	82	120
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	83	122
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	95	136
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD ETC[4] — EIRQ[13]	SIUL Safety Port_0 eTimer_1 — SIUL	I/O O I/O — I	Slow	Medium	99	143
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — ETC[5] — RXD EIRQ[14]	SIUL — eTimer_1 — Safety Port_0 SIUL	I/O — I/O — I I	Slow	Medium	100	144

Figure 6 shows the constraints of the different power supplies.



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

Figure 6. Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)

The MPC5604P supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. Figure 7 shows the constraints of the ADC power supply.

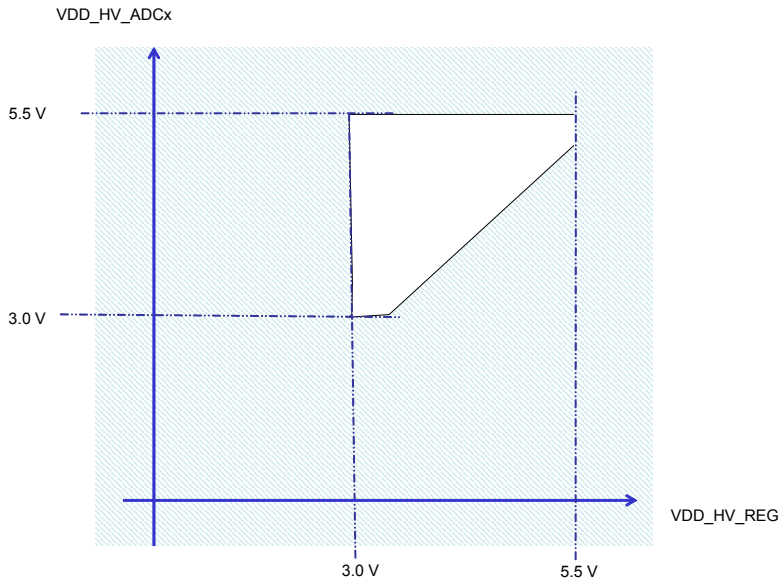


Figure 7. Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)

[5] Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Table 14. Approved NPN ballast components (configuration with resistor on base)

Part	Manufacturer	Approved derivatives[1]
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10;BCX68-16;BCX68-25
BC868	NXP	BC868
BC817	Infineon	BC817-16;BC817-25;BC817SU;
	NXP	BC817-16;BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10;BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10;BCP56-16

1 For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 15. Voltage regulator electrical characteristics (configuration with resistor on base)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
R_B	SR	—	External resistance on bipolar junction transistor (BJT) base	—	18	—	22	kΩ
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from Table 14. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF

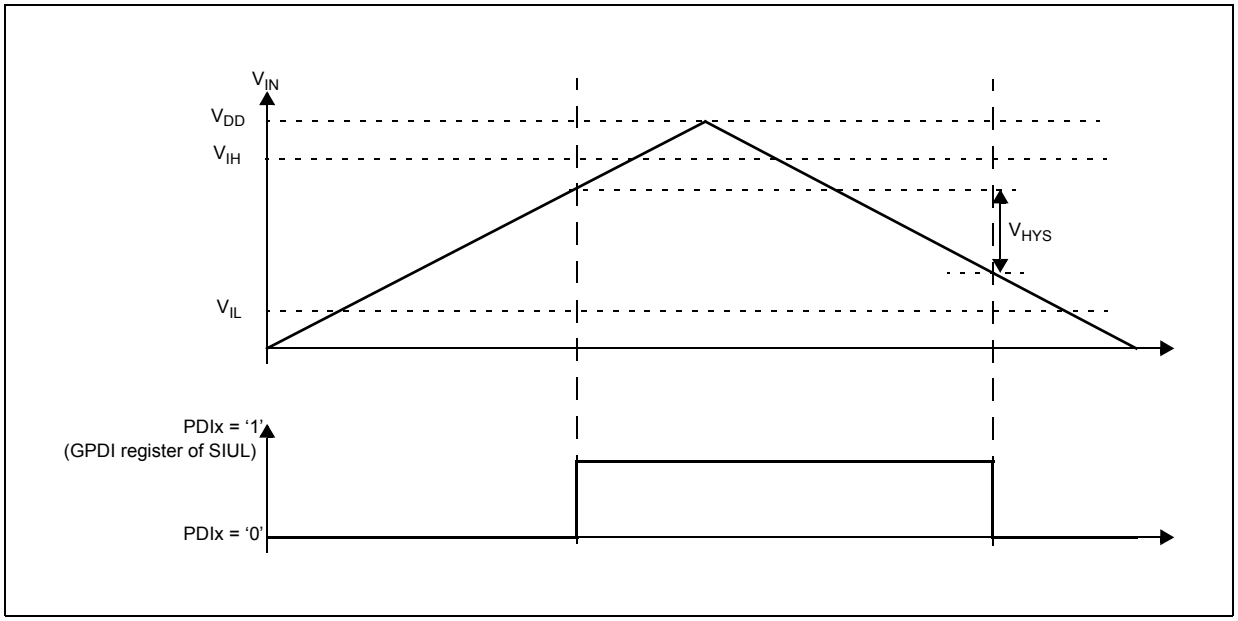


Figure 13. Input DC electrical characteristics definition

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 23.

Table 23. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
144 LQFP	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
100 LQFP	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 24 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 24. I/O weight

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—
PAD[85]	9%	7%	—	—

Table 24. I/O weight (continued)

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[60]	11%	10%	11%	10%
PAD[100]	12%	10%	—	—
PAD[45]	12%	10%	12%	10%
PAD[98]	12%	11%	—	—
PAD[46]	12%	11%	12%	11%
PAD[99]	13%	11%	—	—
PAD[62]	13%	11%	13%	11%
PAD[92]	13%	12%	—	—
VPP_TEST	1%	1%	1%	1%
PAD[4]	14%	12%	14%	12%
PAD[16]	13%	12%	13%	12%
PAD[17]	13%	11%	13%	11%
PAD[42]	13%	11%	13%	11%
PAD[93]	12%	11%	—	—
PAD[95]	12%	11%	—	—
PAD[18]	12%	10%	12%	10%
PAD[94]	11%	10%	—	—
PAD[19]	11%	10%	11%	10%
PAD[77]	10%	9%	—	—
PAD[10]	10%	9%	10%	9%
PAD[78]	9%	8%	—	—
PAD[11]	9%	8%	9%	8%
PAD[79]	8%	7%	—	—
PAD[12]	7%	7%	7%	7%
PAD[41]	7%	6%	7%	6%
PAD[47]	5%	4%	5%	4%
PAD[48]	4%	4%	4%	4%
PAD[51]	4%	4%	4%	4%
PAD[52]	5%	4%	5%	4%
PAD[40]	5%	5%	6%	5%
PAD[80]	9%	8%	—	—
PAD[9]	10%	9%	11%	10%
PAD[81]	10%	9%	—	—

Table 24. I/O weight (continued)

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[13]	10%	9%	12%	11%
PAD[82]	10%	9%	—	—
PAD[22]	10%	9%	13%	12%
PAD[83]	10%	9%	—	—
PAD[50]	10%	9%	14%	12%
PAD[97]	10%	9%	—	—
PAD[38]	10%	9%	14%	13%
PAD[14]	9%	8%	14%	13%
PAD[15]	9%	8%	15%	13%

Table 25. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(2)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}(2)	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	

3.13 16 MHz RC oscillator electrical characteristics

Table 30. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

[1] PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit successive approximation register (SAR) analog-to-digital converter.

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 31. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{INAN0}	SR		ADC0 and shared ADC0/1 analog input voltage[2, 3]	—	$V_{SS\_HV\_ADV0} - 0.3$	—	$V_{DD\_HV\_ADV0} + 0.3$	V
V_{INAN1}	SR		ADC1 analog input voltage[2, 4]	—	$V_{SS\_HV\_ADV1} - 0.3$	—	$V_{DD\_HV\_ADV1} + 0.3$	V
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[5] frequency)	—	3[6]	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	—	D	Sample time[7]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	—	P	Conversion time[8]	f_{ADC} = 20 MHz[9], INPCMP = 1	0.650	—	—	µs
t_{ADC_PU}	SR	—	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	—	—	—	1.5	µs
C_S[10]	—	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[10]	—	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[10]	—	D	ADC input pin capacitance 2	—	—	—	1	pF

Table 36. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

2 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

4 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 37. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

Table 37. JTAG pin AC electrical characteristics (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

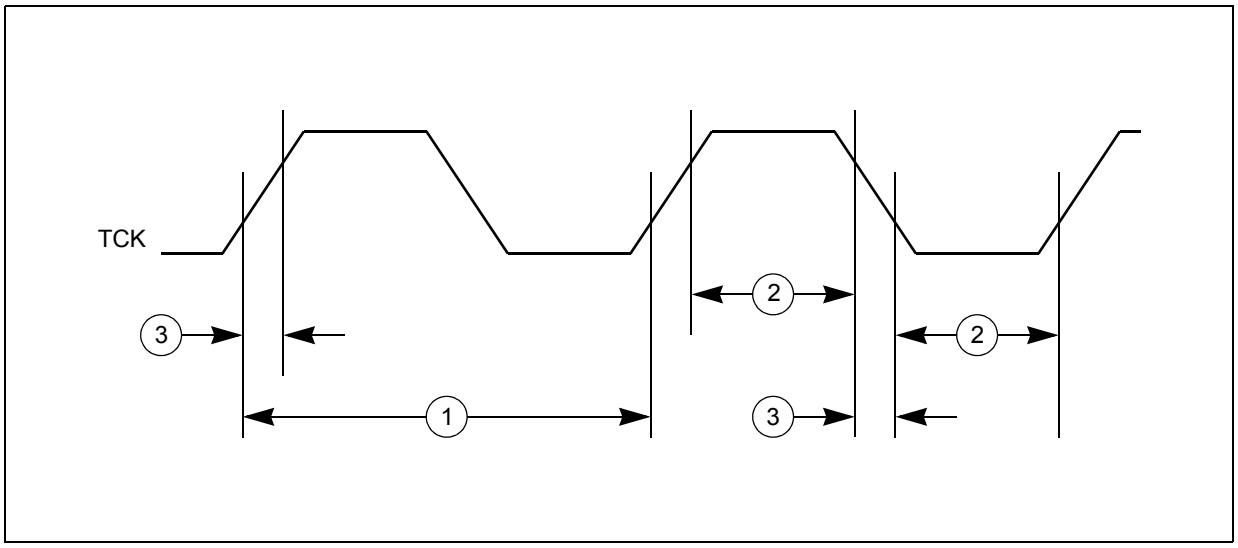
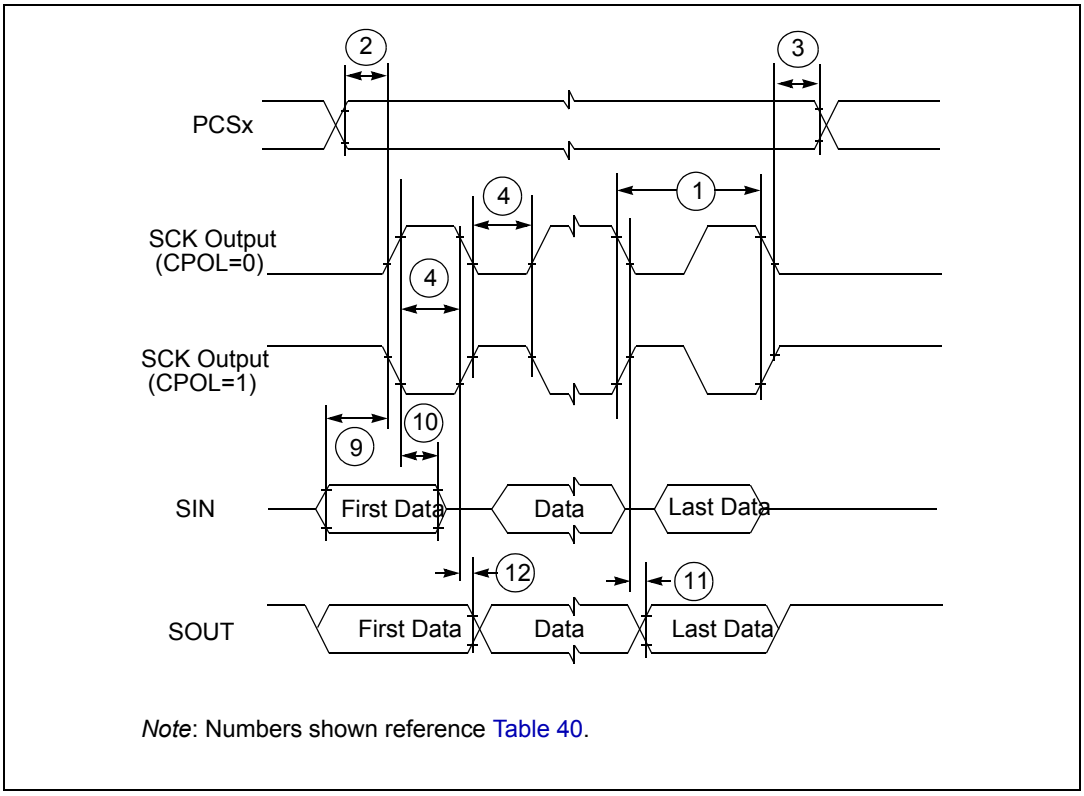


Figure 21. JTAG test clock input timing

Table 40. DSPI timing[1] (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1 All timing is provided with 50 pF capacitance on output, 1 ns transition time on input signal.



Note: Numbers shown reference Table 40.

Figure 28. DSPI classic SPI timing – Master, CPHA = 0

4 Package characteristics

4.1 Package mechanical data

4.1.1 144 LQFP mechanical outline drawing

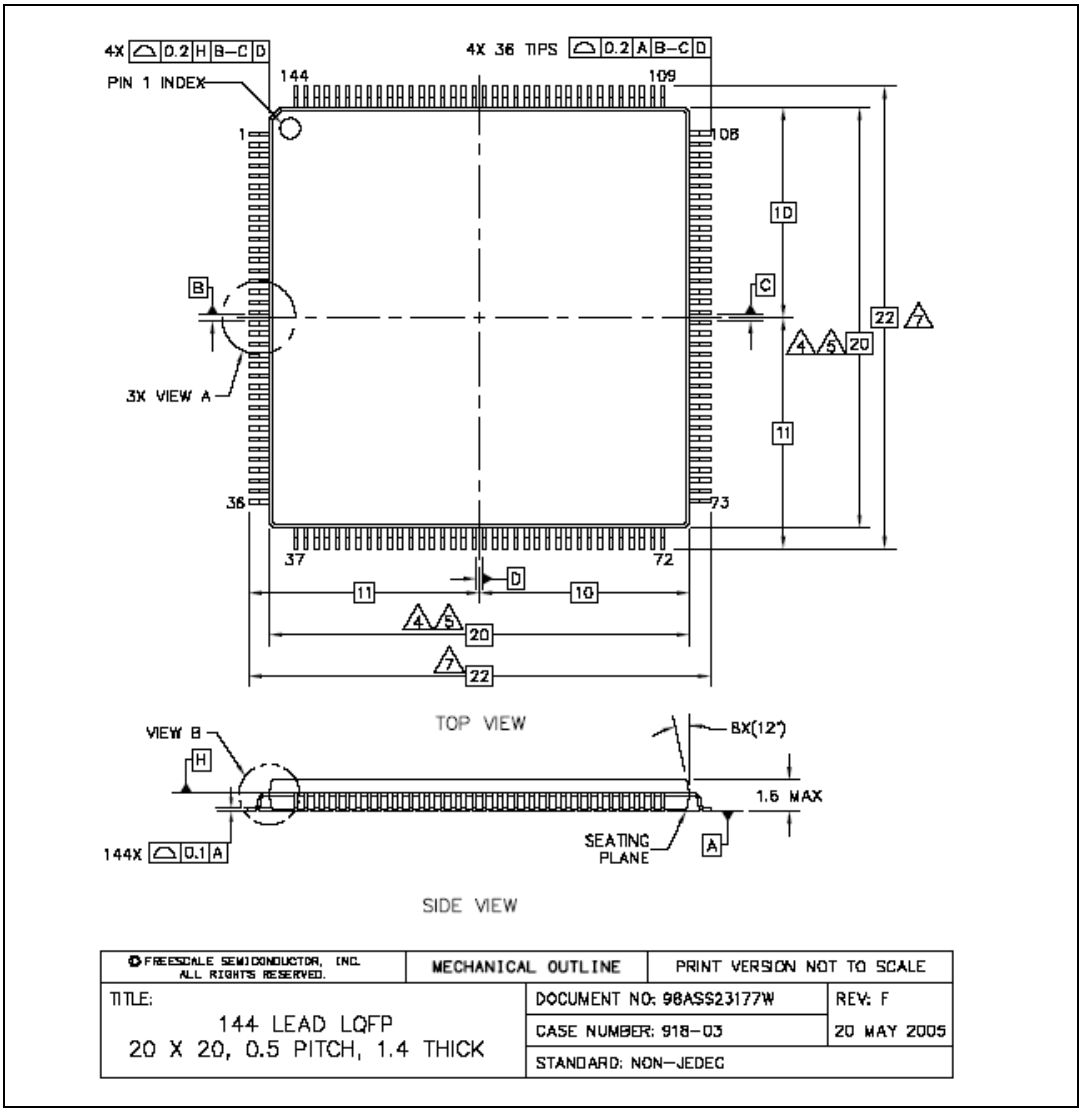
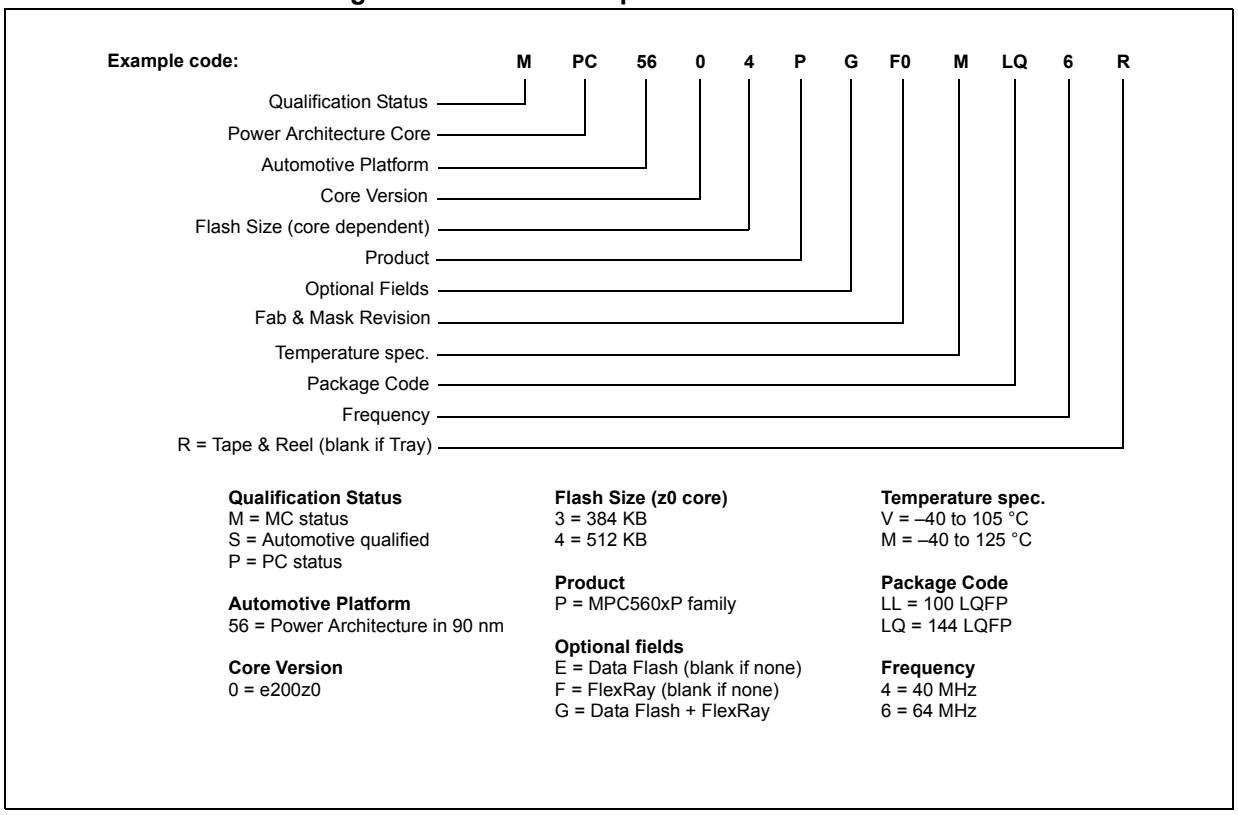


Figure 37. 144 LQFP package mechanical drawing (part 1)

5 Ordering information

Figure 42. Commercial product code structure



Appendix A Abbreviations

Table A-1 lists abbreviations used in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input/output
MC	Modulus counter
MCKO	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RBW	Resolution bandwidth
SCK	Serial communications clock
SOUT	Serial data out
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

6 Document revision history

Table 42 summarizes revisions to this document.

Table 42. Revision history

Revision	Date	Substantive changes
Rev. 1	Aug 2008	Initial release
Rev. 2	Nov 2008	Table 5: TDO and TDI pins (Port pins B[4:5] are single function pins. Table 10, Table 11: Thermal characteristics added. Table 11, Table 12: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 16, Table 17, Table 19, Table 20: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 21: • Values for I_{OL} and I_{OH} (in Conditions column) changed. • Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. • V_{ILR} max value changed. • I_{PUR} min and max values changed. Table 27: Sensitivity value changed. Table 30: Most values in table changed.
Rev. 3	Feb 2009	• Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. • Electrical parameters updated. • EMI characteristics are now in one table; values have been updated. • ESD characteristics are now in one table. • Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. • AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted

Table 42. Revision history (continued)

Revision	Date	Substantive changes
Rev. 4	24-Jun-2009	Through all document: – Replaced all “RESET_B” occurrences with “$\overline{\text{RESET}}$” through all document. – AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections inserted again. – Electrical parameters updated. – Table 2 – Added row for Data Flash. Table 3 – Added a footnote regarding the decoupling capacitors. Table 5 – Removed the “other function“ column. – Rearranged the contents. Table 15 – Updated definition of Condition column. Table 20 – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". Table 22 – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". Table 30 – Updated the parameter definition of ΔRCMVAR. – Removed the condition definition of ΔRCMVAR. Table 30 – Added t_{ADC_C} and TUE rows. Table 31 – Added t_{ADC_C} and TUE rows. – Removed $R_{sw2.}$ Table 34 – Added. Table 29 – Updated and added footnotes. Section 3.17.1, “RESET pin characteristics – Replaces whole section. Table 38 – Renamed the “Flash (KB)“ heading column in “Code Flash / Data Flash (EE) (KB)“ – Replaced the value of RAM from 32 to 36KB in the last four rows.