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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	108
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604pgf1vlq6

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5603P/4P series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 1 provides a summary of different members of the MPC5604P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5604P device comparison

Feature	MPC5603P	MPC5604P
Code flash memory (with ECC)	384 KB	512 KB
Data flash memory / EE option (with ECC)	64 KB (optional feature)	
SRAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	
eDMA (enhanced direct memory access) channels	16	
FlexRay[1]	Optional feature	
FlexCAN (controller area network)	2[2,3]	
Safety port	Yes (via second FlexCAN module)	
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	Yes	

Table 4. System pins (continued)

Symbol	Description	Direction	Pad speed[1]		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
EXTAL	• Analog input of oscillator amplifier circuit, when oscillator not in bypass mode • Analog input for clock generator when oscillator in bypass mode	—	—	—	19	30
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input only	Slow	—	60	88
TDI	Test Data In	Input only	Slow	Medium	58	86
TDO	Test Data Out	Output only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1 SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin muxing

Table 5 defines the pin list and muxing for the MPC5604P devices.

Each row of Table 5 shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

MPC5604P devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the data sheet's "Pad AC Specifications" section.

Table 5. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIUL FlexPWM_0 DSPI_3 — DSPI_3	I/O O O — I	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIUL — — — ADC_1	Input only	—	—	41	58
Port E(16-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIUL — — — ADC_1	Input only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	42
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	44

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max[1]	
$V_{SS\_LV\_REGCOR}$[4]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[4,5]	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[4]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1 Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.

3 The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV. As long as that condition is met, ADC_0 and ADC_1 can be operated at 5 V with the rest of the device operating at 3.3 V.

4 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.

5 The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

[5] Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic interference (EMI) characteristics

Table 12. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Max)	Unit
V_{EME}	Radiated emissions	Device configuration, test conditions and EM testing per standard IEC61967-2 Supply voltage = 5 V DC Ambient temperature = 25 °C Worst-case orientation	f_{OSC} 8 MHz f_{CPU} 64 MHz No PLL frequency modulation	150 kHz–150 MHz	16	dBµV
				150–1000 MHz	15	
				IEC Level	M	—
			f_{OSC} 8 MHz f_{CPU} 64 MHz 1% PLL frequency modulation	150 kHz–150 MHz	15	dBµV
				150–1000 MHz	14	
				IEC Level	M	—

3.7 Electrostatic discharge (ESD) characteristics

Table 13. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

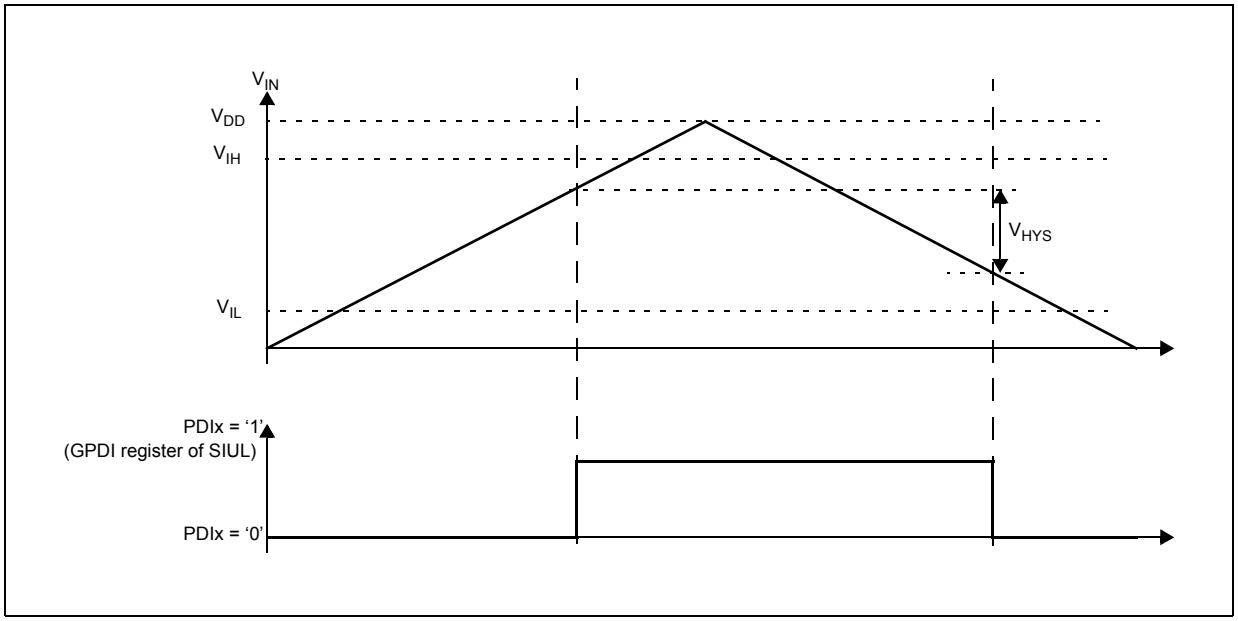

Figure 13. Input DC electrical characteristics definition

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 23.

Table 23. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
144 LQFP	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
100 LQFP	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 24 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 24. I/O weight

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—
PAD[85]	9%	7%	—	—

Table 24. I/O weight (continued)

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 24. I/O weight (continued)

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%
PAD[102]	11%	10%	—	—

Table 24. I/O weight (continued)

Pad	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[13]	10%	9%	12%	11%
PAD[82]	10%	9%	—	—
PAD[22]	10%	9%	13%	12%
PAD[83]	10%	9%	—	—
PAD[50]	10%	9%	14%	12%
PAD[97]	10%	9%	—	—
PAD[38]	10%	9%	14%	13%
PAD[14]	9%	8%	14%	13%
PAD[15]	9%	8%	15%	13%

Table 25. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(2)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}(2)	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	

3.13 16 MHz RC oscillator electrical characteristics

Table 30. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

[1] PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit successive approximation register (SAR) analog-to-digital converter.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.

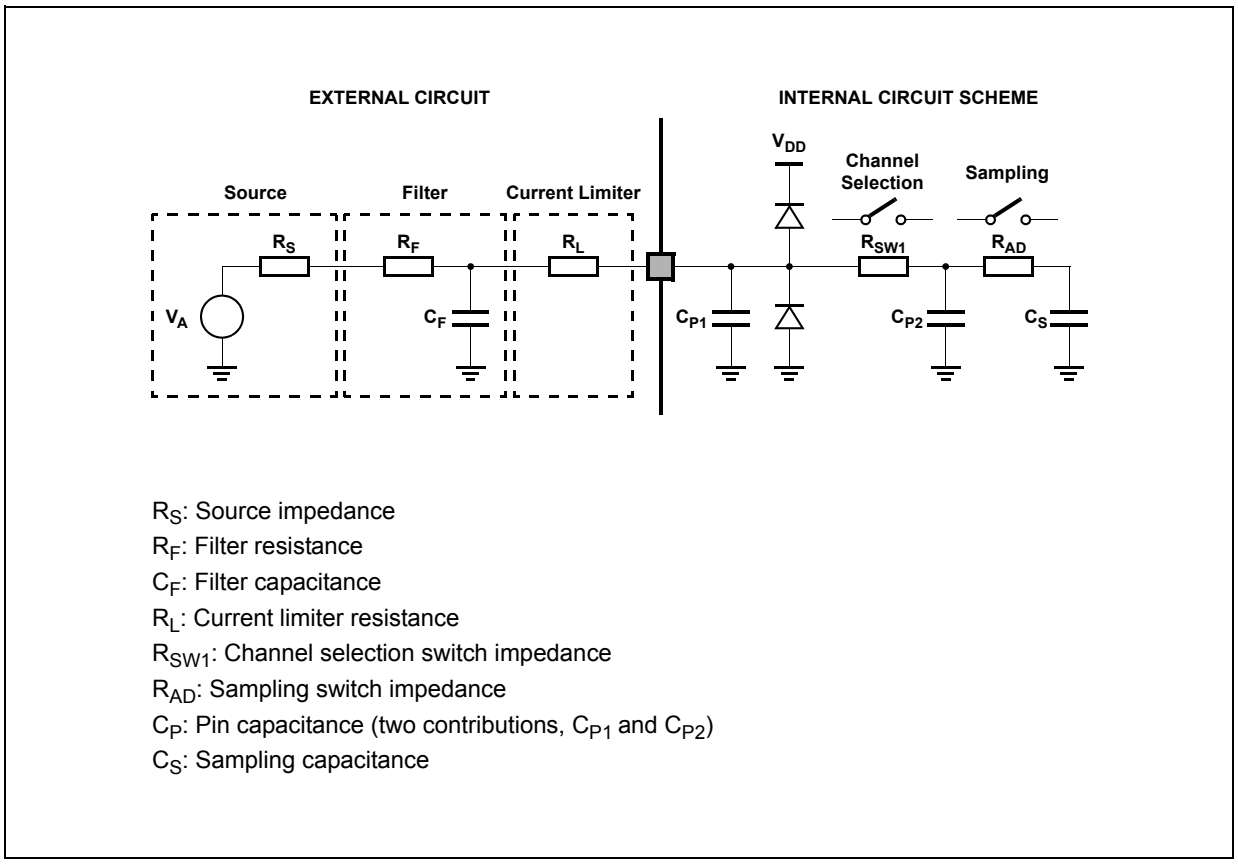

Figure 15. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 15): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

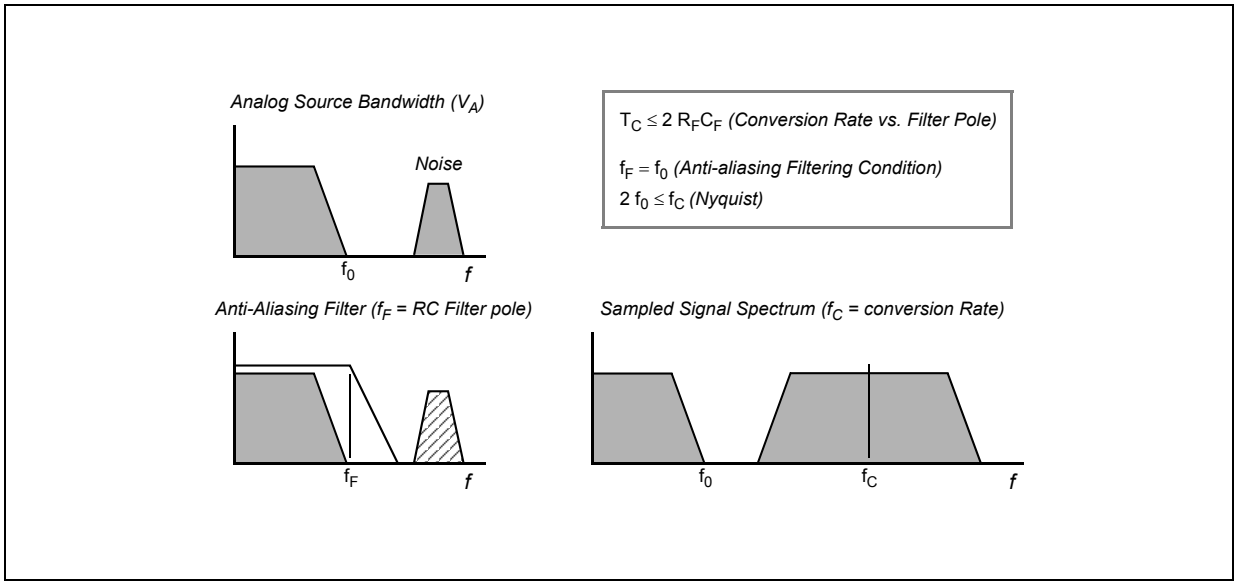

Figure 17. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Table 31. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
R_{SW1}[10]	—	D	Internal resistance of analog source	$V_{DD\_HV\_ADC}$ = 5 V ± 10%	—	—	0.6	kΩ
				$V_{DD\_HV\_ADC}$ = 3.3 V ± 10%	—	—	3	kΩ
R_{AD}[10]	—	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	—	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	CC	P	Integral non-linearity	No overload	–1.5	—	1.5	LSB
DNL	CC	P	Differential non-linearity	No overload	–1.0	—	1.0	LSB
OSE	CC	T	Offset error	—	—	±1	—	LSB
GE	CC	T	Gain error	—	—	±1	—	LSB
TUE	CC	P	Total unadjusted error without current injection	—	–2.5	—	2.5	LSB
TUE	CC	T	Total unadjusted error with current injection	—	–3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_ADCx}$ to $V_{DD\_HV\_ADCx}$.

2 V_{AINx} may exceed $V_{SS\_HV\_AD}$ and $V_{DD\_HV\_AD}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

3 Not allowed to refer this voltage to $V_{DD\_HV\_ADV1}$, $V_{SS\_HV\_ADV1}$

4 Not allowed to refer this voltage to $V_{DD\_HV\_ADV0}$, $V_{SS\_HV\_ADV0}$

5 AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

6 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.

7 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

8 This parameter includes the sample time t_{ADC_S}.

9 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

10 See Figure 15.

4 Package characteristics

4.1 Package mechanical data

4.1.1 144 LQFP mechanical outline drawing

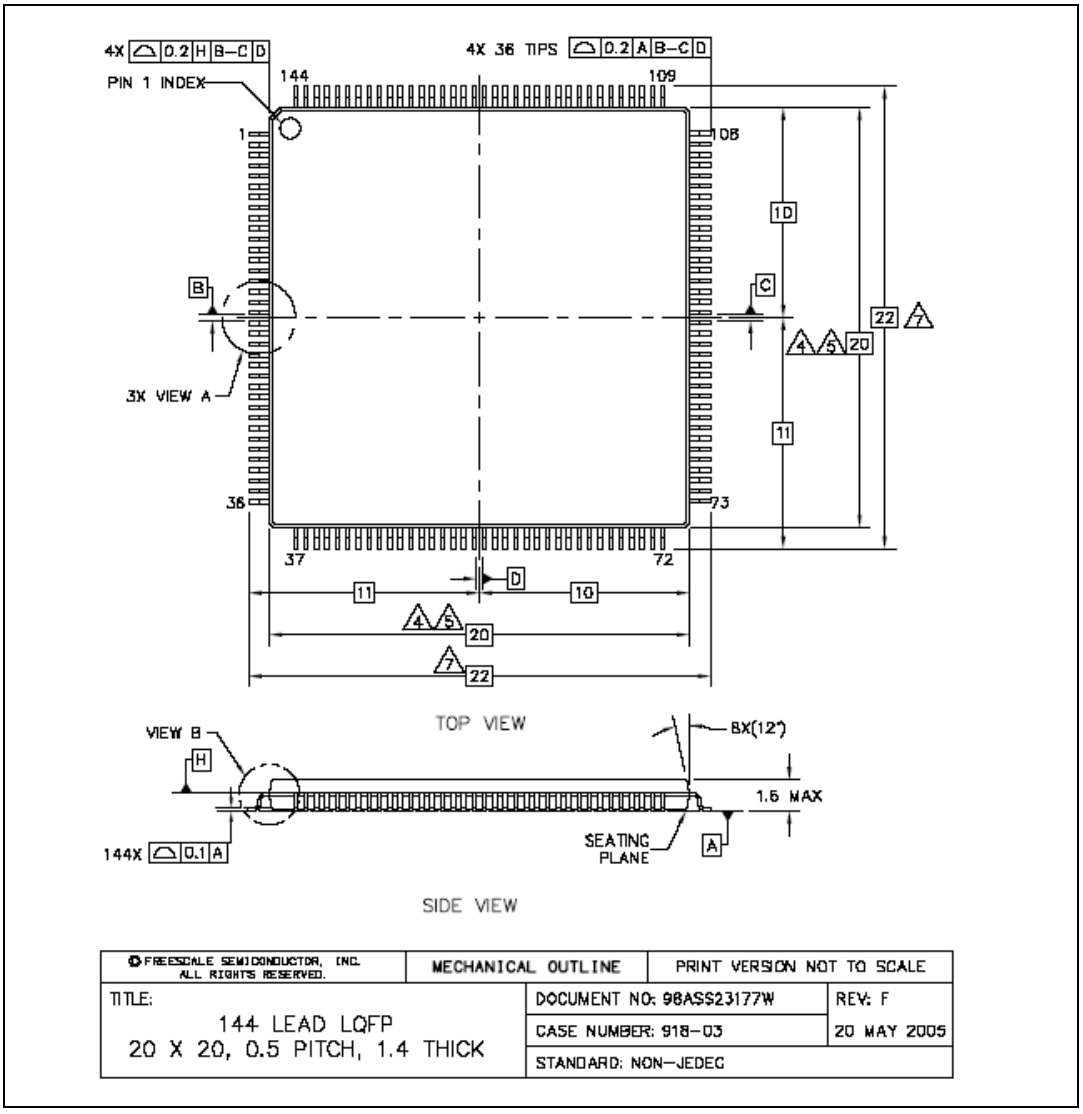

Figure 37. 144 LQFP package mechanical drawing (part 1)

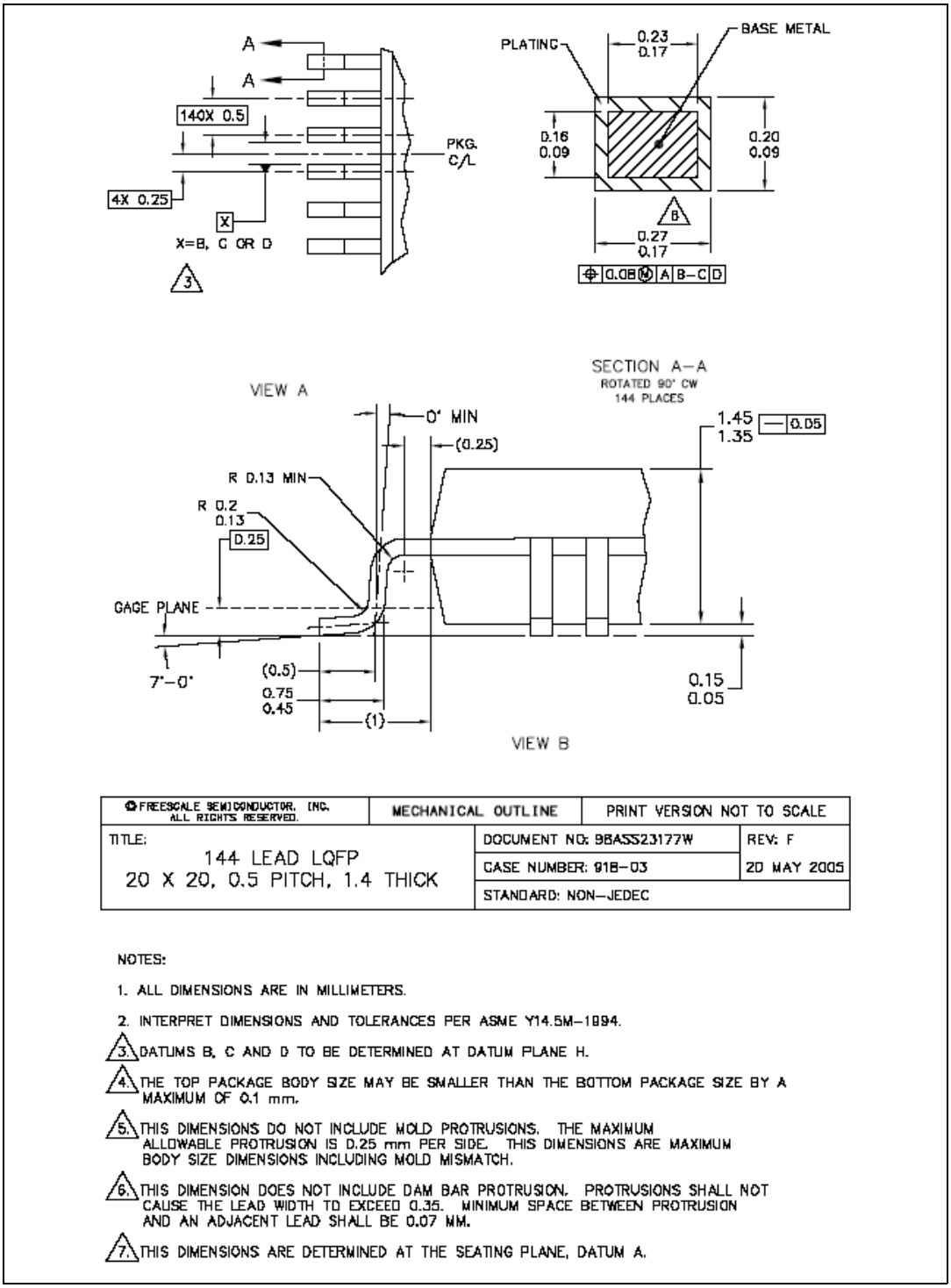

Figure 38. 144 LQFP package mechanical drawing (part 2)

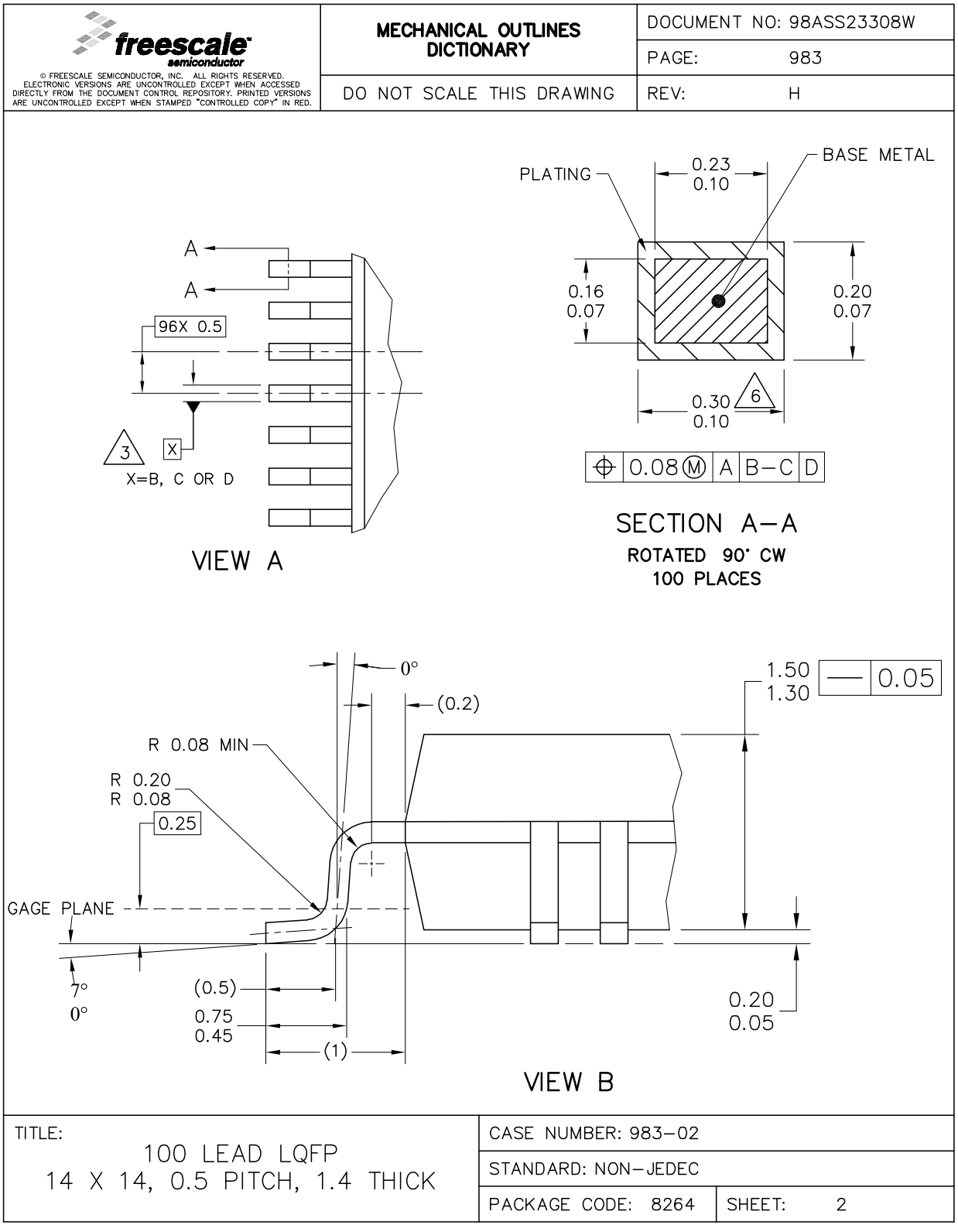

Figure 40. 100 LQFP package mechanical drawing (part 2)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3

Figure 41. 100 LQFP package mechanical drawing (part 3)

6 Document revision history

Table 42 summarizes revisions to this document.

Table 42. Revision history

Revision	Date	Substantive changes
Rev. 1	Aug 2008	Initial release
Rev. 2	Nov 2008	Table 5: TDO and TDI pins (Port pins B[4:5] are single function pins. Table 10, Table 11: Thermal characteristics added. Table 11, Table 12: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 16, Table 17, Table 19, Table 20: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 21: • Values for I_{OL} and I_{OH} (in Conditions column) changed. • Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. • V_{ILR} max value changed. • I_{PUR} min and max values changed. Table 27: Sensitivity value changed. Table 30: Most values in table changed.
Rev. 3	Feb 2009	• Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. • Electrical parameters updated. • EMI characteristics are now in one table; values have been updated. • ESD characteristics are now in one table. • Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. • AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted

Table 42. Revision history (continued)

Revision	Date	Substantive changes
Rev. 8	23-May-2012	Section 1.5.4, “Flash memory: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” Figure 42 (Commercial product code structure), replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" Table 7 (Absolute maximum ratings), updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs Table 5 (Pin muxing), changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated Section 3.8.1, “Voltage regulator electrical characteristics Added Table 25 (I/O consumption) Section 3.10, DC electrical characteristics: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” Table 19 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)), added IPU row for $\overline{\text{RESET}}$ pin Table 21 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)), added IPU row for $\overline{\text{RESET}}$ pin Table 31 (ADC conversion characteristics), added V_{INAN} entry Removed “Order codes” table