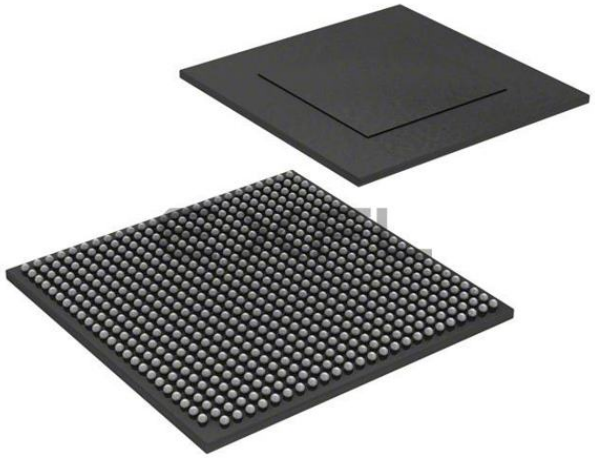

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d4avt08adr

- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

1.3 Updated Signal Naming Convention

The signal names of the i.MX 6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, etc.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4.1.10 HDMI Maximum Power Consumption

Table 13 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 13. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 100, "21 x 21 mm Functional Contact Assignments," on page 149.
- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REXT, SATA_PHY_RX_N, SATA_PHY_RX_P, and SATA_PHY_TX_N) can be left floating. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.
- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can be left floating. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 18. MLB PLL Electrical Parameters

Parameter	Value
Lock time	<1.5 ms

4.4.6 ARM PLL

Table 19. ARM PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

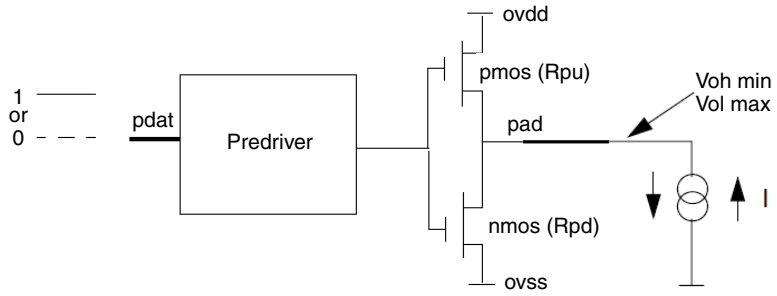

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 21 shows the DC parameters for the clock inputs.

Table 21. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
Startup current	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15msec with a driven 32KHz RTC clock @ 1.1V. This current draw is present even if an external clock source directly drives XTALI	—	—	600	uA
DC input current	I_{XTALI_DC}	—	—	—	2.5	uA

Table 40. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE4	Clock rise to address valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE9	Clock rise to EIM_WE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

4 Refer to JEDEC DDR3 SDRAM Standards for Data Setup (tDS), Hold (tDH) and Slew Rate Derating tables.

Figure 26 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram appear in Table 44.

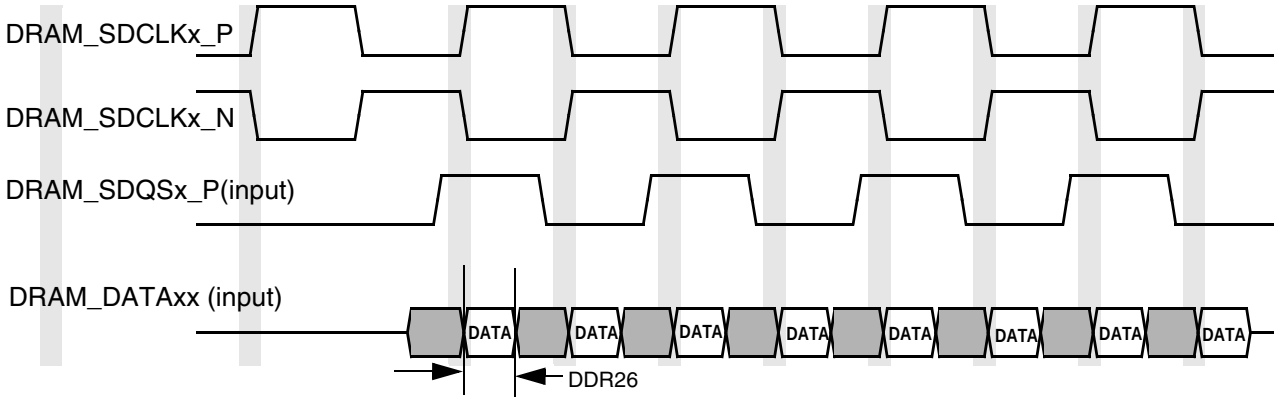

Figure 26. DDR3/DDR3L Read Cycle

4.9.4.2 LPDDR2 Parameters

Table 44. DDR3/DDR3L Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DRAM_DATAxx valid window width.	—	450	—	ps

1 To receive the reported setup and hold values, the read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 27 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 45.

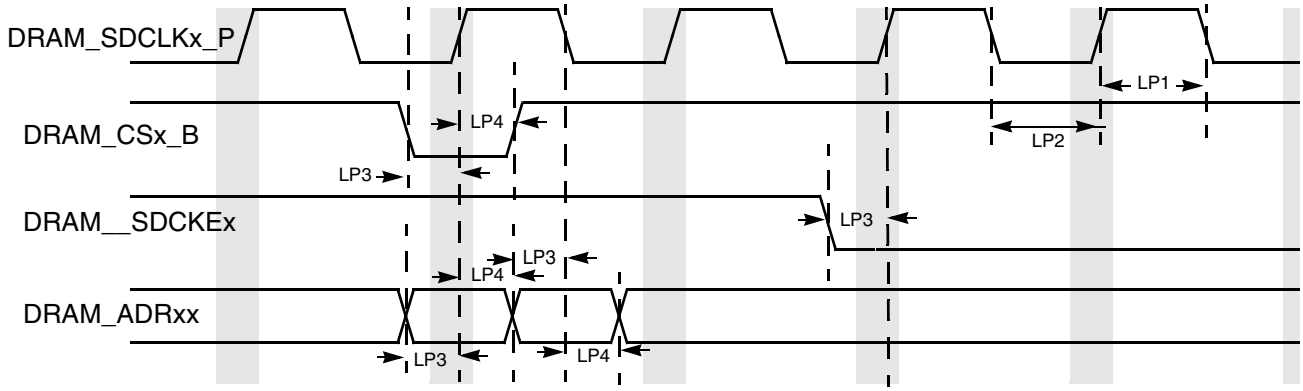

Figure 27. LPDDR2 Command and Address Timing Diagram

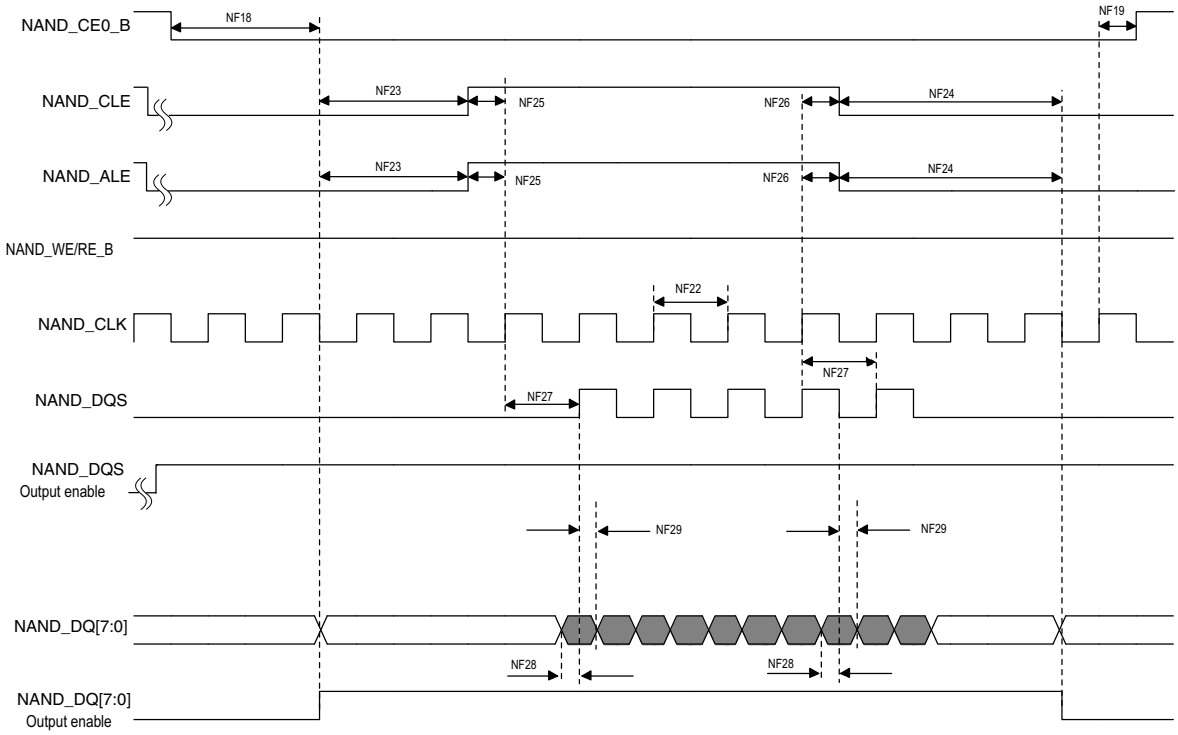

Figure 36. Source Synchronous Mode Data Write Timing Diagram

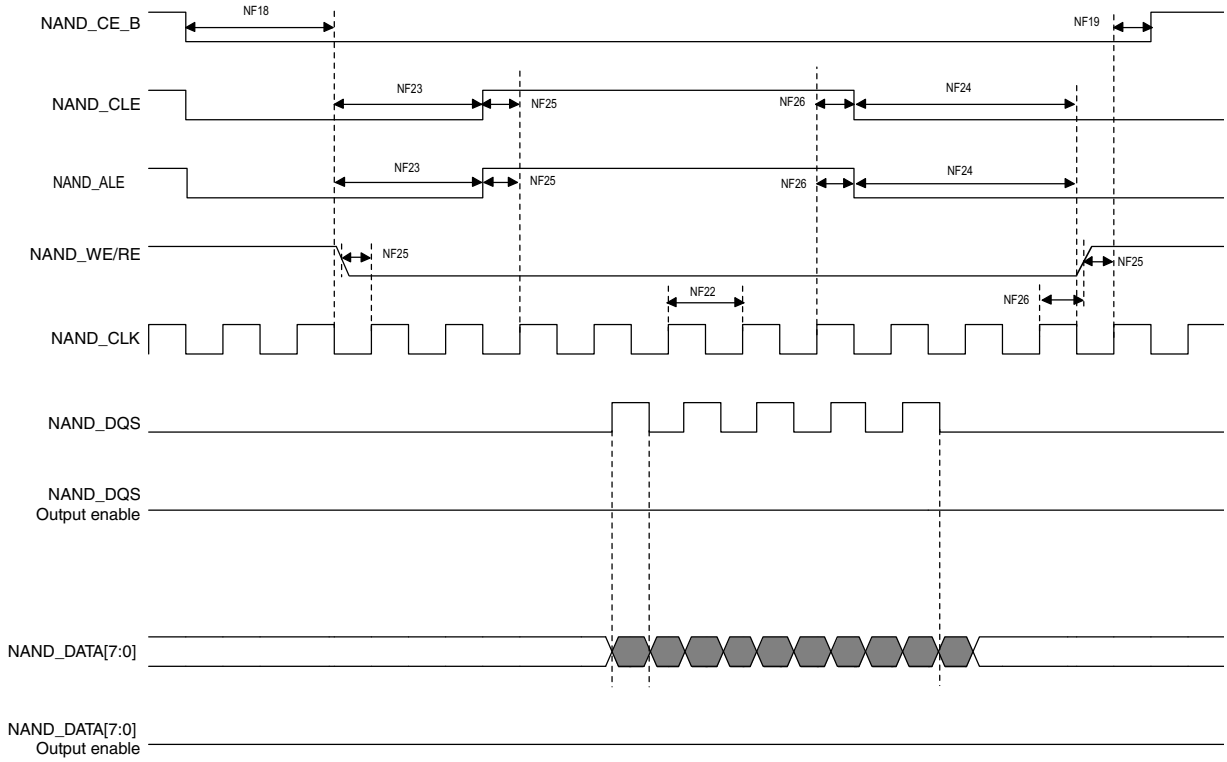

Figure 37. Source Synchronous Mode Data Read Timing Diagram

Table 54. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 46 depicts the timing of eMMC4.4/4.41. Table 55 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

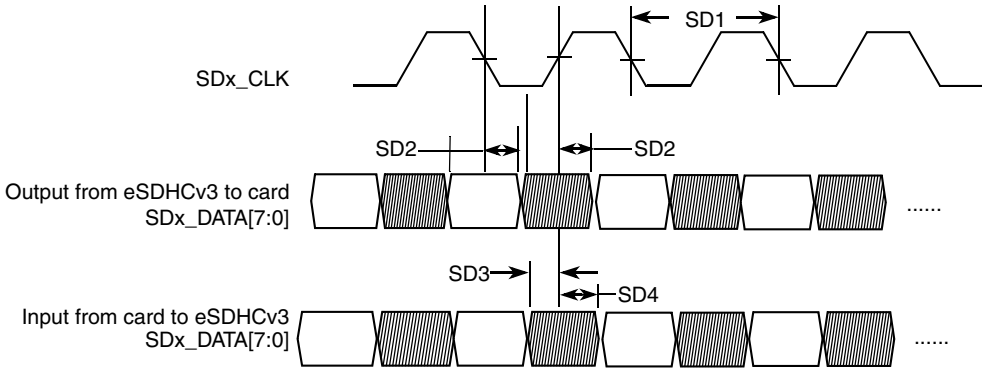

Figure 46. eMMC4.4/4.41 Timing

Table 55. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 62. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

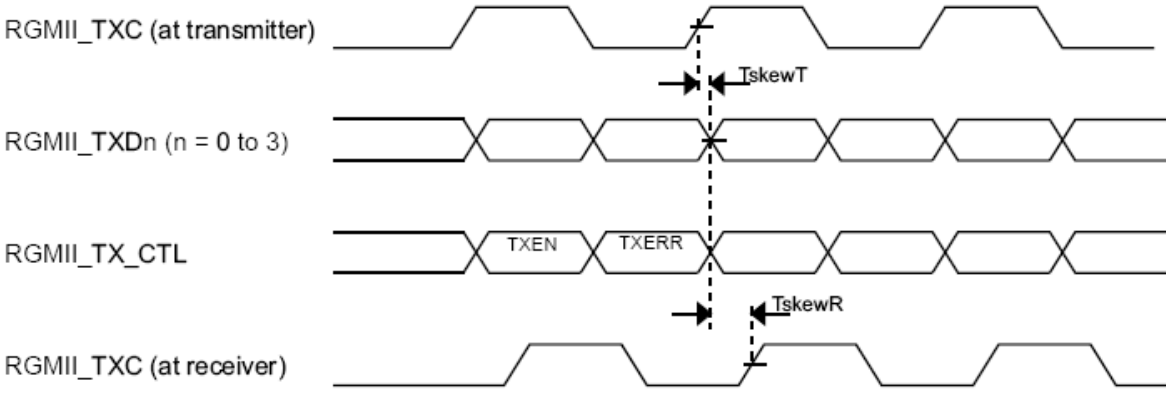

Figure 53. RGMII Transmit Signal Timing Diagram Original

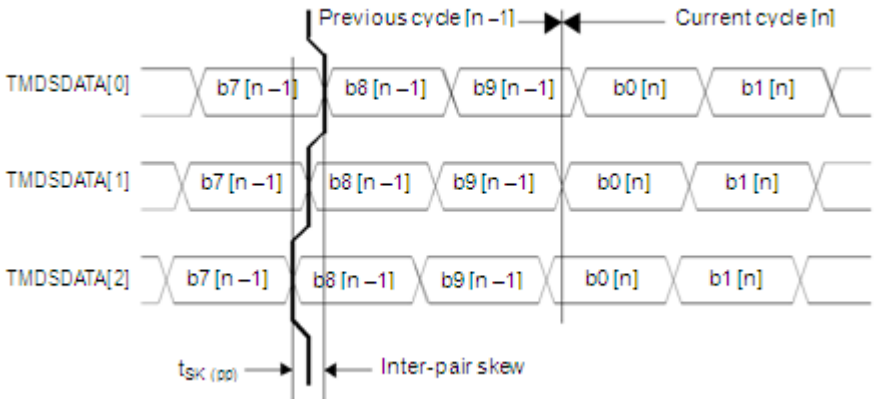

Figure 62. Inter-Pair Skew Definition

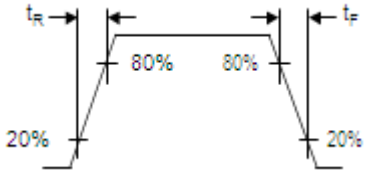

Figure 63. TMDS Output Signals Rise and Fall Time Definition

Table 64. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 59.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 59.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 59.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 59.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 61.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 62.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 63.	75	—	0.4 UI	ps

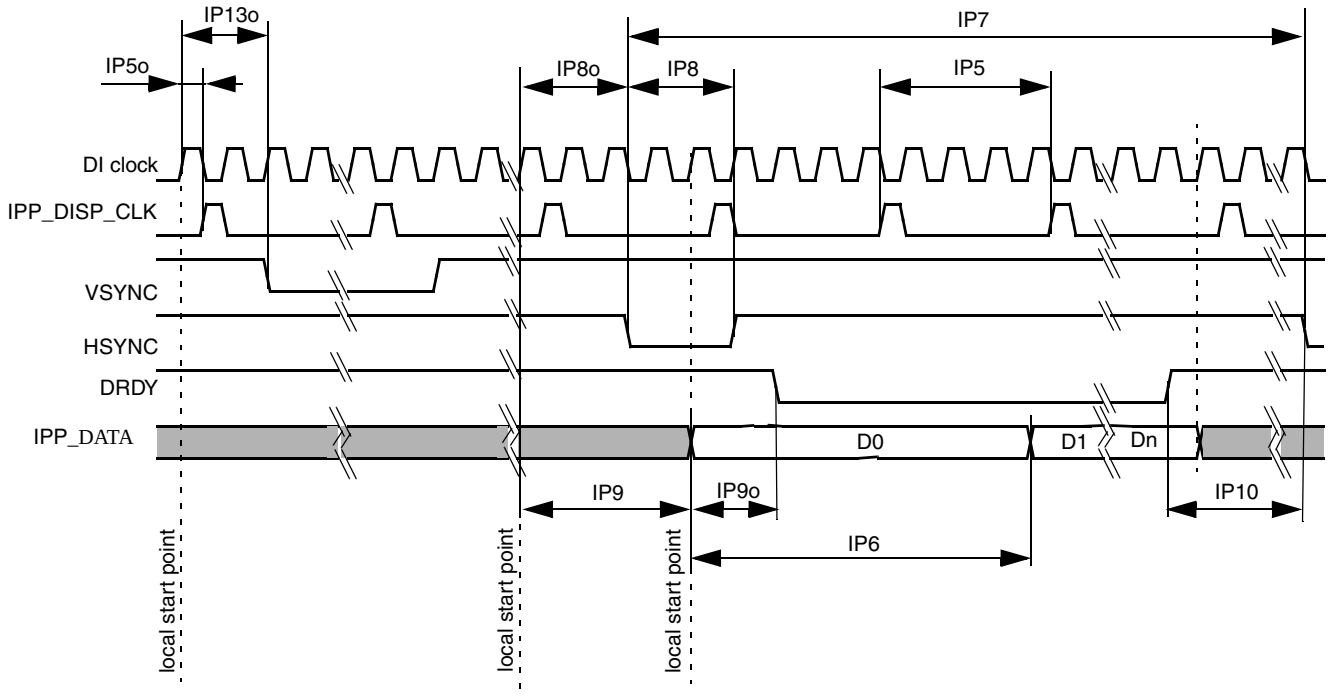

Figure 69. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 70 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

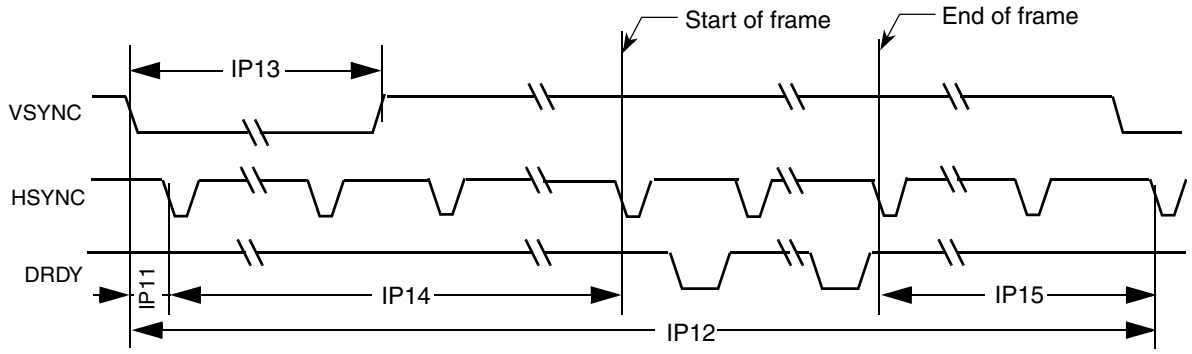

Figure 70. TFT Panels Timing Diagram—Vertical Sync Pulse

4.11.13.3 Receiver Real-Time Data Flow

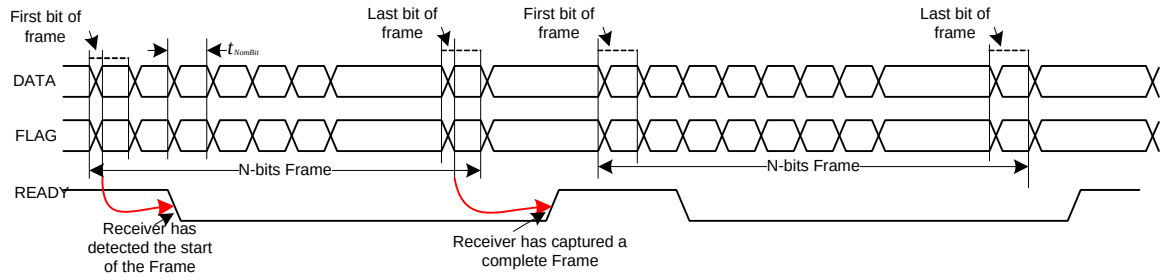

Figure 81. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

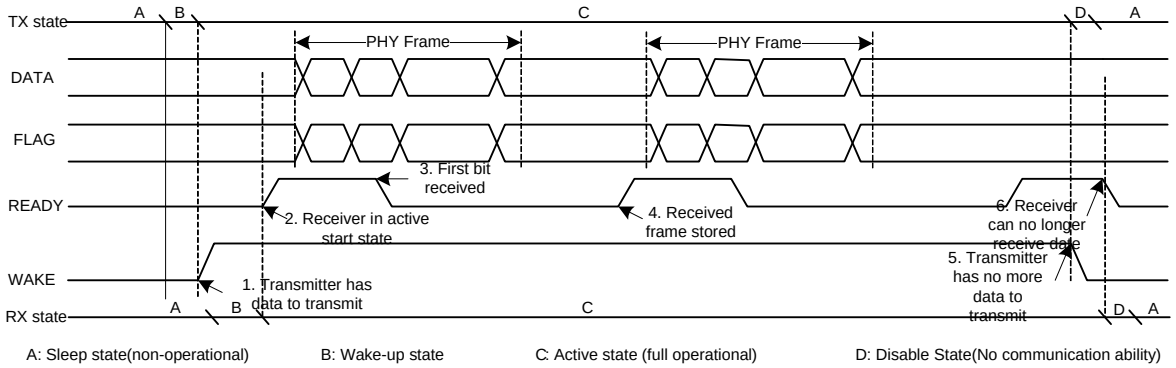

Figure 82. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

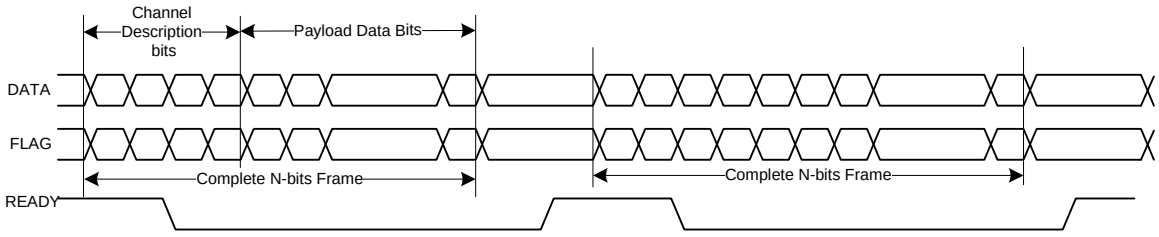

Figure 83. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.17.1.1 SATA PHY Transmitter Characteristics

Table 81 provides specifications for SATA PHY transmitter characteristics.

Table 81. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.11.17.1.2 SATA PHY Receiver Characteristics

Table 82 provides specifications for SATA PHY receiver characteristics.

Table 82. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.11.17.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.11.18 SCAN JTAG Controller (SJC) Timing Parameters

Figure 90 depicts the SJC test clock input timing. Figure 91 depicts the SJC boundary scan timing. Figure 92 depicts the SJC test access port. Figure 93 depicts the JTAG_TRST_B timing. Signal parameters are listed in Table 83.

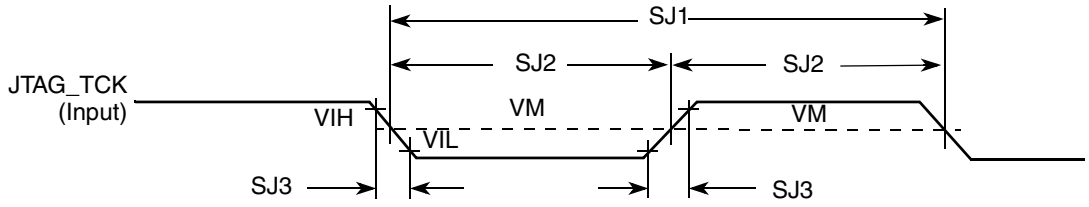

Figure 90. Test Clock Input Timing Diagram

4.11.21.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.21.2.1 UART Transmitter

Figure 100 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 91 lists the UART RS-232 serial mode transmit timing characteristics.

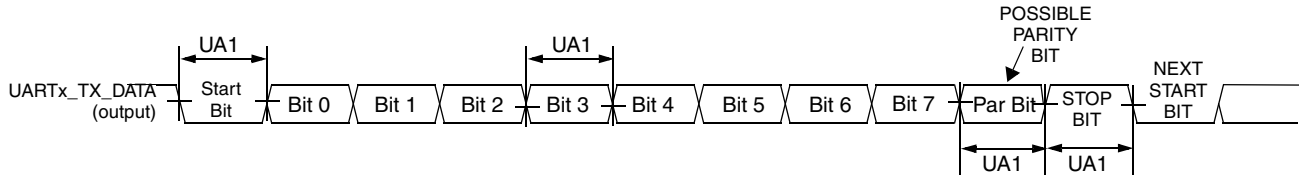

Figure 100. UART RS-232 Serial Mode Transmit Timing Diagram

Table 91. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.11.21.2.2 UART Receiver

Figure 101 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 92 lists serial mode receive timing characteristics.

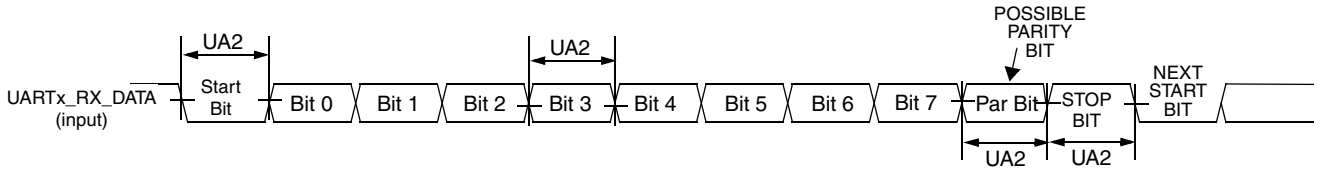

Figure 101. UART RS-232 Serial Mode Receive Timing Diagram

Table 92. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 99. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	—

Table 100 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 100. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)
CLK1_N	C7	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	—	—	CSI_DATA1_N	—	—
CSI_D1P	D2	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	E1	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	E2	NVCC_MIPI	—	—	CSI_DATA2_P	—	—
CSI_D3M	F2	NVCC_MIPI	—	—	CSI_DATA3_N	—	—

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