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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6d4avt10ac

1.1 Ordering Information

Table 1shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed[1] Grade	Temperature Grade	Package
MCIMX6Q6AVT10AC	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT10AD	i.MX 6Quad	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AC	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT10AD	i.MX 6Quad	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AC	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q6AVT08AD	i.MX 6Quad	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AC	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6Q4AVT08AD	i.MX 6Quad	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AC	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT10AD	i.MX 6Dual	With VPU, GPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AC	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT10AD	i.MX 6Dual	With GPU, no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AC	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D6AVT08AD	i.MX 6Dual	With VPU, GPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AC	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive1	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6D4AVT08AD	i.MX 6Dual	With GPU, no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

[1] If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

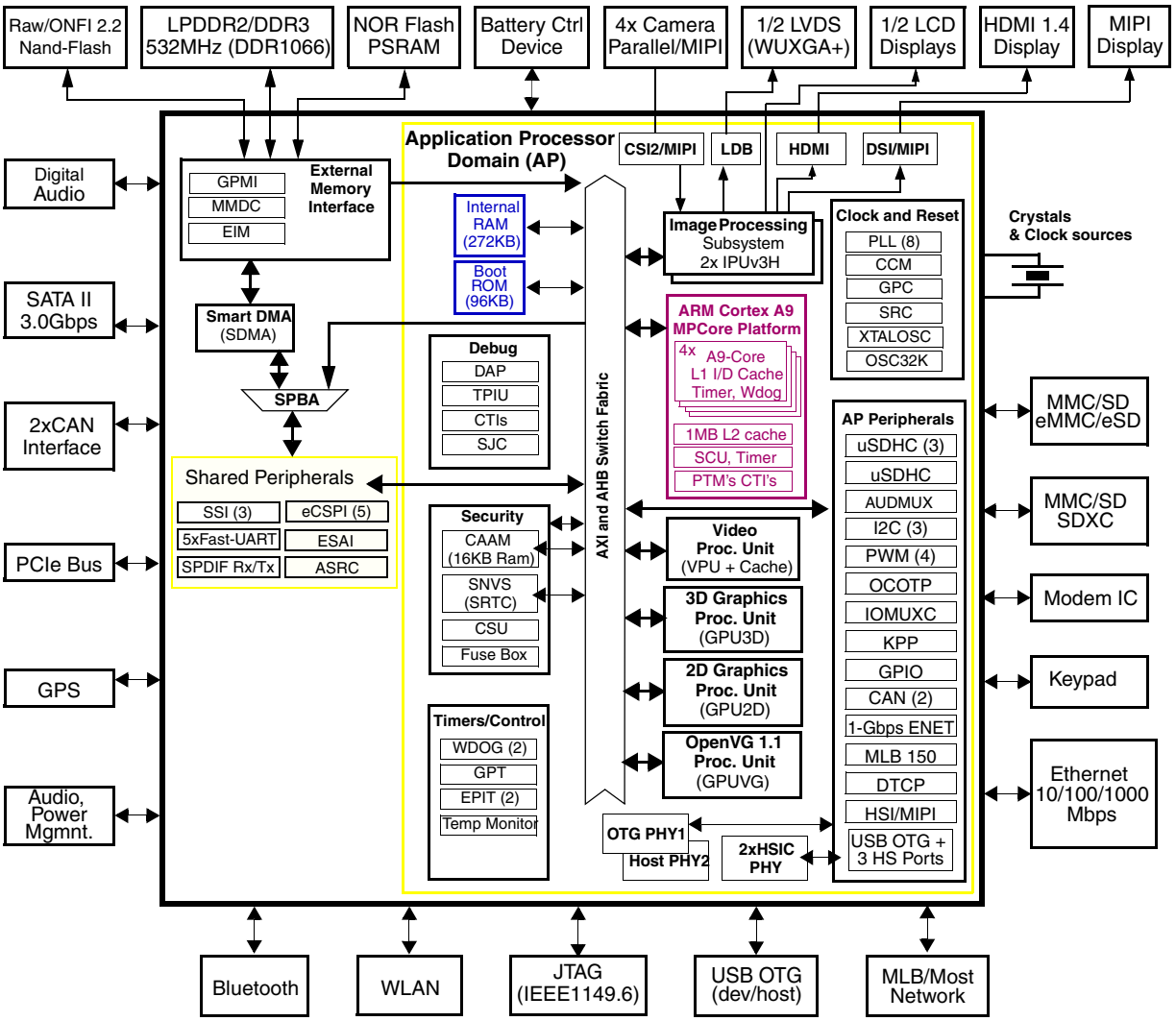


Figure 2. i.MX 6Dual/6Quad Automotive Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU2Dv4	Graphics Processing Unit, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the SoC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX 6Dual/6Quad Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 19
FCPBGA Package Thermal Resistance	on page 20
Operating Ranges	on page 21
External Clock Sources	on page 23
Maximum Supply Currents	on page 25
Low Power Mode Supply Currents	on page 26
USB PHY Current Consumption	on page 28
SATA Typical Power Consumption	on page 28
PCIe 2.0 Maximum Power Consumption	on page 30
HDMI Maximum Power Consumption	on page 31

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.5	V
Internal supply voltages	VDD_ARM_CAP VDD_ARM23_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The parameters in Table 23 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 23. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9 × OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1 × OVDD	V
Input reference voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)	—	0.26	See Note [2]	—
Differential Input Logic Low	Vil(diff)	—	See Note [2]	-0.26	—
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	µA
Pull-up/pull-down impedance mismatch	MMpupd	—	-15	+15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 29).

4.6.3.2 DDR3/DDR3L Mode I/O DC Parameters

The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 24 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 24. DDR3/DDR3L I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA Voh (DSE = 001)	0.8 × OVDD[1]	—	V
		Ioh = -1 mA Voh (for all except DSE = 001)			
Low-level output voltage	Vol	Iol = 0.1 mA Vol (DSE = 001)	—	0.2 × OVDD	V
		Iol = 1 mA Vol (for all except DSE = 001)			
Input reference voltage	Vref[2]	—	0.49 × OVDD	0.51 × OVDD	
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 35 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 35. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.8.4 MLB 6-Pin I/O Differential Output Impedance

Table 36 shows MLB 6-pin I/O differential output impedance of i.MX 6Dual/6Quad processors.

Table 36. MLB 6-Pin I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Z_O	—	1.6	—	—	kΩ

1 To receive the reported setup and hold values, the write calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 29 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 47.

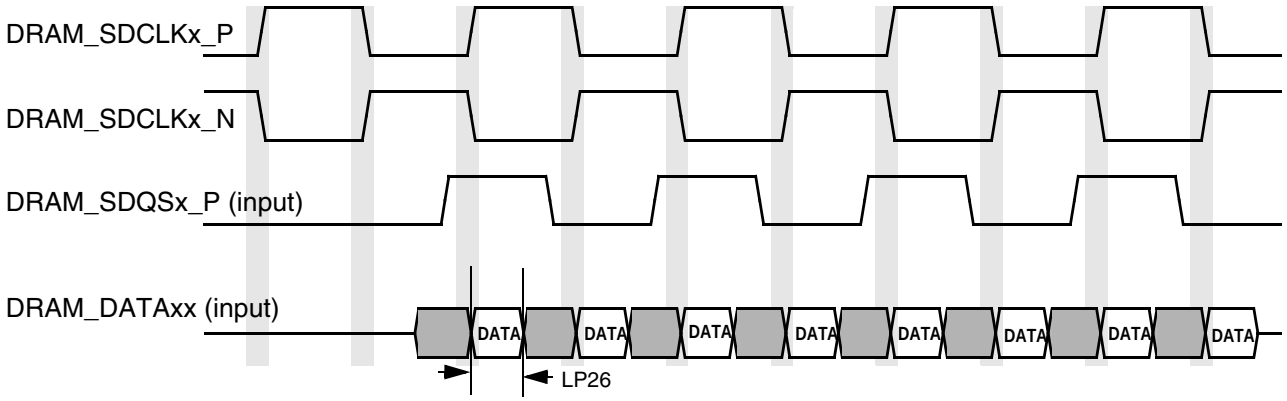


Figure 29. LPDDR2 Read Cycle

Table 47. LPDDR2 Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2	—	250	—	ps

1 To receive the reported setup and hold values, read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

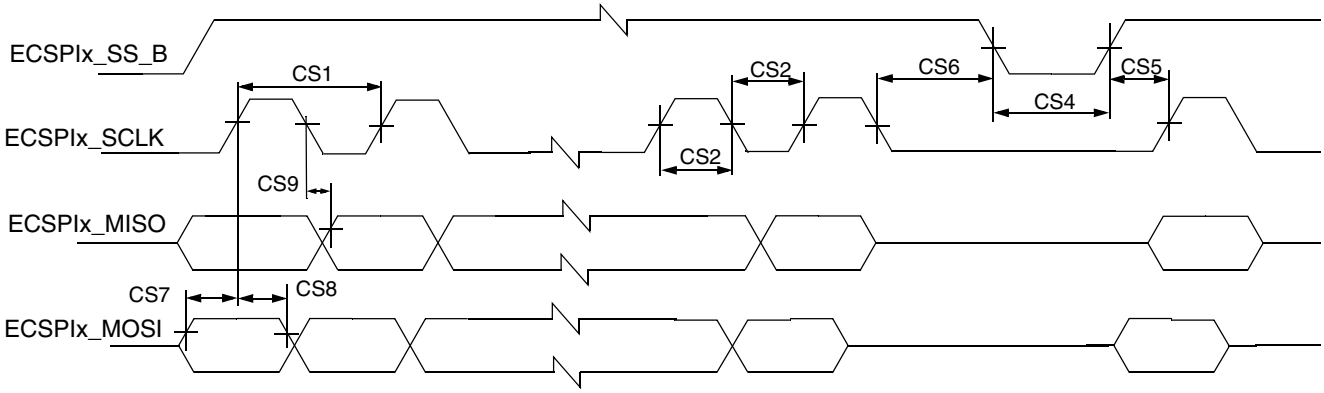
3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.11.2.2 ECSPI Slave Mode Timing

Figure 42 depicts the timing of ECSPI in slave mode and Table 52 lists the ECSPI slave mode timing characteristics.



Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 42. ECSPI Slave Mode Timing Diagram

Table 52. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

[1] ECSPI slow includes:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

[2] ECSPI fast includes:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 45 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

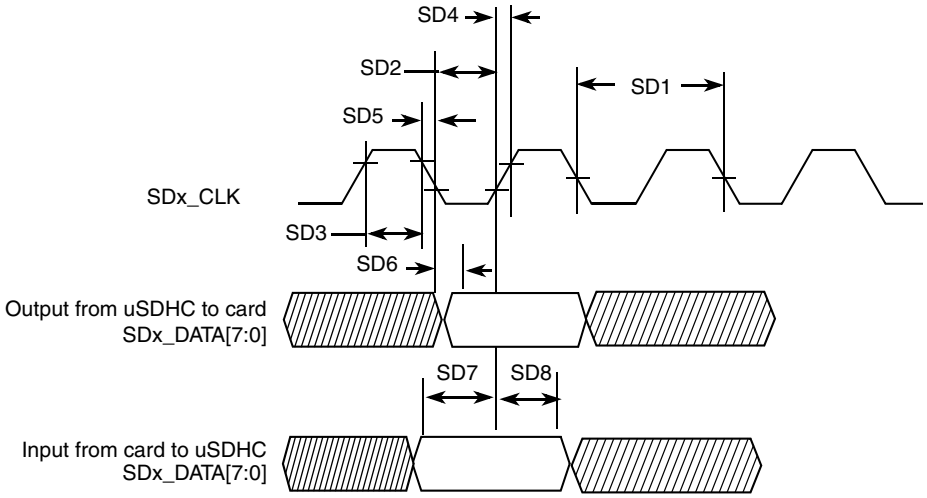


Figure 45. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 62. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

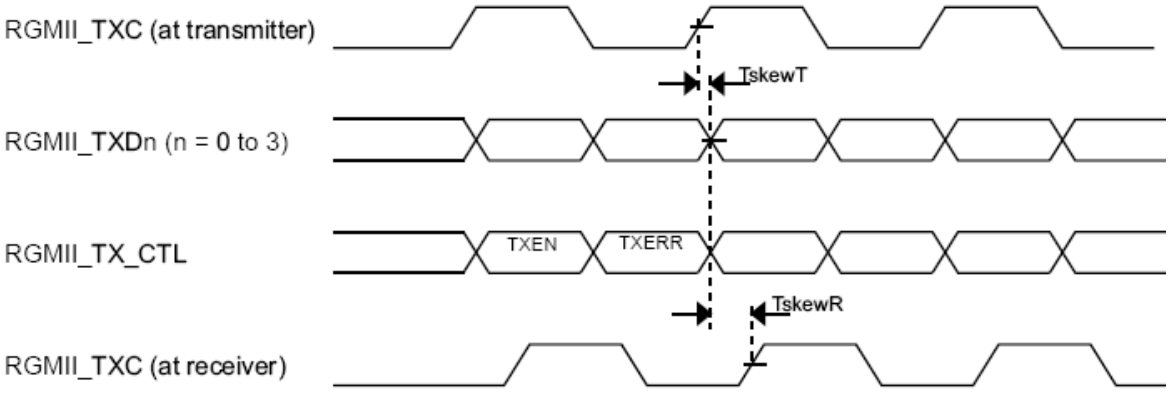


Figure 53. RGMII Transmit Signal Timing Diagram Original

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.”

Table 71. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and I/O supply voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 72. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications—Apply to DSI_CLK_P/_N and DSI_DATA_P/_N Inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

Table 73. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Drivers AC Specifications						
t_{rlp},t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}	—	30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—	—	—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—	—	ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load Resistance	—	80	100	125	Ω

Table 87. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.20.3 SSI Transmitter Timing with External Clock

Figure 98 depicts the SSI transmitter external clock timing and Table 88 lists the timing parameters for the transmitter timing with the external clock.

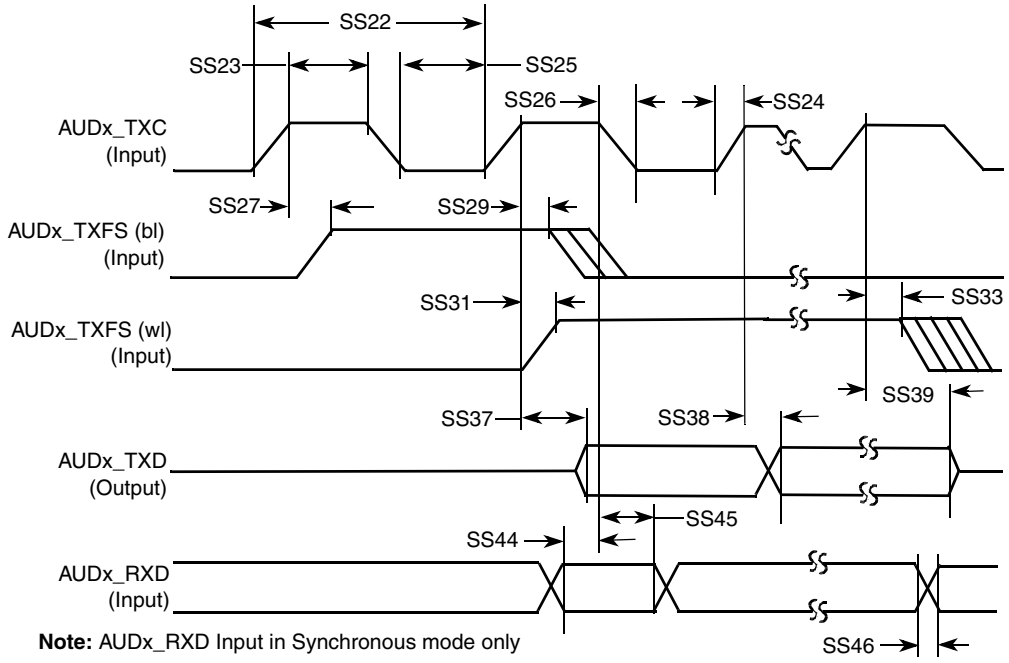


Figure 98. SSI Transmitter External Clock Timing Diagram

Table 88. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 97. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

1 Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 98 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 98. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	0
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	0
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH	—	—	SATA_PHY_RX_N	—	—
SATA_RXP	B14	SATA_VPH	—	—	SATA_PHY_RX_P	—	—
SATA_TXM	B12	SATA_VPH	—	—	SATA_PHY_TX_N	—	—
SATA_TXP	A12	SATA_VPH	—	—	SATA_PHY_TX_P	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100K)
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100K)