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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6d4avt10acr

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 6.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps

- Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)
- MLB (MediaLB) provides interface to MOST Networks (150 Mbps) with the option of DTCP cipher accelerator

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 150 Mbps). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32/64-bit DDR3-1066 (LV) or LPDDR2-1066 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Support up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controllers.

Optionally LDO_SOC and VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB PHY, LVDS PHY, HDMI PHY, MIPI PHY, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. The LDO_2P5 supplies the SATA PHY, USB PHY, LVDS PHY, HDMI PHY, MIPI PHY, E-fuse module and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output

voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

Table 45. LPDDR2 Timing Parameter

ID	Parameter[1,2]	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	DRAM_SDCLKx_P clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	DRAM_SDCLKx_P clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B, DRAM_ADDRxx setup time	t_{IS}	270	—	ps
LP4	DRAM_CSx_B, DRAM_ADDRxx hold time	t_{IH}	270	—	ps
LP3	DRAM_ADDRxx setup time	t_{IS}	230	—	ps
LP4	DRAM_ADDRxx hold time	t_{IH}	230	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 28 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 46.

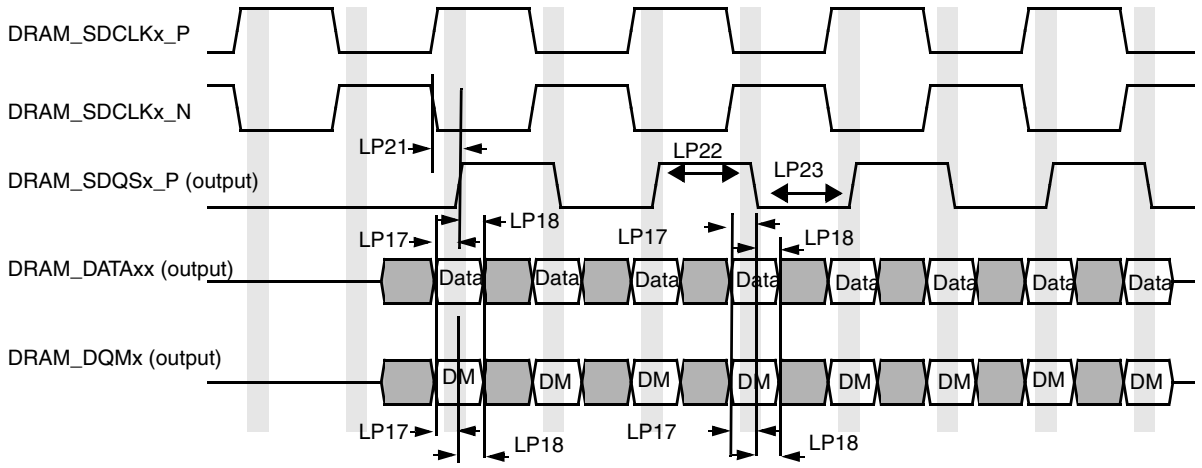

Figure 28. LPDDR2 Write Cycle

Table 46. LPDDR2 Write Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	t_{DS}	235	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	t_{DH}	235	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	t_{DQSS}	0.75	1.25	tCK
LP22	DRAM_SDQSx_P high level width	t_{DQSH}	0.4	—	tCK
LP23	DRAM_SDQSx_P low level width	t_{DQSL}	0.4	—	tCK

1 To receive the reported setup and hold values, the write calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 29 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 47.

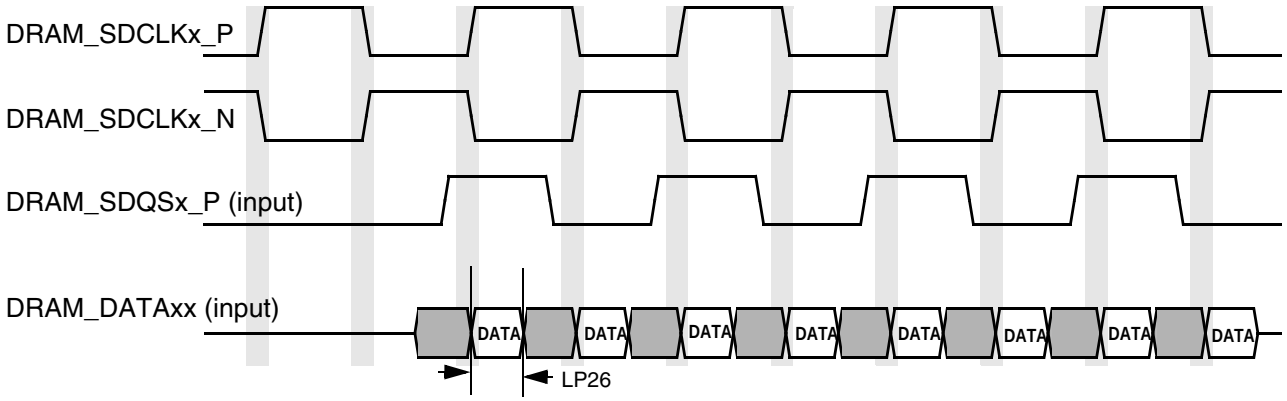

Figure 29. LPDDR2 Read Cycle

Table 47. LPDDR2 Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2	—	250	—	ps

1 To receive the reported setup and hold values, read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.11.4.3 SDR50/SDR104 AC Timing

Figure 47 depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

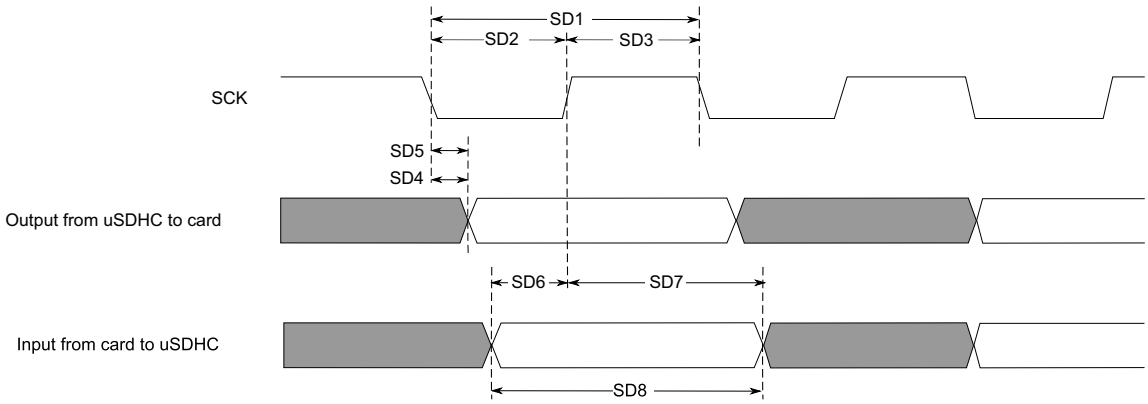

Figure 47. SDR50/SDR104 Timing

Table 56. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3 \times t_{CLK}$	$0.7 \times t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3 \times t_{CLK}$	$0.7 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

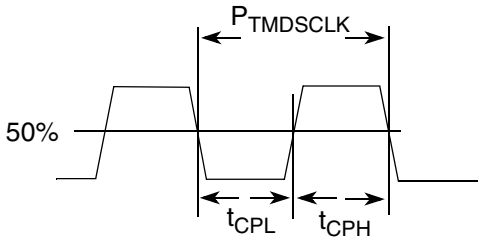

Figure 59. TMDS Clock Signal Definitions

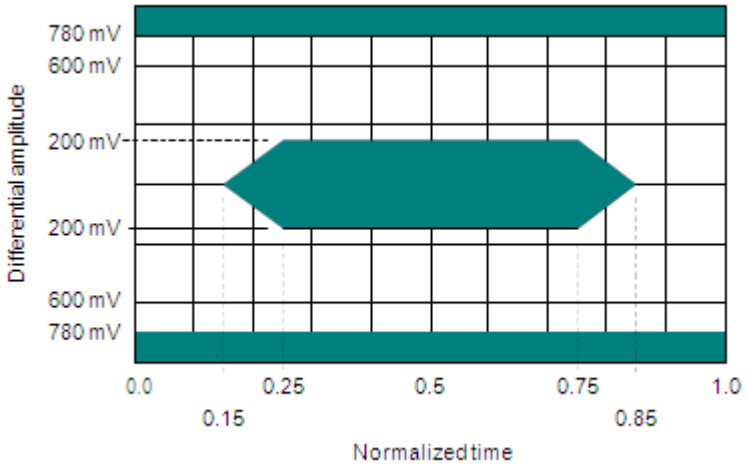

Figure 60. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

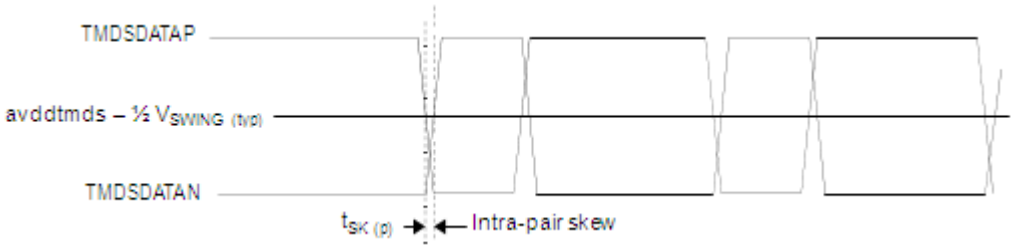

Figure 61. Intra-Pair Skew Definition

Table 65. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 68 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.

Table 72. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.11.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 72 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signalling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

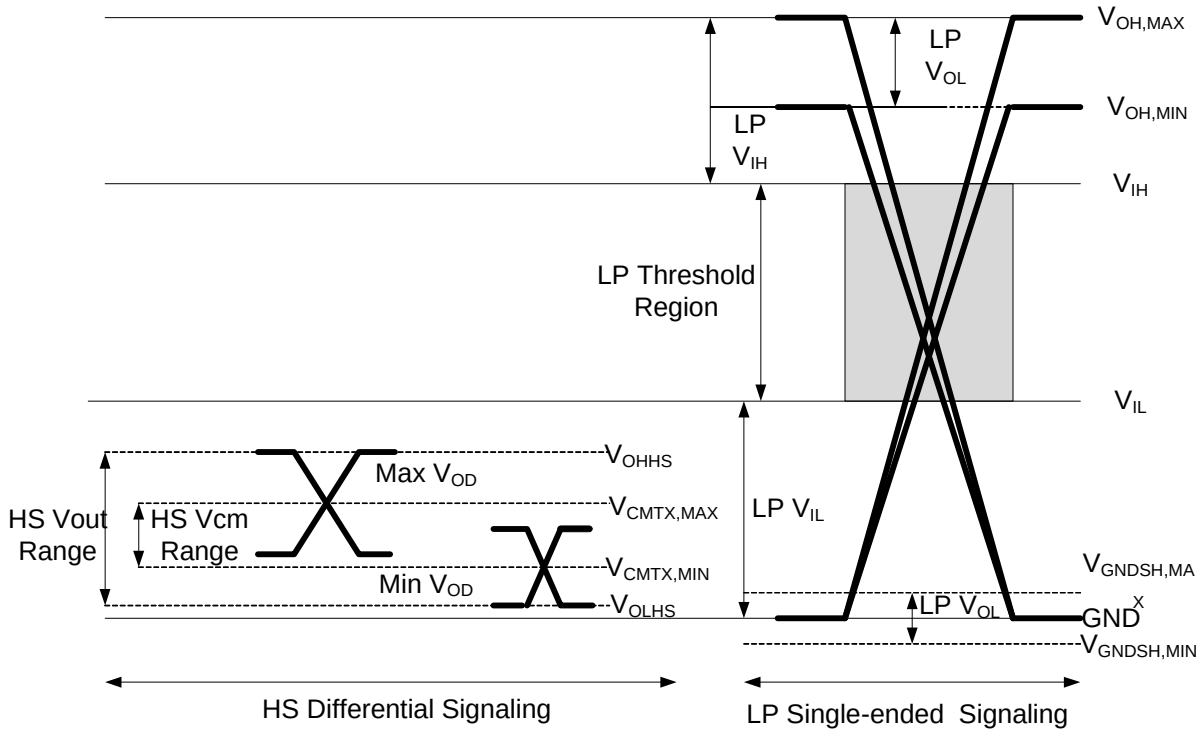

Figure 72. D-PHY Signaling Levels

4.11.12.3 HS Line Driver Characteristics

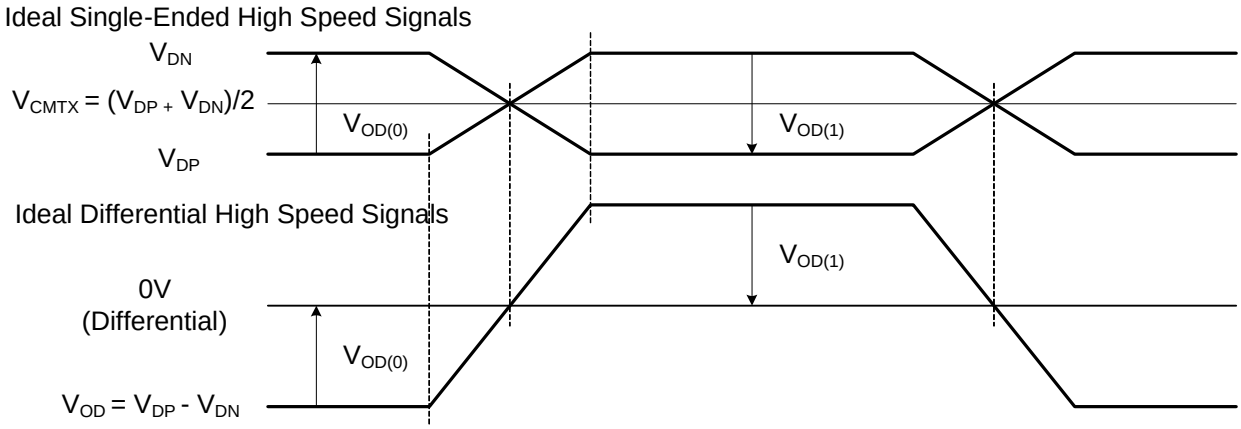

Figure 73. Ideal Single-ended and Resulting Differential HS Signals

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

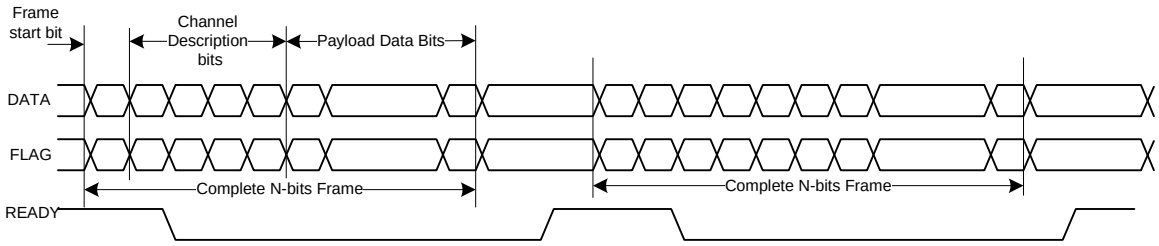

Figure 84. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

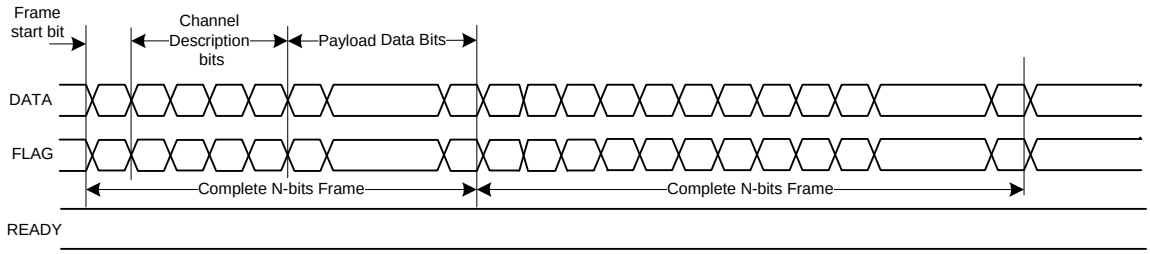

Figure 85. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 74. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

4.11.13.9 DATA and FLAG Signal Timing

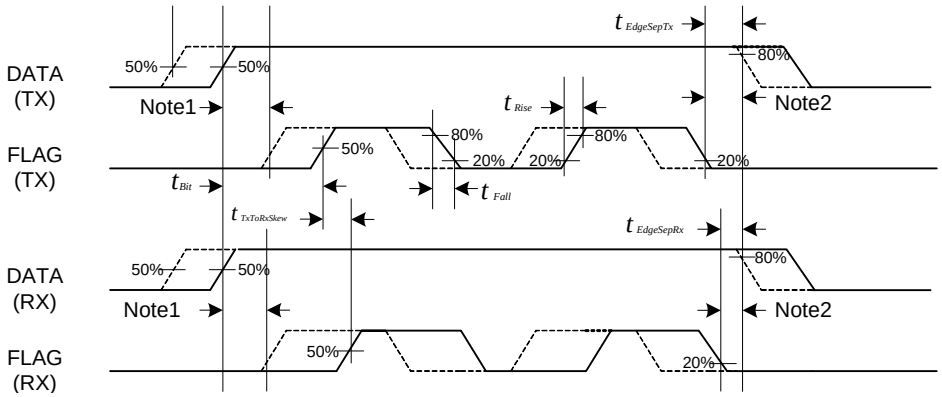

Figure 86. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 75 lists the MediaLB 3-pin interface electrical characteristics.

Table 75. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_L	0 < V_{in} < VDD	—	±10	µA

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 76 lists the MediaLB 6-pin interface electrical characteristics.

Table 76. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): I V_{O+} - V_{O-} I	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: I $V_{OD, high}$ - $V_{OD, low}$ I	ΔV_{OD}	—	-50	50	mV

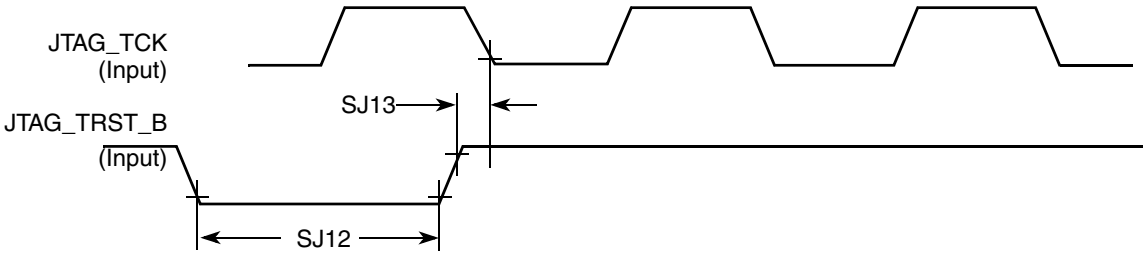

Figure 93. JTAG_TRST_B Timing Diagram

Table 83. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.11.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 84 and Figure 94 and Figure 95 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	PU (100K)
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	PU (100K)
HDMI_CLKM	J5	HDMI_VPH	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	J6	HDMI_VPH	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	K5	HDMI_VPH	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	K6	HDMI_VPH	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	J3	HDMI_VPH	—	—	HDMI_TX_DATA1_N	—	—
HDMI_D1P	J4	HDMI_VPH	—	—	HDMI_TX_DATA1_P	—	—
HDMI_D2M	K3	HDMI_VPH	—	—	HDMI_TX_DATA2_N	—	—
HDMI_D2P	K4	HDMI_VPH	—	—	HDMI_TX_DATA2_P	—	—
HDMI_HPD	K1	HDMI_VPH	—	—	HDMI_TX_HPD	—	—
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	JTAG_MODE	Input	PU (100K)
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	JTAG_TCK	Input	PU (47K)
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	JTAG_TDI	Input	PU (47K)
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	JTAG_TDO	Output	Keeper
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	JTAG_TMS	Input	PU (47K)
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	JTAG_TRST_B	Input	PU (47K)
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO06	Input	PU (100K)
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	GPIO4_IO08	Input	PU (100K)
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO10	Input	PU (100K)
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO12	Input	PU (100K)
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO14	Input	PU (100K)
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO07	Input	PU (100K)
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	GPIO4_IO09	Input	PU (100K)
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	GPIO4_IO11	Input	PU (100K)
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	GPIO4_IO13	Input	PU (100K)
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO15	Input	PD (100K)
LVDS0_CLK_N	V4	NVCC_LVDS_2P5	LVDS	—	LVDS0_CLK_N	—	—
LVDS0_CLK_P	V3	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_CLK_P	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX0_N	—	—
LVDS0_TX0_P	U1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX0_P	Input	Keeper
LVDS0_TX1_N	U4	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX1_N	—	—
LVDS0_TX1_P	U3	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX1_P	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX2_P	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX3_N	—	—

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD	AC	AB	AA	Y
1	GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N
2	DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P
3	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N
4	DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P
5	DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3	GND
6	DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET
7	DRAM_D11	GND	DRAM_D15	DRAM_D16	GND	DRAM_D20
8	DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21
9	DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19
10	DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25
11	DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0
12	DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15
13	DRAM_A5	GND	DRAM_A6	DRAM_A8	GND	DRAM_A7
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1
16	DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0
17	ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32	DRAM_D36
18	DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33	DRAM_D37
19	DRAM_D35	GND	DRAM_D39	DRAM_D38	GND	DRAM_D40
20	DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45	DRAM_D44
21	DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57	DRAM_DQM7
22	DRAM_D49	GND	DRAM_D48	DRAM_D52	GND	DRAM_D59
23	DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61	DRAM_D62
24	DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B	GND
25	GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7	DRAM_D58

Table 103. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Updates throughout for Silicon revision D, include: - Figure 1 Part number nomenclature diagram. - Example Orderable Part Number tables, Table 1 • Feature description for Miscellaneous IPs and interfaces; SSI and ESAI. • Table 2, UART 1–5 description change: programmable baud rate up to 5 MHz. • Table 2, uSDHC 1–4 description change: including SDXC cards up to 2 TB. • Table 6, operating range for Run mode: LDO bypassed, minimum value corrected to 1.150 V. • Table 6, table footnotes, added LDO enabled mode footnote for internal LDO output set points. • Table 61, added table footnote to the Comment heading in the Comment column. • Removed table “On-Chip LDOs and their On-Chip Loads.” • Section 4.1.4, External Clock Sources; added Note, “The internal RTC oscillator does not …”. • Section 4.1.5, reworded second paragraph about the power management IC to explain that a robust thermal design is required for the increased system power dissipation. • Table 8, Maximum Supply Currents: NVCC_RGMII Condition value changed to N=6. • Table 8, Maximum Supply currents: Added row; NVCC_LVDS2P5 • Section 4.2.1 Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1 Power-Up Sequence: removed Note. • Section 4.5.2 OSC32K, second paragraph reworded to describe OSC32K automatic switching. • Section 4.5.2 OSC32K, added Note following second paragraph to caution use of internal oscillator use. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih minimum value to 0.8. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih maximum value to 1.1. • Table 37 Reset Timing Parameters; removed footnote. • Section 4.9.3 External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 40. EIM Bus Timing Parameters; reworded footnotes for clarity. • Table 41. EIM Asynchronous Timing Parameters; removed comment from the Max heading cell. • Table 41. EIM Asynchronous Timing Parameters; reworded footnote 2 for clarity. • Table 61. RMII Signal Timing; parameter M19 Max value relaxed to 13.5 ns. • Table 77. MLB 256/512 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 78. MLB 1024 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 100. Corrected the ALT5 Default Function names. • Figure 106 and Figure 107 21 x 21 mm Lidded Package; updated drawing (Rev D).
Rev. 2.3	07/26 /2013	• Table 100, *21 x 21Functional Contact Assignments*: Restored NANDF_WP_B row and description. • System Timing Parameters Table 37, *Reset timing parameter*, CC1 description clarified, change from: "Duration of SRC_POR_B to be qualified as valid (input slope <= 5 ns)" to: "Duration of SRC_POR_B to be qualified as valid" and added a footnote to the parameter with the following text: "SRC_POR_B rise and fall times must be 5 ns or less." This change was made for clarity and does not represent a specification change.
Rev. 2.2	07/2013	• Editor corrections to revision history links. No technical content changes.
Rev. 2.1	07/2013	• Figure 1, Changed temperature references from Consumer to Commercial. • Table 100, *21 x 21Functional Contact Assignments*: —Removed rows: DRAM_VREF, HDMI_DDCCEC, and HDMI_REF. —Due to a typographical error in revision 2.0, the ball names for rows EIM_DA2 through EIM_DA15 were ordered incorrectly. This has been corrected in revision 2.1. The ball map is correct in both revision 2.0 and 2.1.