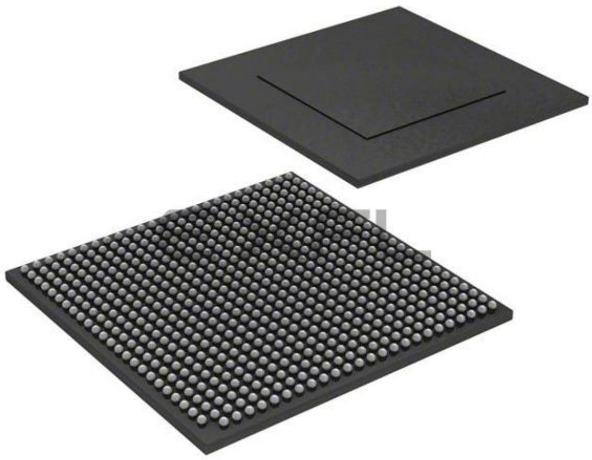

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-A9 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 852MHz |
| Co-Processors/DSP | Multimedia; NEON™ SIMD |
| RAM Controllers | LPDDR2, LVDDR3, DDR3 |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keypad, LCD |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | SATA 3Gbps (1) |
| USB | USB 2.0 + PHY (4) |
| Voltage - I/O | 1.8V, 2.5V, 2.8V, 3.3V |
| Operating Temperature | -40°C ~ 125°C (TJ) |
| Security Features | ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection |
| Package / Case | 624-FBGA, FCBGA |
| Supplier Device Package | 624-FCBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d6avt08acr |

**Table 2. i.MX 6Dual/6Quad Modules List (continued)**

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|---|---|---|---|
| GPU2Dv2 | Graphics Processing Unit-2D, ver. 2 | Multimedia Peripherals | The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions. |
| GPU2Dv4 | Graphics Processing Unit, ver. 4 | Multimedia Peripherals | The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1 |
| GPUVGv2 | Vector Graphics Processing Unit, ver. 2 | Multimedia Peripherals | OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions. |
| HDMI Tx | HDMI Tx interface | Multimedia Peripherals | The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display. |
| HSI | MIPI HSI interface | Connectivity Peripherals | The MIPI HSI provides a standard MIPI interface to the applications processor. |
| $I^2C$-1<br>$I^2C$-2<br>$I^2C$-3 | $I^2C$ Interface | Connectivity Peripherals | $I^2C$ provide serial interface for external devices. Data rates of up to 400 kbps are supported. |
| IOMUXC | IOMUX Control | System Control Peripherals | This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable. |
| IPUv3H-1<br>IPUv3H-2 | Image Processing Unit, ver. 3H | Multimedia Peripherals | IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation.<br>The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces:<br>• Parallel Interfaces for both display and camera<br>• Single/dual channel LVDS display interface<br>• HDMI transmitter<br>• MIPI/DSI transmitter<br>• MIPI/CSI-2 receiver<br>The processing includes:<br>• Image conversions: resizing, rotation, inversion, and color space conversion<br>• A high-quality de-interlacing filter<br>• Video/graphics combining<br>• Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement<br>• Support for display backlight reduction |
| KPP | Key Pad Port | Connectivity Peripherals | KPP Supports 8 x 8 external key pad matrix. KPP features are:<br>• Open drain design<br>• Glitch suppression circuit design<br>• Multiple keys detection<br>• Standby key press detection |

**Table 8. Maximum Supply Currents (continued)**

| Power Supply | Conditions | Maximum Current | | Unit |
|---|---|---|---|---|
| | | Power Virus | CoreMark | |
| NVCC_LVDS2P5 | — | NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5. | | |
| **MISC** | | | | |
| DRAM_VREF | — | 1 | | mA |

[1] The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

[2] Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

[3] This is the maximum current per active USB physical interface.

[4] The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

[5] General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

### 4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6Dual/6Quad processors in selected low power modes.

**Table 9. Stop Mode Current and Power Consumption**

| Mode | Test Conditions | Supply | Typical[1] | Unit |
|---|---|---|---|---|
| WAIT | • ARM, SoC, and PU LDOs are set to 1.225 V<br>• HIGH LDO set to 2.5 V<br>• Clocks are gated<br>• DDR is in self refresh<br>• PLLs are active in bypass (24 MHz)<br>• Supply voltages remain ON | VDD_ARM_IN (1.4 V) | 6 | mA |
| | | VDD_SOC_IN (1.4 V) | 23 | mA |
| | | VDD_HIGH_IN (3.0 V) | 3.7 | mA |
| | | Total | 52 | mW |

Optionally LDO_SOC and VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

## 4.3.2 Regulators for Analog Modules

### 4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB PHY, LVDS PHY, HDMI PHY, MIPI PHY, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

### 4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. The LDO_2P5 supplies the SATA PHY, USB PHY, LVDS PHY, HDMI PHY, MIPI PHY, E-fuse module and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

### 4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output

### 4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

**Table 22. GPIO I/O DC Parameters**

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level output voltage[1] | Voh | Ioh = -0.1 mA (DSE[2] = 001, 010)<br>Ioh = -1 mA<br>(DSE = 011, 100, 101, 110, 111) | OVDD – 0.15 | — | V |
| Low-level output voltage[1] | Vol | Iol = 0.1 mA (DSE[2] = 001, 010)<br>Iol = 1mA<br>(DSE = 011, 100, 101, 110, 111) | — | 0.15 | V |
| High-Level DC input voltage[1, 3] | Vih | — | 0.7 × OVDD | OVDD | V |
| Low-Level DC input voltage[1, 3] | Vil | — | 0 | 0.3 × OVDD | V |
| Input Hysteresis | Vhys | OVDD = 1.8 V<br>OVDD = 3.3 V | 0.25 | — | V |
| Schmitt trigger VT+[3, 4] | VT+ | — | 0.5 × OVDD | — | V |
| Schmitt trigger VT–[3, 4] | VT– | — | — | 0.5 × OVDD | V |
| Input current (no pull-up/down) | Iin | Vin = OVDD or 0 | -1 | 1 | μA |
| Input current (22 kΩ pull-up) | Iin | Vin = 0 V<br>Vin = OVDD | — | 212<br>1 | μA |
| Input current (47 kΩ pull-up) | Iin | Vin = 0 V<br>Vin = OVDD | — | 100<br>1 | μA |
| Input current (100 kΩ pull-up) | Iin | Vin = 0 V<br>Vin= OVDD | — | 48<br>1 | μA |
| Input current (100 kΩ pull-down) | Iin | Vin = 0 V<br>Vin = OVDD | — | 1<br>48 | μA |
| Keeper circuit resistance | Rkeep | Vin = 0.3 x OVDD<br>Vin = 0.7 x OVDD | 105 | 175 | kΩ |

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

### 4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

## 4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 29 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

**Table 29. DDR I/O LPDDR2 Mode AC Parameters[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AC input logic high | Vih(ac) | — | Vref + 0.22 | — | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | — | Vref – 0.22 | V |
| AC differential input high voltage[2] | Vidh(ac) | — | 0.44 | — | — | V |
| AC differential input low voltage | Vidl(ac) | — | — | — | 0.44 | V |
| Input AC differential cross point voltage[3] | Vix(ac) | Relative to Vref | -0.12 | — | 0.12 | V |
| Over/undershoot peak | Vpeak | — | — | — | 0.35 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | 533 MHz | — | — | 0.3 | V-ns |
| Single output slew rate, measured between Vol(ac) and Voh(ac) | tsr | 50 Ω to Vref.<br>5 pF load.<br>Drive impedance = 4 0 Ω ±30% | 1.5 | — | 3.5 | V/ns |
| | | 50 Ω to Vref.<br>5pF load.<br>Drive impedance = 60 Ω ±30% | 1 | — | 2.5 | |
| Skew between pad rise/fall asymmetry + skew caused by SSN | $t_{SKD}$ | clk = 533 MHz | — | — | 0.1 | ns |

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 30 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

**Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AC input logic high | Vih(ac) | — | Vref + 0.175 | — | OVDD | V |
| AC input logic low | Vil(ac) | — | 0 | — | Vref – 0.175 | V |
| AC differential input voltage[2] | Vid(ac) | — | 0.35 | — | — | V |
| Input AC differential cross point voltage[3] | Vix(ac) | Relative to Vref | Vref – 0.15 | — | Vref + 0.15 | V |
| Over/undershoot peak | Vpeak | — | — | — | 0.4 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | 533 MHz | — | — | 0.5 | V-ns |

### 4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 35 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

**Table 35. DDR I/O Output Buffer Impedance**

| Parameter | Symbol | Test Conditions | Typical | | Unit |
|---|---|---|---|---|---|
| | | | NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11 | NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10 | |
| Output Driver Impedance | Rdrv | Drive Strength (DSE) =<br>000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Ω |

**Note:**

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

### 4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

### 4.8.4 MLB 6-Pin I/O Differential Output Impedance

Table 36 shows MLB 6-pin I/O differential output impedance of i.MX 6Dual/6Quad processors.

**Table 36. MLB 6-Pin I/O Differential Output Impedance**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential Output Impedance | $Z_O$ | — | 1.6 | — | — | kΩ |

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

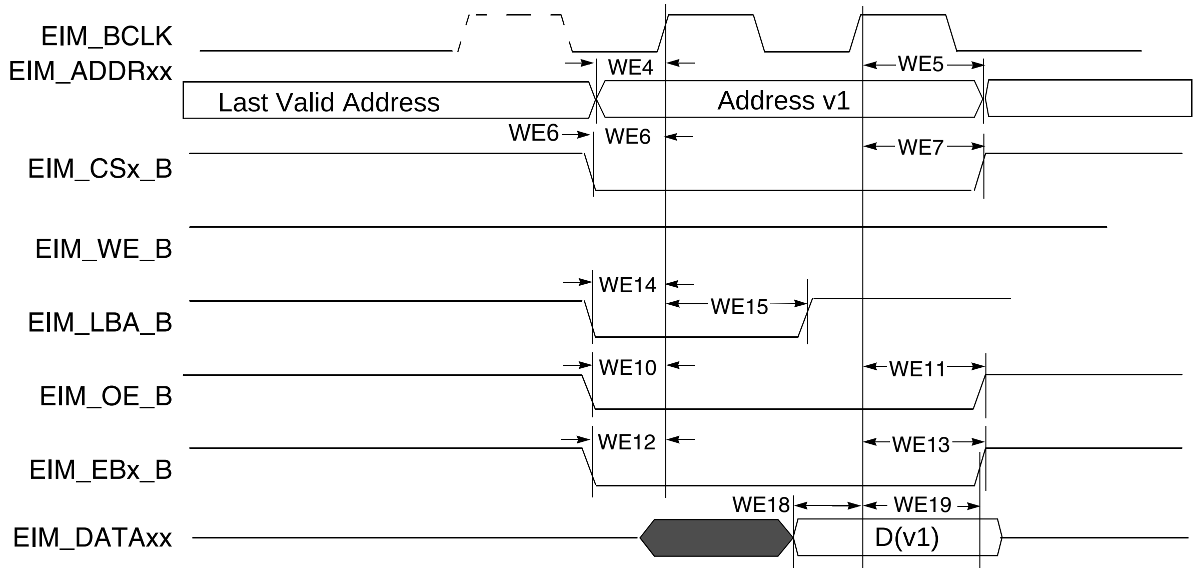


**Figure 14. Synchronous Memory Read Access, WSC=1**

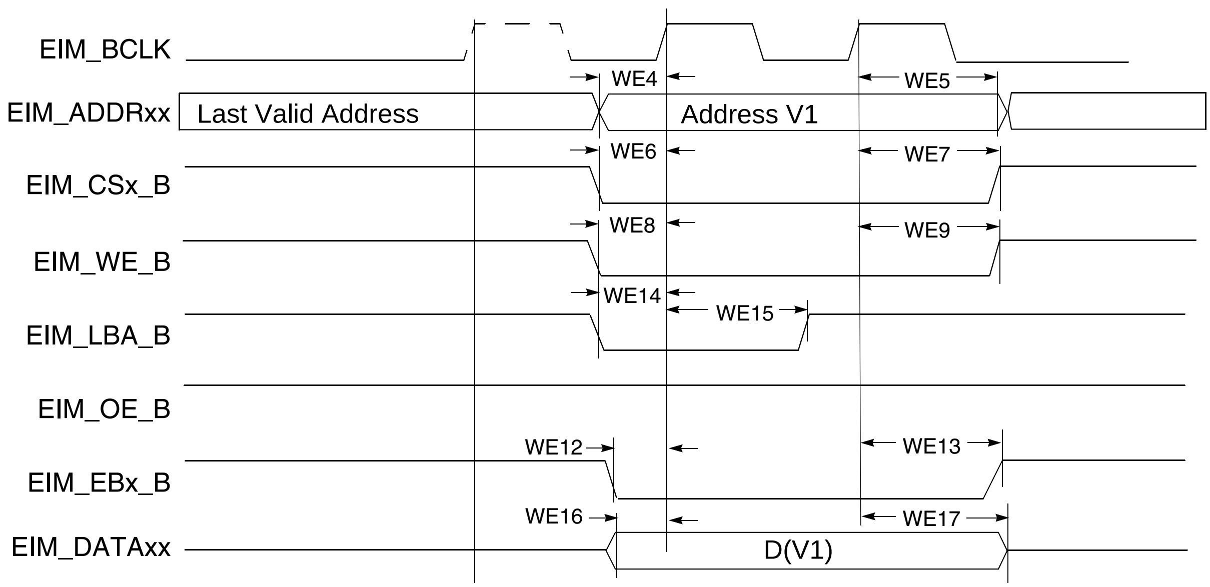


**Figure 15. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0**

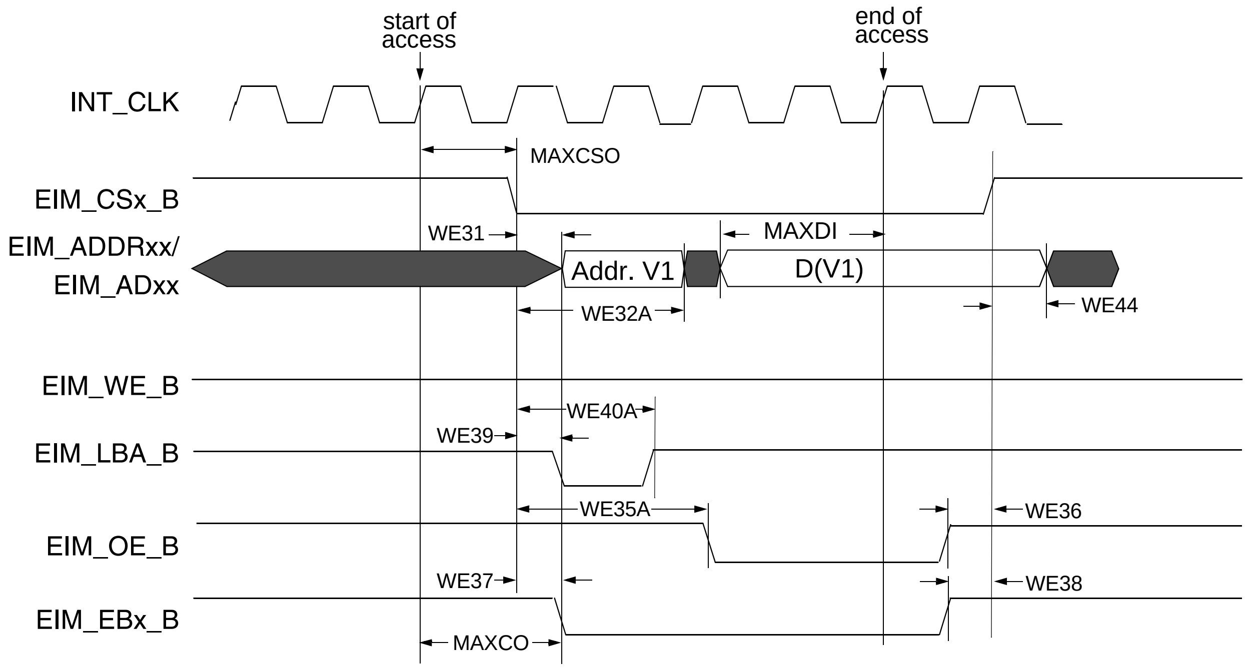


**Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)**

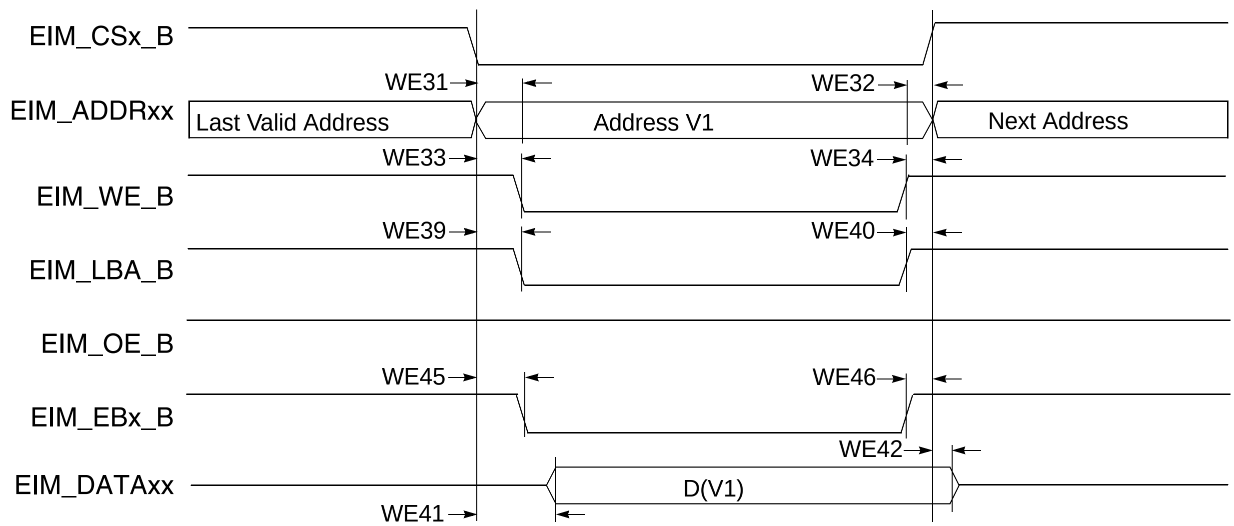


**Figure 20. Asynchronous Memory Write Access**

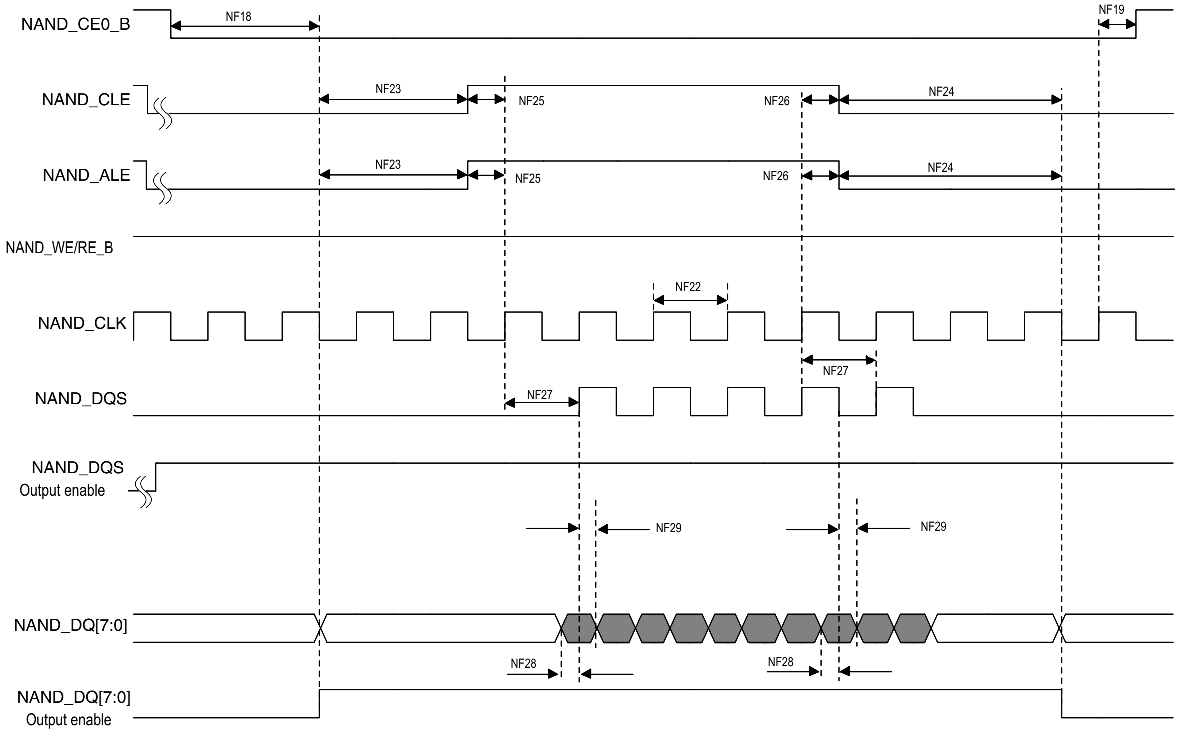


**Figure 36. Source Synchronous Mode Data Write Timing Diagram**

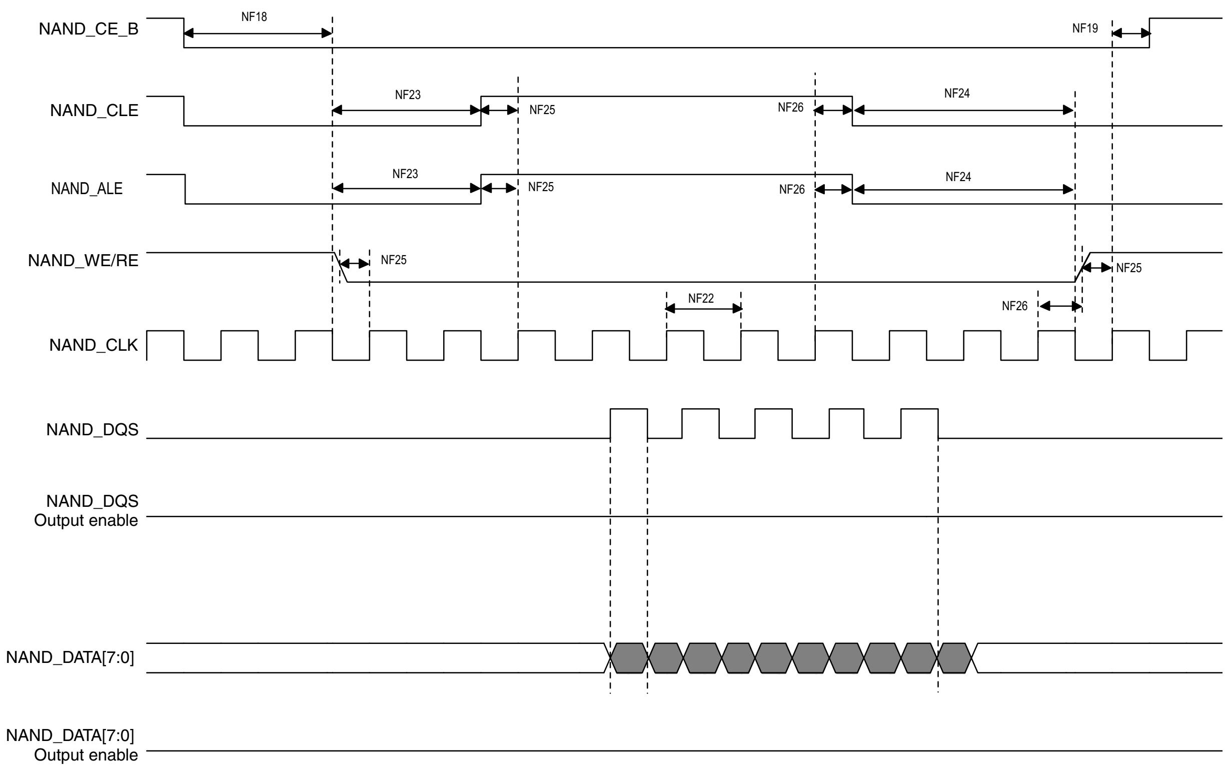


**Figure 37. Source Synchronous Mode Data Read Timing Diagram**

## 4.10.3 Samsung Toggle Mode AC Timing

### 4.10.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible)” for details.

### 4.10.3.2 Read and Write Timing

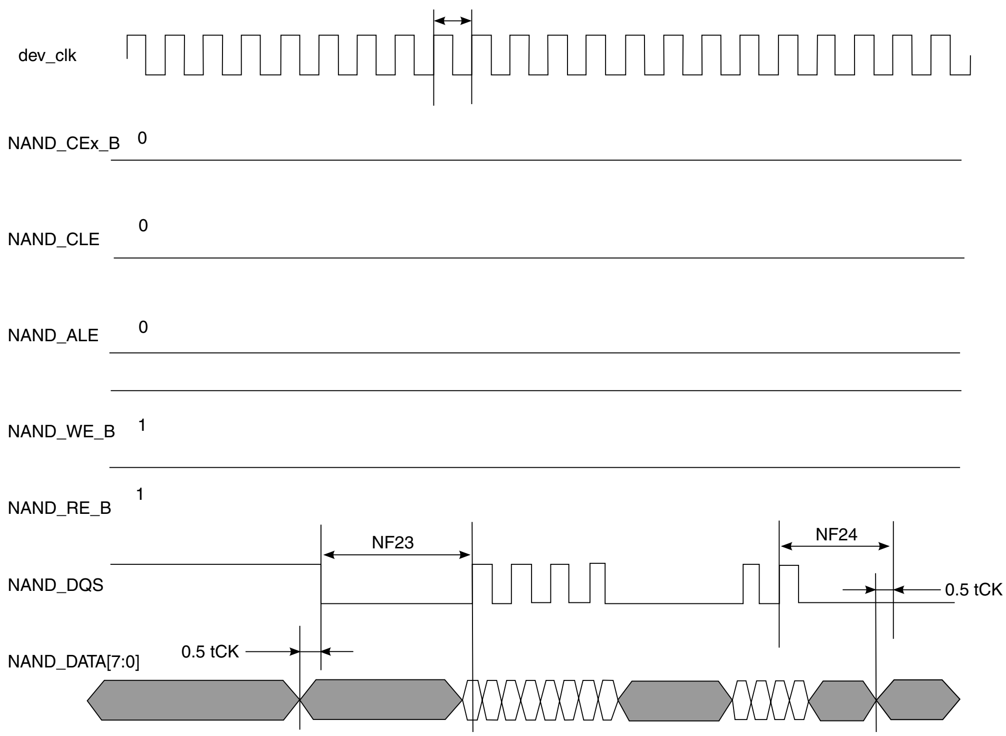


Figure 39. Samsung Toggle Mode Data Write Timing

**Table 54. SD/eMMC4.3 Interface Timing Specification (continued)**

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|---|---|---|---|
| **eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)** | | | | | |
| SD7 | eSDHC Input Setup Time | $t_{ISU}$ | 2.5 | — | ns |
| SD8 | eSDHC Input Hold Time[4] | $t_{IH}$ | 1.5 | — | ns |

[1] In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
[2] In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[3] In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
[4] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

## 4.11.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 46 depicts the timing of eMMC4.4/4.41. Table 55 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

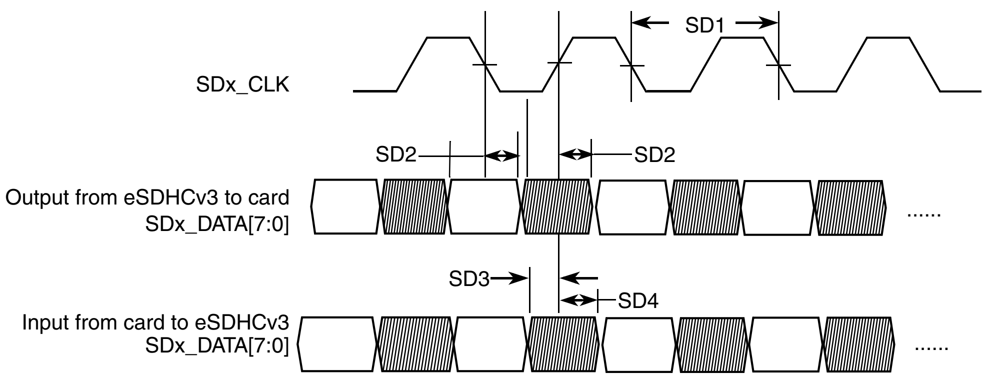


**Figure 46. eMMC4.4/4.41 Timing**

**Table 55. eMMC4.4/4.41 Interface Timing Specification**

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|---|---|---|---|
| **Card Input Clock** | | | | | |
| SD1 | Clock Frequency (EMMC4.4 DDR) | $f_{PP}$ | 0 | 52 | MHz |
| SD1 | Clock Frequency (SD3.0 DDR) | $f_{PP}$ | 0 | 50 | MHz |
| **uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)** | | | | | |
| SD2 | uSDHC Output Delay | $t_{OD}$ | 2.5 | 7.1 | ns |
| **uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)** | | | | | |
| SD3 | uSDHC Input Setup Time | $t_{ISU}$ | 2.6 | — | ns |
| SD4 | uSDHC Input Hold Time | $t_{IH}$ | 1.5 | — | ns |

### 4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 49 shows MII transmit signal timings. Table 58 describes the timing parameters (M5–M8) shown in the figure.

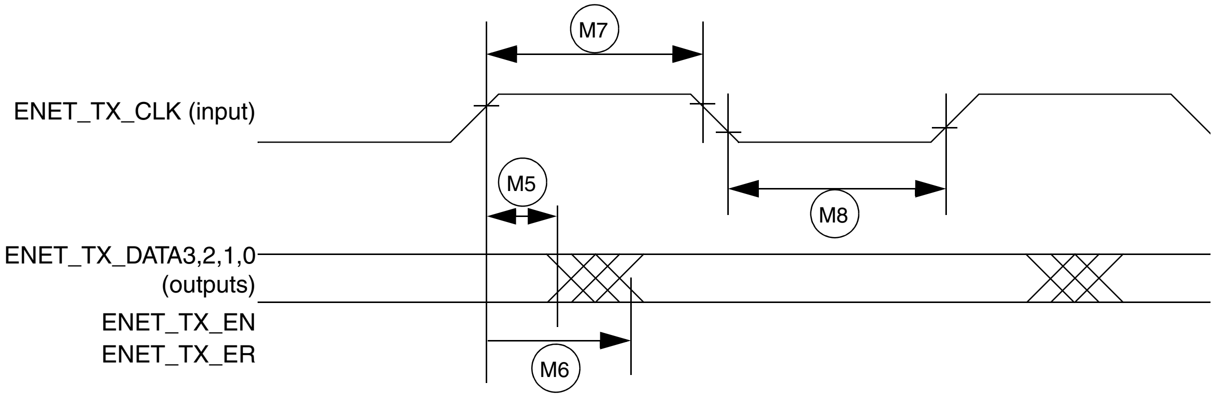


**Figure 49. MII Transmit Signal Timing Diagram**

**Table 58. MII Transmit Signal Timing**

| ID | Characteristic[1] | Min | Max | Unit |
|---|---|---|---|---|
| M5 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid | 5 | — | ns |
| M6 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid | — | 20 | ns |
| M7 | ENET_TX_CLK pulse width high | 35% | 65% | ENET_TX_CLK period |
| M8 | ENET_TX_CLK pulse width low | 35% | 65% | ENET_TX_CLK period |

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

### 4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 50 shows MII asynchronous input timings. Table 59 describes the timing parameter (M9) shown in the figure.

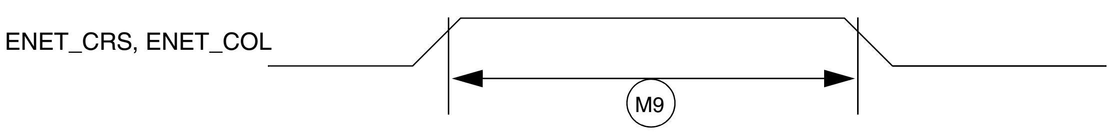


**Figure 50. MII Async Inputs Timing Diagram**

Table 69 shows timing characteristics of signals presented in Figure 69 and Figure 70.

**Table 69. Synchronous Display Interface Timing Characteristics (Pixel Level)**

| ID | Parameter | Symbol | Value | Description | Unit |
|---|---|---|---|---|---|
| IP5 | Display interface clock period | Tdicp | (see[1]) | Display interface clock IPP_DISP_CLK | ns |
| IP6 | Display pixel clock period | Tdpcp | DISP_CLK_PER_PIXEL × Tdicp | Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.***n***).<br>The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period.<br>The DISP_CLK_PER_PIXEL is received by DC/DI one access division to ***n*** components. | ns |
| IP7 | Screen width time | Tsw | (SCREEN_WIDTH) × Tdicp | SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included.<br>The SCREEN_WIDTH should be built by suitable DI's counter[2]. | ns |
| IP8 | HSYNC width time | Thsw | (HSYNC_WIDTH) | HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter. | ns |
| IP9 | Horizontal blank interval 1 | Thbi1 | BGXP × Tdicp | BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter. | ns |
| IP10 | Horizontal blank interval 2 | Thbi2 | (SCREEN_WIDTH – BGXP – FW) × Tdicp | Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter. | ns |
| IP12 | Screen height | Tsh | (SCREEN_HEIGHT) × Tsw | SCREEN_HEIGHT— screen height in lines with blanking.<br>The SCREEN_HEIGHT is a distance between 2 VSYNCs.<br>The SCREEN_HEIGHT should be built by suitable DI's counter. | ns |
| IP13 | VSYNC width | Tvsw | VSYNC_WIDTH | VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter. | ns |
| IP14 | Vertical blank interval 1 | Tvbi1 | BGYP × Tsw | BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter. | ns |
| IP15 | Vertical blank interval 2 | Tvbi2 | (SCREEN_HEIGHT – BGYP – FH) × Tsw | Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter. | ns |

### 4.11.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 72 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signalling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

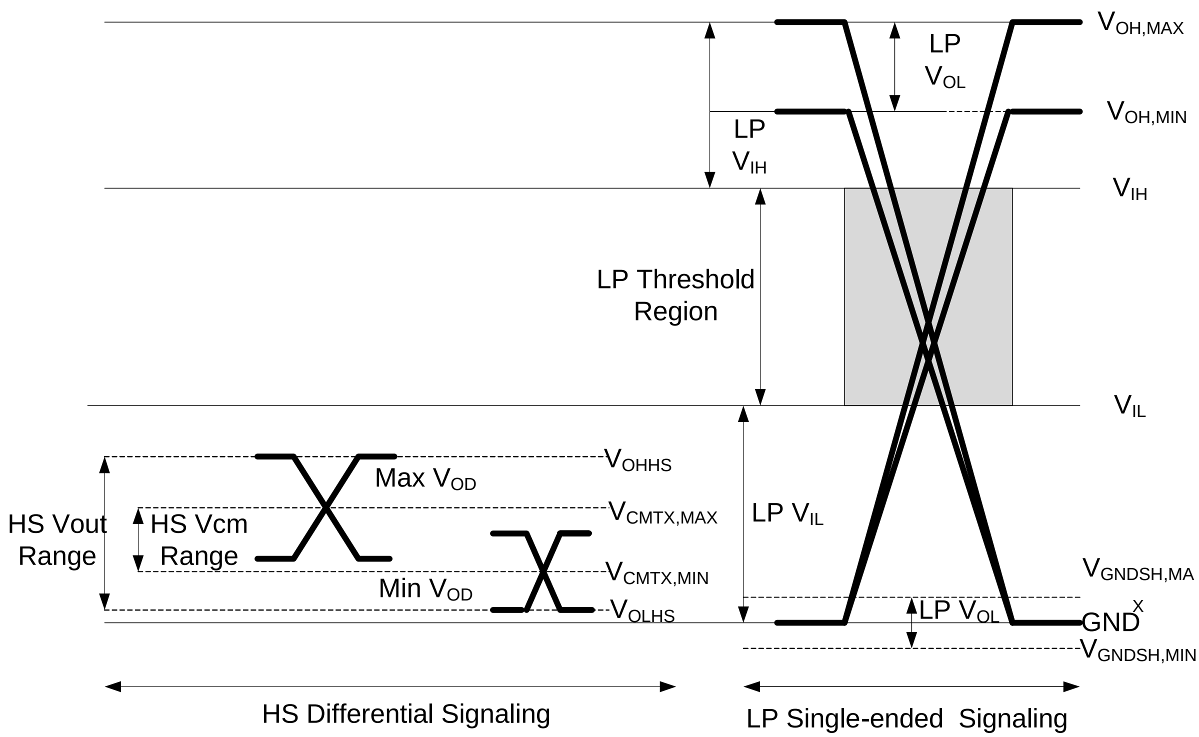


**Figure 72. D-PHY Signaling Levels**

### 4.11.12.3 HS Line Driver Characteristics

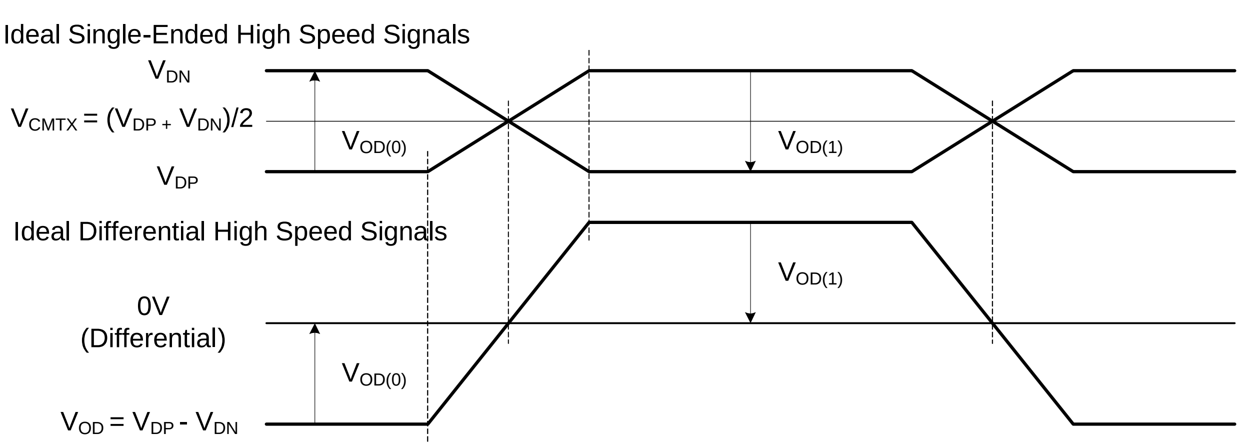


**Figure 73. Ideal Single-ended and Resulting Differential HS Signals**

**Table 73. Electrical and Timing Information (continued)**

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LP Line Drivers AC Specifications** | | | | | | |
| $t_{rlp},t_{flp}$ | Single ended output rise/fall time | 15% to 85%, $C_L$<70 pF | — | — | 25 | ns |
| $t_{reo}$ | — | 30% to 85%, $C_L$<70 pF | — | — | 35 | ns |
| $\delta V/\delta t_{SR}$ | Signal slew rate | 15% to 85%, $C_L$<70 pF | — | — | 120 | mV/ns |
| $C_L$ | Load capacitance | — | 0 | — | 70 | pF |
| **HS Line Receiver AC Specifications** | | | | | | |
| $t_{SETUP[RX]}$ | Data to Clock Receiver Setup time | — | 0.15 | — | — | UI |
| $t_{HOLD[RX]}$ | Clock to Data Receiver Hold time | — | 0.15 | — | — | UI |
| $\Delta V_{CMRX(HF)}$ | Common mode interference beyond 450 MHz | — | — | — | 200 | mVpp |
| $\Delta V_{CMRX(LF)}$ | Common mode interference between 50 MHz and 450 MHz | — | -50 | — | 50 | mVpp |
| $C_{CM}$ | Common mode termination | — | — | — | 60 | pF |
| **LP Line Receiver AC Specifications** | | | | | | |
| $e_{SPIKE}$ | Input pulse rejection | — | — | — | 300 | Vps |
| $T_{MIN}$ | Minimum pulse response | — | 50 | — | — | ns |
| $V_{INT}$ | Pk-to-Pk interference voltage | — | — | — | 400 | mV |
| $f_{INT}$ | Interference frequency | — | 450 | — | — | MHz |
| **Model Parameters used for Driver Load switching performance evaluation** | | | | | | |
| $C_{PAD}$ | Equivalent Single ended I/O PAD capacitance. | — | — | — | 1 | pF |
| $C_{PIN}$ | Equivalent Single ended Package + PCB capacitance. | — | — | — | 2 | pF |
| $L_S$ | Equivalent wire bond series inductance | — | — | — | 1.5 | nH |
| $R_S$ | Equivalent wire bond series resistance | — | — | — | 0.15 | Ω |
| $R_L$ | Load Resistance | — | 80 | 100 | 125 | Ω |

**Table 77. MLB 256/512 Fs Timing Parameters (continued)**

| Parameter | Symbol | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| Bus Hold from MLB_CLK low | $t_{mdzh}$ | 4 | — | ns | — |
| Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high) | Tdelay | — | 10.75 | — | ns |

[1] The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

[2] MLB_CLK low/high time includes the pulse width variation.

[3] The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for $t_{mdzh}$. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 78; unless otherwise noted.

**Table 78. MLB 1024 Fs Timing Parameters**

| Parameter | Symbol | Min | Max | Unit | Comment |
|---|---|---|---|---|---|
| MLB_CLK Operating Frequency[1] | $f_{mck}$ | 45.056 | 51.2 | MHz | 1024xfs at 44.0 kHz<br>1024xfs at 50.0 kHz |
| MLB_CLK rise time | $t_{mckr}$ | — | 1 | ns | $V_{IL}$ TO $V_{IH}$ |
| MLB_CLK fall time | $t_{mckf}$ | — | 1 | ns | $V_{IH}$ TO $V_{IL}$ |
| MLB_CLK low time | $t_{mckl}$ | 6.1 | — | ns | (see [2]) |
| MLB_CLK high time | $t_{mckh}$ | 9.3 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling | $t_{dsmcf}$ | 1 | — | ns | — |
| MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low | $t_{dhmcf}$ | $t_{mdzh}$ | — | ns | — |
| MLB_SIG/MLB_DATA output high impedance from MLB_CLK low | $t_{mcfdz}$ | 0 | $t_{mckl}$ | ns | (see [3]) |
| Bus Hold from MLB_CLK low | $t_{mdzh}$ | 2 | — | ns | — |
| Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high) | Tdelay | — | 6 | ns | — |

[1] The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

[2] MLB_CLK low/high time includes the pulse width variation.

[3] The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for $t_{mdzh}$. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 79 lists the MediaLB 6-pin interface timing characteristics, and Figure 88 shows the MLB 6-pin delay, setup, and hold times.

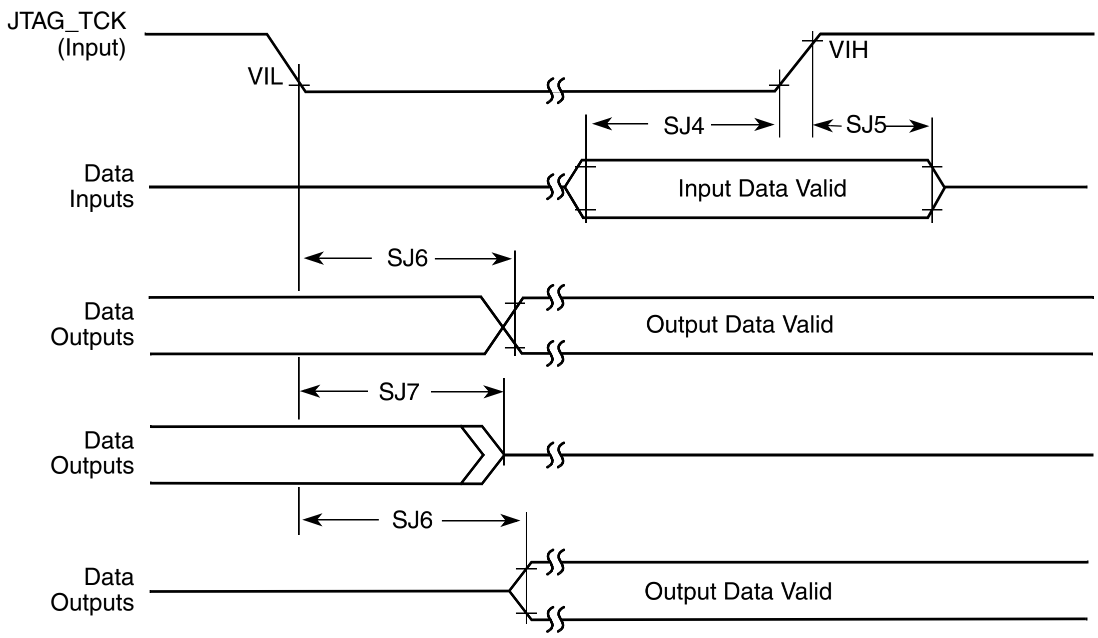


**Figure 91. Boundary Scan (JTAG) Timing Diagram**

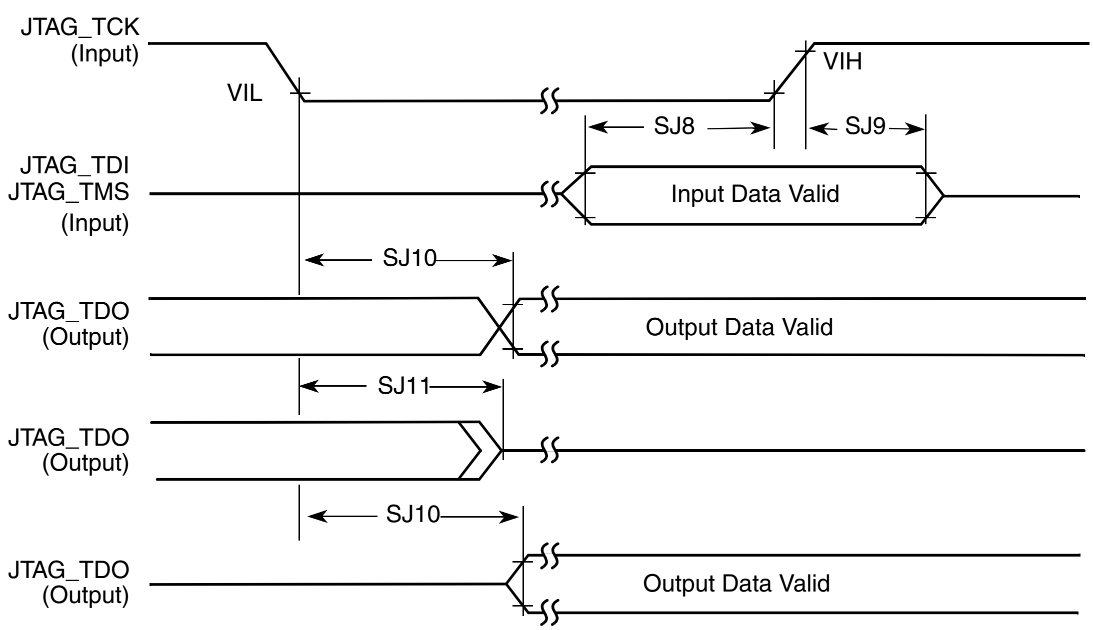


**Figure 92. Test Access Port Timing Diagram**

### 4.11.20.2 SSI Receiver Timing with Internal Clock

Figure 97 depicts the SSI receiver internal clock timing and Table 87 lists the timing parameters for the receiver timing with the internal clock.

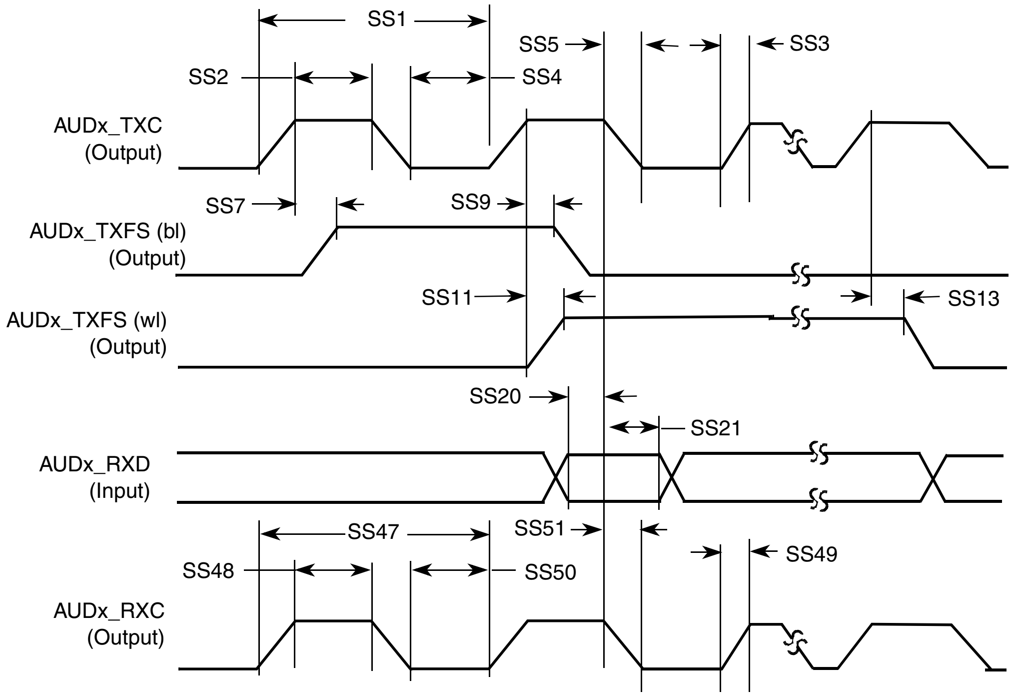


**Figure 97. SSI Receiver Internal Clock Timing Diagram**

**Table 87. SSI Receiver Timing with Internal Clock**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Internal Clock Operation | | | | |
| SS1 | AUDx_TXC/AUDx_RXC clock period | 81.4 | — | ns |
| SS2 | AUDx_TXC/AUDx_RXC clock high period | 36.0 | — | ns |
| SS3 | AUDx_TXC/AUDx_RXC clock rise time | — | 6.0 | ns |
| SS4 | AUDx_TXC/AUDx_RXC clock low period | 36.0 | — | ns |
| SS5 | AUDx_TXC/AUDx_RXC clock fall time | — | 6.0 | ns |
| SS7 | AUDx_RXC high to AUDx_TXFS (bl) high | — | 15.0 | ns |
| SS9 | AUDx_RXC high to AUDx_TXFS (bl) low | — | 15.0 | ns |
| SS11 | AUDx_RXC high to AUDx_TXFS (wl) high | — | 15.0 | ns |
| SS13 | AUDx_RXC high to AUDx_TXFS (wl) low | — | 15.0 | ns |
| SS20 | AUDx_RXD setup time before AUDx_RXC low | 10.0 | — | ns |
| SS21 | AUDx_RXD hold time after AUDx_RXC low | 0.0 | — | ns |

**Table 99. 21 x 21 mm Supplies Contact Assignment (continued)**

| Supply Rail Name | Ball(s) Position(s) | Remark |
|---|---|---|
| VDDHIGH_CAP | H10, J10 | Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used) |
| VDDHIGH_IN | H9, J9 | Primary supply for the 2.5 V regulator |
| VDDPU_CAP | H17, J17, K17, L17, M17, N17, P17 | Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used) |
| VDDSOC_CAP | R10, T10, T13, T14, U10, U13, U14 | Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used) |
| VDDSOC_IN | H16, J16, K16, L16, M16, N16, P16, R16, T16, U16 | Primary supply for the SoC and PU regulators |
| VDDUSB_CAP | F9 | Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used) |
| ZQPAD | AE17 | — |

Table 100 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

**Table 100. 21 x 21 mm Functional Contact Assignments**

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| BOOT_MODE0 | C12 | VDD_SNVS_IN | GPIO | ALT0 | SRC_BOOT_MODE0 | Input | PD (100K) |
| BOOT_MODE1 | F12 | VDD_SNVS_IN | GPIO | ALT0 | SRC_BOOT_MODE1 | Input | PD (100K) |
| CLK1_N | C7 | VDD_HIGH_CAP | — | — | CLK1_N | — | — |
| CLK1_P | D7 | VDD_HIGH_CAP | — | — | CLK1_P | — | — |
| CLK2_N | C5 | VDD_HIGH_CAP | — | — | CLK2_N | — | — |
| CLK2_P | D5 | VDD_HIGH_CAP | — | — | CLK2_P | — | — |
| CSI_CLK0M | F4 | NVCC_MIPI | — | — | CSI_CLK_N | — | — |
| CSI_CLK0P | F3 | NVCC_MIPI | — | — | CSI_CLK_P | — | — |
| CSI_D0M | E4 | NVCC_MIPI | — | — | CSI_DATA0_N | — | — |
| CSI_D0P | E3 | NVCC_MIPI | — | — | CSI_DATA0_P | — | — |
| CSI_D1M | D1 | NVCC_MIPI | — | — | CSI_DATA1_N | — | — |
| CSI_D1P | D2 | NVCC_MIPI | — | — | CSI_DATA1_P | — | — |
| CSI_D2M | E1 | NVCC_MIPI | — | — | CSI_DATA2_N | — | — |
| CSI_D2P | E2 | NVCC_MIPI | — | — | CSI_DATA2_P | — | — |
| CSI_D3M | F2 | NVCC_MIPI | — | — | CSI_DATA3_N | — | — |

**Table 100. 21 x 21 mm Functional Contact Assignments (continued)**

| Ball Name | Ball | Power Group | Ball Type | Out of Reset Condition[1] | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode (Reset Mode) | Default Function (Signal Name) | Input/Output | Value[2] |
| SD3_CLK | D14 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO03 | Input | PU (100K) |
| SD3_CMD | B13 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO02 | Input | PU (100K) |
| SD3_DAT0 | E14 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO04 | Input | PU (100K) |
| SD3_DAT1 | F14 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO05 | Input | PU (100K) |
| SD3_DAT2 | A15 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO06 | Input | PU (100K) |
| SD3_DAT3 | B15 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO07 | Input | PU (100K) |
| SD3_DAT4 | D13 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO01 | Input | PU (100K) |
| SD3_DAT5 | C13 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO00 | Input | PU (100K) |
| SD3_DAT6 | E13 | NVCC_SD3 | GPIO | ALT5 | GPIO6_IO18 | Input | PU (100K) |
| SD3_DAT7 | F13 | NVCC_SD3 | GPIO | ALT5 | GPIO6_IO17 | Input | PU (100K) |
| SD3_RST | D15 | NVCC_SD3 | GPIO | ALT5 | GPIO7_IO08 | Input | PU (100K) |
| SD4_CLK | E16 | NVCC_NANDF | GPIO | ALT5 | GPIO7_IO10 | Input | PU (100K) |
| SD4_CMD | B17 | NVCC_NANDF | GPIO | ALT5 | GPIO7_IO09 | Input | PU (100K) |
| SD4_DAT0 | D18 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO08 | Input | PU (100K) |
| SD4_DAT1 | B19 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO09 | Input | PU (100K) |
| SD4_DAT2 | F17 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO10 | Input | PU (100K) |
| SD4_DAT3 | A20 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO11 | Input | PU (100K) |
| SD4_DAT4 | E18 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO12 | Input | PU (100K) |
| SD4_DAT5 | C19 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO13 | Input | PU (100K) |
| SD4_DAT6 | B20 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO14 | Input | PU (100K) |
| SD4_DAT7 | D19 | NVCC_NANDF | GPIO | ALT5 | GPIO2_IO15 | Input | PU (100K) |
| TAMPER | E11 | VDD_SNVS_IN | GPIO | ALT0 | SNVS_TAMPER | Input | PD (100K) |
| TEST_MODE | E12 | VDD_SNVS_IN | — | — | TCU_TEST_MODE | Input | PD (100K) |
| USB_H1_DN | F10 | VDD_USB_CAP | — | — | USB_H1_DN | — | — |
| USB_H1_DP | E10 | VDD_USB_CAP | — | — | USB_H1_DP | — | — |
| USB_OTG_CHD_B | B8 | VDD_USB_CAP | — | — | USB_OTG_CHD_B | — | — |
| USB_OTG_DN | B6 | VDD_USB_CAP | — | — | USB_OTG_DN | — | — |
| USB_OTG_DP | A6 | VDD_USB_CAP | — | — | USB_OTG_DP | — | — |
| XTALI | A7 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | B7 | NVCC_PLL | — | — | XTALO | — | — |

1 The state immediately after reset and before ROM firmware or software has executed.

2 Variance of the pull-up and pull-down strengths are shown in the tables as follows:


- Table 22, "GPIO I/O DC Parameters," on page 39.
- Table 23, "LPDDR2 I/O DC Electrical Parameters," on page 40
- Table 24, "DDR3/DDR3L I/O DC Electrical Parameters," on page 40