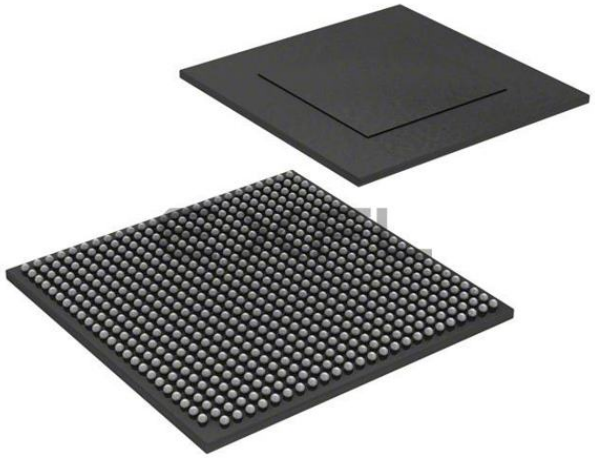

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d6avt08adr

- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

1.3 Updated Signal Naming Convention

The signal names of the i.MX 6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, etc.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 39 provides EIM interface pads allocation in different modes.

Table 39. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 40. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE4	Clock rise to address valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE9	Clock rise to EIM_WE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

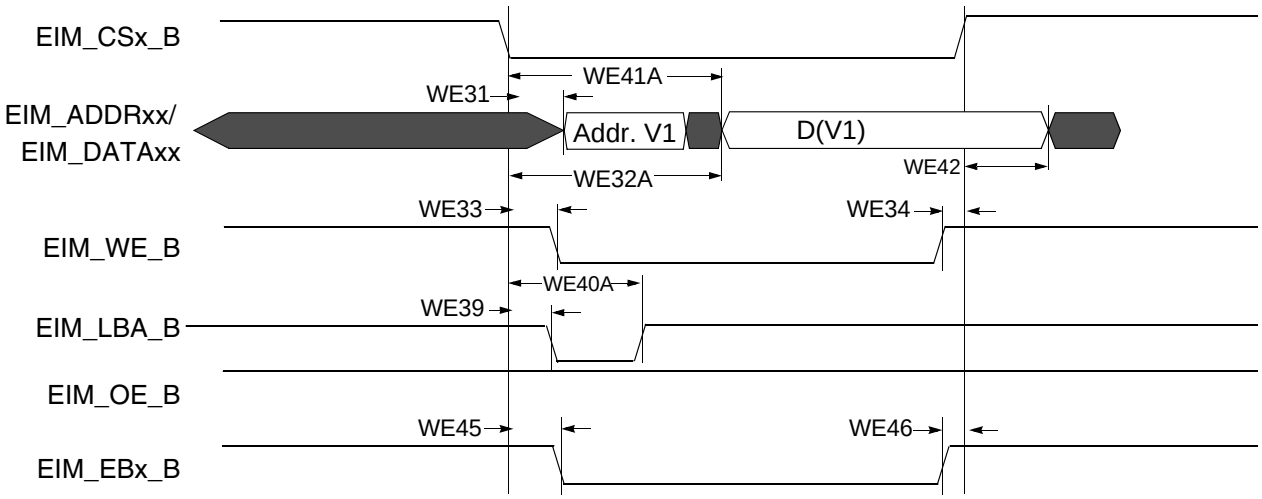

Figure 21. Asynchronous A/D Muxed Write Access

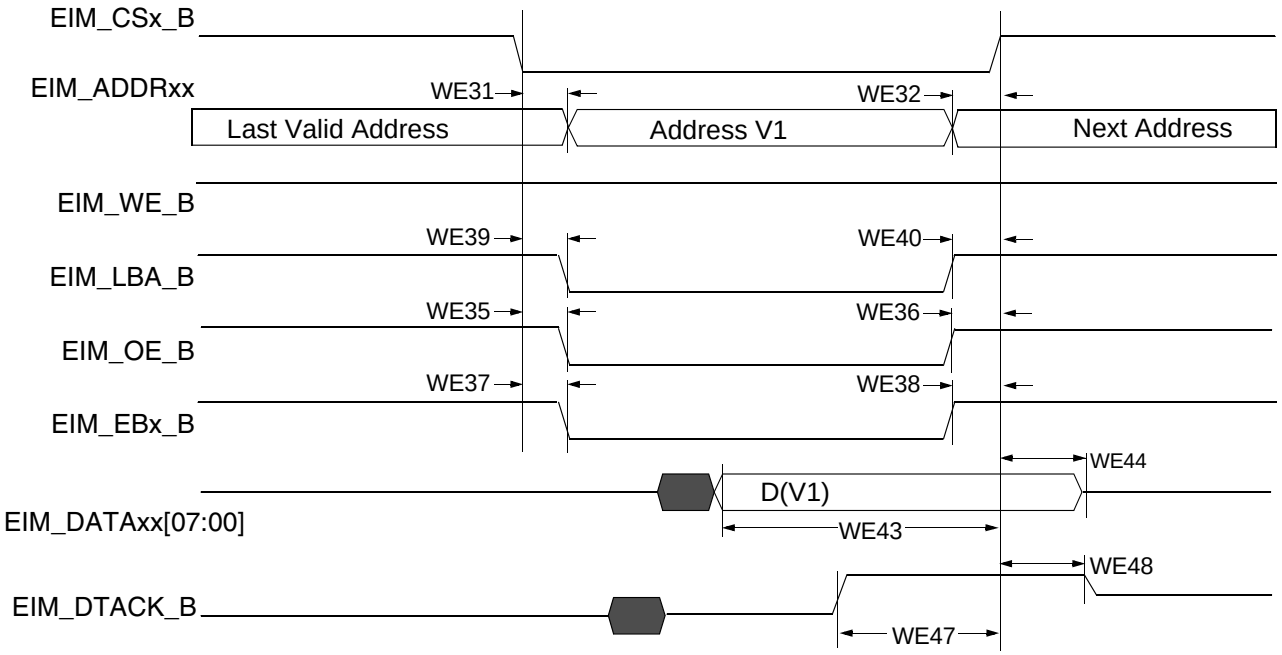

Figure 22. DTACK Mode Read Access (DAP=0)

Table 42. DDR3/DDR3L Timing Parameter (continued)

ID	Parameter[1,2]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR4	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx setup time	tIS	500	—	ps
DDR5	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKEx, DRAM_SDWE_B, DRAM_ODTx hold time	tIH	400	—	ps
DDR6	Address output setup time	tIS	500	—	ps
DDR7	Address output hold time	tIH	400	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 25 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 43.

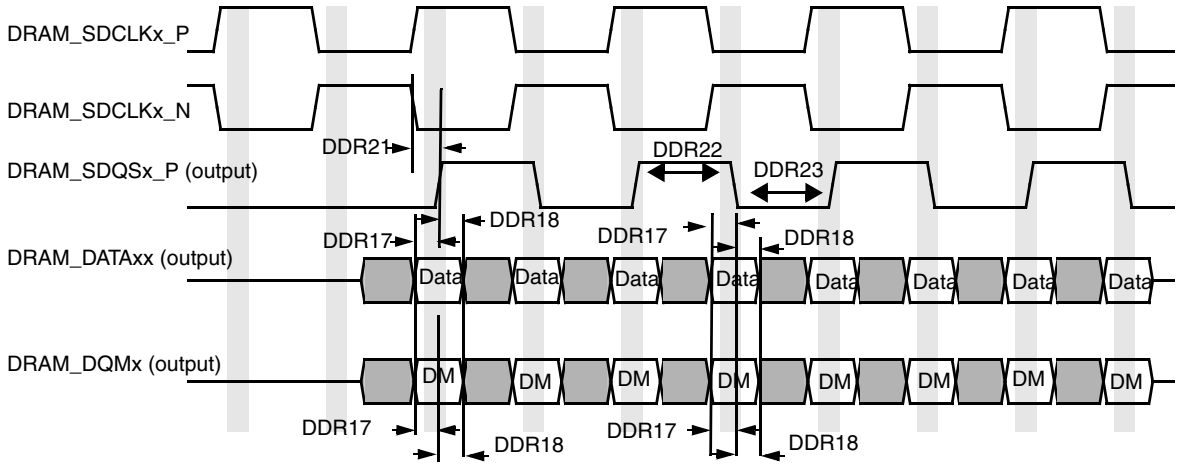

Figure 25. DDR3/DDR3L Write Cycle

Table 43. DDR3/DDR3L Write Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tDS	125[4]	—	ps
DDR18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tDH	150[4]	—	ps
DDR21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DRAM_SDQSx_P high level width	tDQSH	0.45	0.55	tCK
DDR23	DRAM_SDQSx_P low level width	tDQSL	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to DRAM_VREF

1 To receive the reported setup and hold values, the write calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 29 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 47.

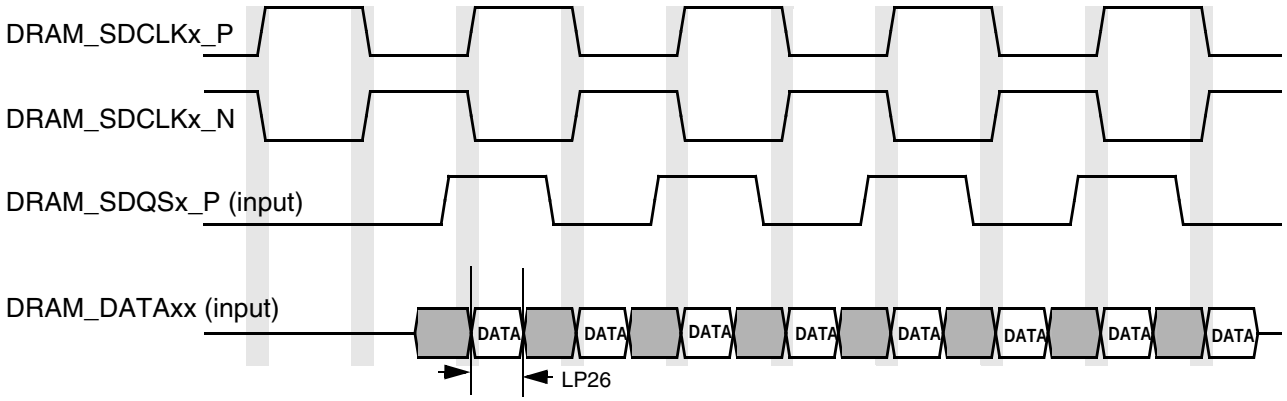

Figure 29. LPDDR2 Read Cycle

Table 47. LPDDR2 Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2	—	250	—	ps

1 To receive the reported setup and hold values, read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

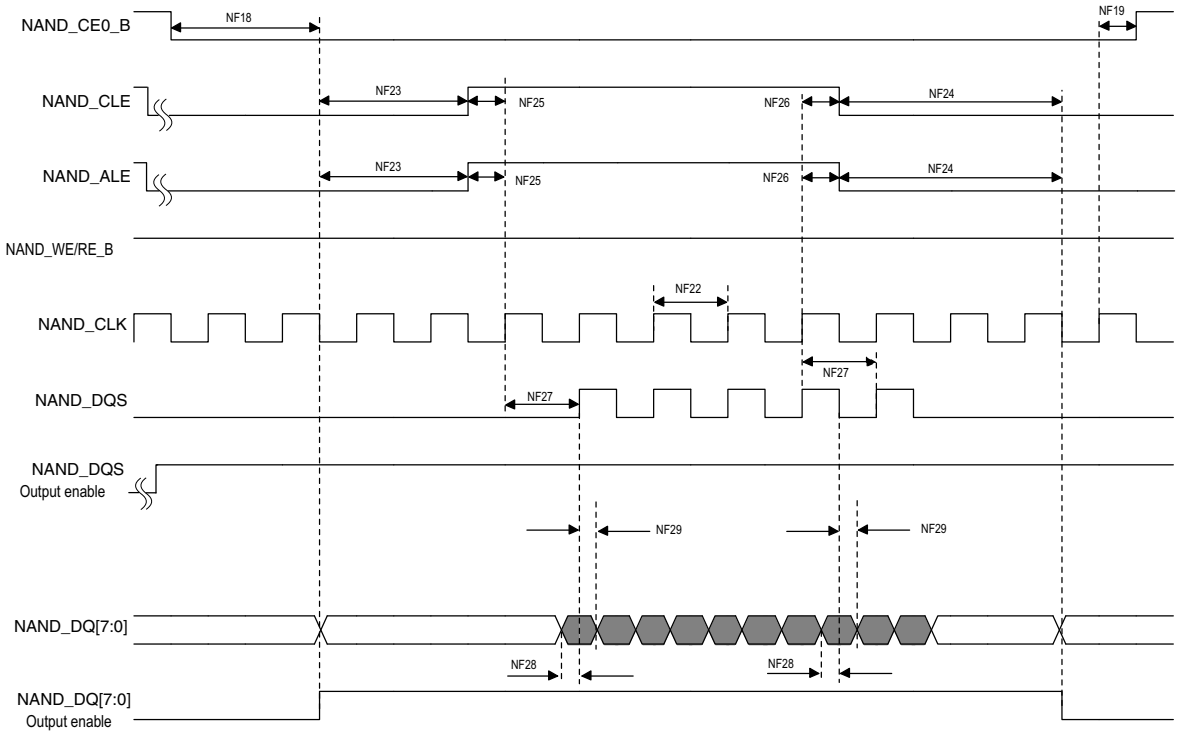

Figure 36. Source Synchronous Mode Data Write Timing Diagram

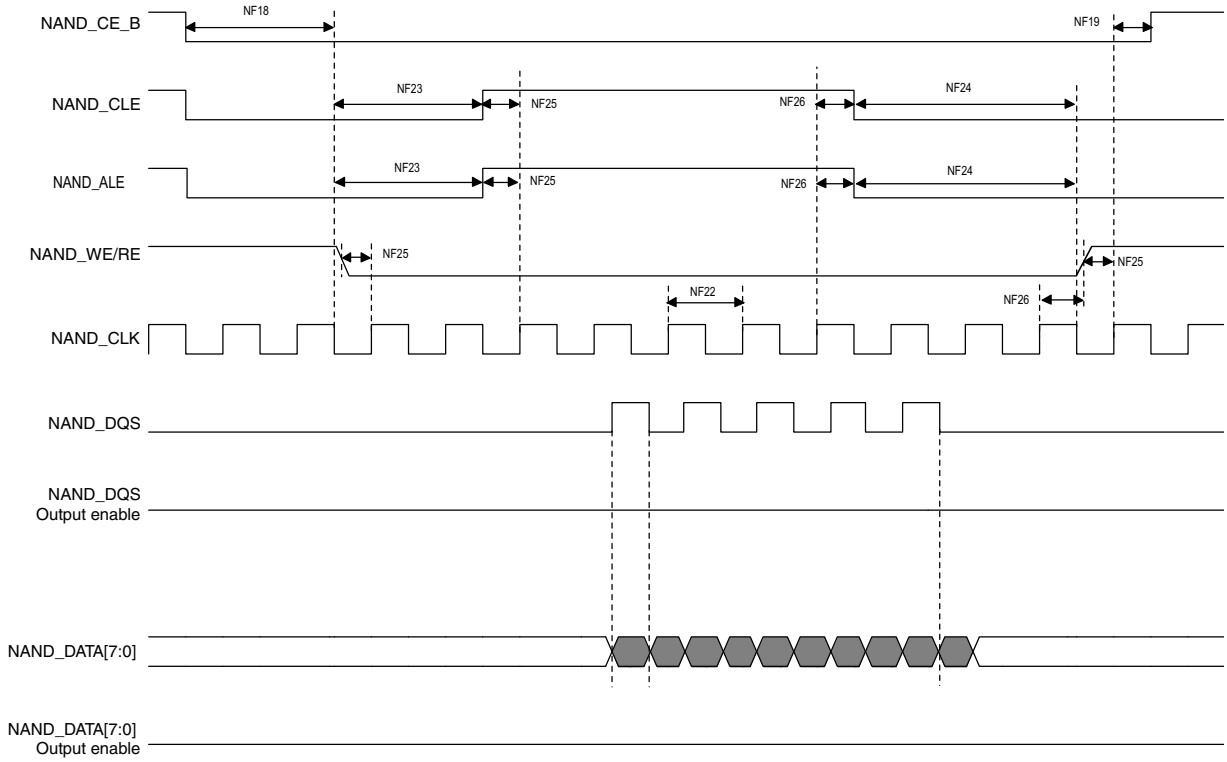

Figure 37. Source Synchronous Mode Data Read Timing Diagram

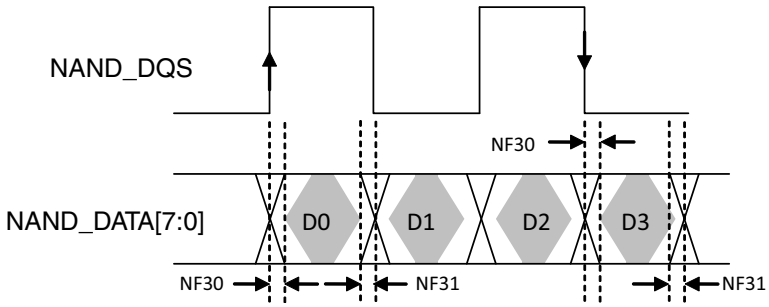

Figure 38. NAND_DQS/NAND_DQ Read Valid Window

Table 49. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		—
NF29	Data write hold	tDH	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1 The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 38 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

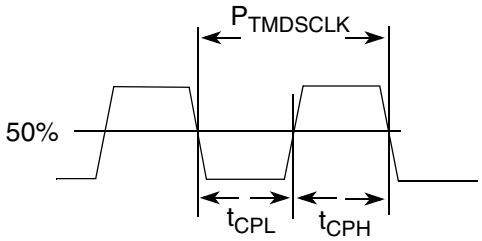

Figure 59. TMDS Clock Signal Definitions

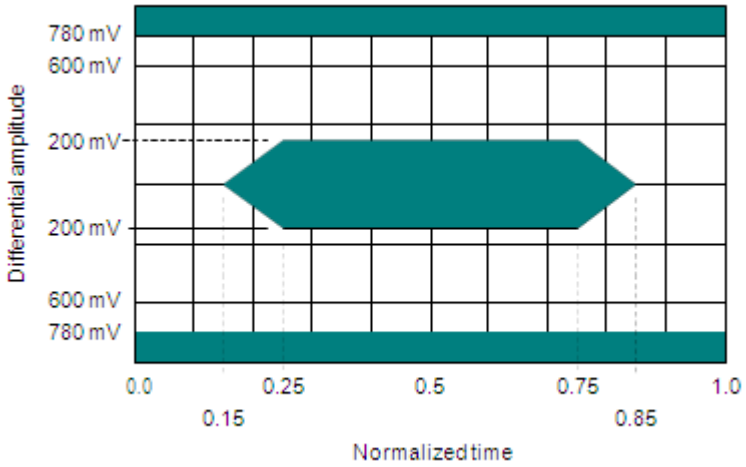

Figure 60. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

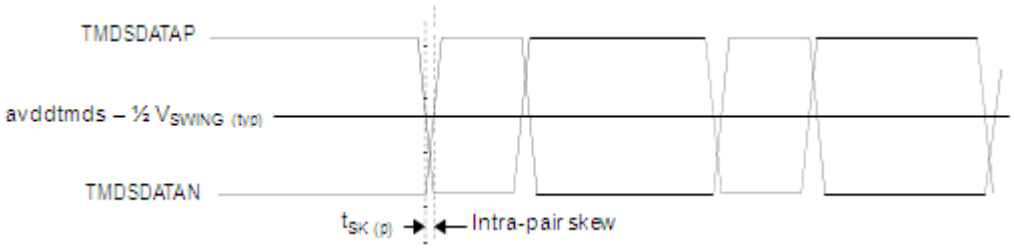

Figure 61. Intra-Pair Skew Definition

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.11.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 65.

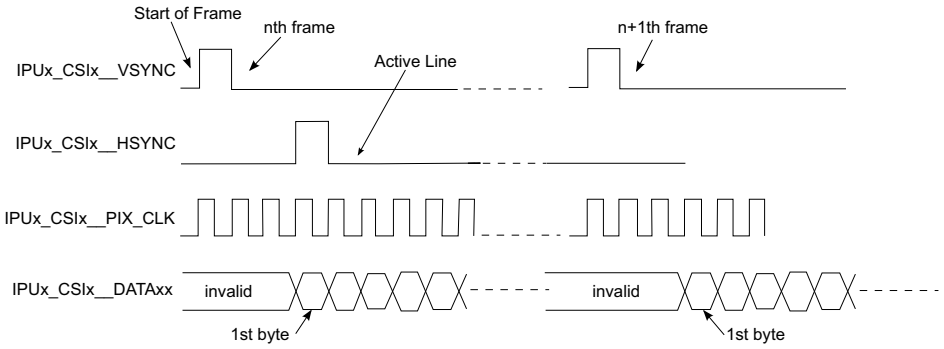

Figure 65. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

stops receiving data from the stream. For the next line, the IPU2_CSIx_HSYNC timing repeats. For the next frame, the IPU2_CSIx_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the IPU2_CSIx_HSYNC signal, which is not used (see Figure 66). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPU2_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

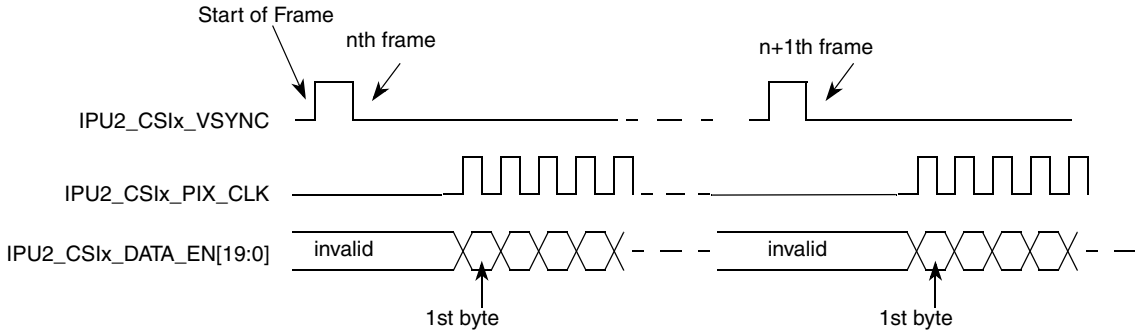

Figure 66. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 66 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPU2_CSIx_VSYNC; active-high/low IPU2_CSIx_HSYNC; and rising/falling-edge triggered IPU2_CSIx_PIX_CLK.

4.11.10.3 Electrical Characteristics

Figure 67 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 67 lists the sensor interface timing characteristics.

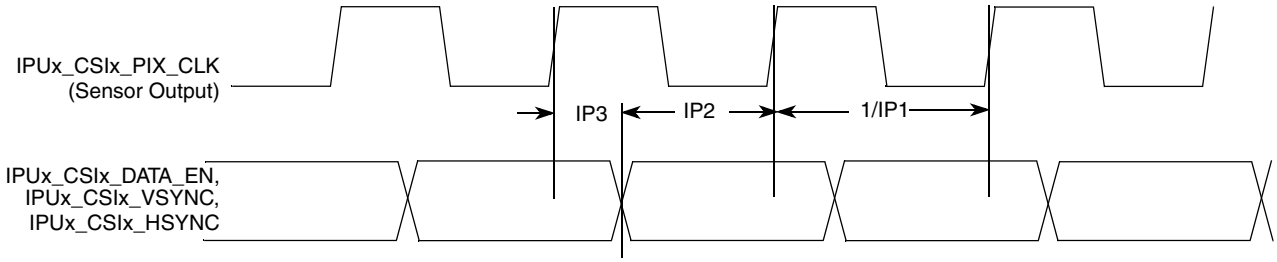

Figure 67. Sensor Interface Timing Diagram

Table 67. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 68 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 68. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

Table 68. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_DIx_DISP_CLK	PixCLK							—
IPUx_DIx_PIN01	—							May be required for anti-tearing
IPUx_DIx_PIN02	HSYNC							—
IPUx_DIx_PIN03	VSYNC							VSYNC out
IPUx_DIx_PIN04	—							Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—							
IPUx_DIx_PIN06	—							
IPUx_DIx_PIN07	—							
IPUx_DIx_PIN08	—							

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 97 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 97. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	Boot Mode Selection
BOOT_MODE0	Input	Boot Mode Selection
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]

Table 98. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 21.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D	REV: D
	STANDARD: NON–JEDEC	
	08 OCT 2013	

Figure 107. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 2 of 2)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	0
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	0
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	0
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	0
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	Hi-Z
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK1_P	Input	Hi-Z
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK1_N	—	—
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	0
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	0
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	DDRCLK	—	DRAM_SDQS4_N	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	DDRCLK	—	DRAM_SDQS5_N	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	DDRCLK	—	DRAM_SDQS6_N	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	DDRCLK	—	DRAM_SDQS7_N	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	0
DSI_CLK0M	H3	NVCC_MIPI	—	—	DSI_CLK_N	—	—
DSI_CLK0P	H4	NVCC_MIPI	—	—	DSI_CLK_P	—	—
DSI_D0M	G2	NVCC_MIPI	—	—	DSI_DATA0_N	—	—
DSI_D0P	G1	NVCC_MIPI	—	—	DSI_DATA0_P	—	—
DSI_D1M	H2	NVCC_MIPI	—	—	DSI_DATA1_N	—	—
DSI_D1P	H1	NVCC_MIPI	—	—	DSI_DATA1_P	—	—
EIM_A16	H25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR16	Output	0
EIM_A17	G24	NVCC_EIM1	GPIO	ALT0	EIM_ADDR17	Output	0
EIM_A18	J22	NVCC_EIM1	GPIO	ALT0	EIM_ADDR18	Output	0

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100K)
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100K)
ENET_REF_CLK[3]	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100K)
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100K)

Table 103. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Updates throughout for Silicon revision D, include: - Figure 1 Part number nomenclature diagram. - Example Orderable Part Number tables, Table 1 • Feature description for Miscellaneous IPs and interfaces; SSI and ESAI. • Table 2, UART 1–5 description change: programmable baud rate up to 5 MHz. • Table 2, uSDHC 1–4 description change: including SDXC cards up to 2 TB. • Table 6, operating range for Run mode: LDO bypassed, minimum value corrected to 1.150 V. • Table 6, table footnotes, added LDO enabled mode footnote for internal LDO output set points. • Table 61, added table footnote to the Comment heading in the Comment column. • Removed table “On-Chip LDOs and their On-Chip Loads.” • Section 4.1.4, External Clock Sources; added Note, “The internal RTC oscillator does not …”. • Section 4.1.5, reworded second paragraph about the power management IC to explain that a robust thermal design is required for the increased system power dissipation. • Table 8, Maximum Supply Currents: NVCC_RGMII Condition value changed to N=6. • Table 8, Maximum Supply currents: Added row; NVCC_LVDS2P5 • Section 4.2.1 Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1 Power-Up Sequence: removed Note. • Section 4.5.2 OSC32K, second paragraph reworded to describe OSC32K automatic switching. • Section 4.5.2 OSC32K, added Note following second paragraph to caution use of internal oscillator use. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih minimum value to 0.8. • Table 21 XTALI and RTC_XTALI DC parameters; changed RTC_XTALI Vih maximum value to 1.1. • Table 37 Reset Timing Parameters; removed footnote. • Section 4.9.3 External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 40. EIM Bus Timing Parameters; reworded footnotes for clarity. • Table 41. EIM Asynchronous Timing Parameters; removed comment from the Max heading cell. • Table 41. EIM Asynchronous Timing Parameters; reworded footnote 2 for clarity. • Table 61. RMII Signal Timing; parameter M19 Max value relaxed to 13.5 ns. • Table 77. MLB 256/512 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 78. MLB 1024 Fs Timing Parameters; added last row for MLBSIG (MLBDAT). • Table 100. Corrected the ALT5 Default Function names. • Figure 106 and Figure 107 21 x 21 mm Lidded Package; updated drawing (Rev D).
Rev. 2.3	07/26 /2013	• Table 100, *21 x 21Functional Contact Assignments*: Restored NANDF_WP_B row and description. • System Timing Parameters Table 37, *Reset timing parameter*, CC1 description clarified, change from: "Duration of SRC_POR_B to be qualified as valid (input slope <= 5 ns)" to: "Duration of SRC_POR_B to be qualified as valid" and added a footnote to the parameter with the following text: "SRC_POR_B rise and fall times must be 5 ns or less." This change was made for clarity and does not represent a specification change.
Rev. 2.2	07/2013	• Editor corrections to revision history links. No technical content changes.
Rev. 2.1	07/2013	• Figure 1, Changed temperature references from Consumer to Commercial. • Table 100, *21 x 21Functional Contact Assignments*: —Removed rows: DRAM_VREF, HDMI_DDCCEC, and HDMI_REF. —Due to a typographical error in revision 2.0, the ball names for rows EIM_DA2 through EIM_DA15 were ordered incorrectly. This has been corrected in revision 2.1. The ball map is correct in both revision 2.0 and 2.1.